Microchip Technology - PIC32MM0016GPL036T-I/M2 Datasheet

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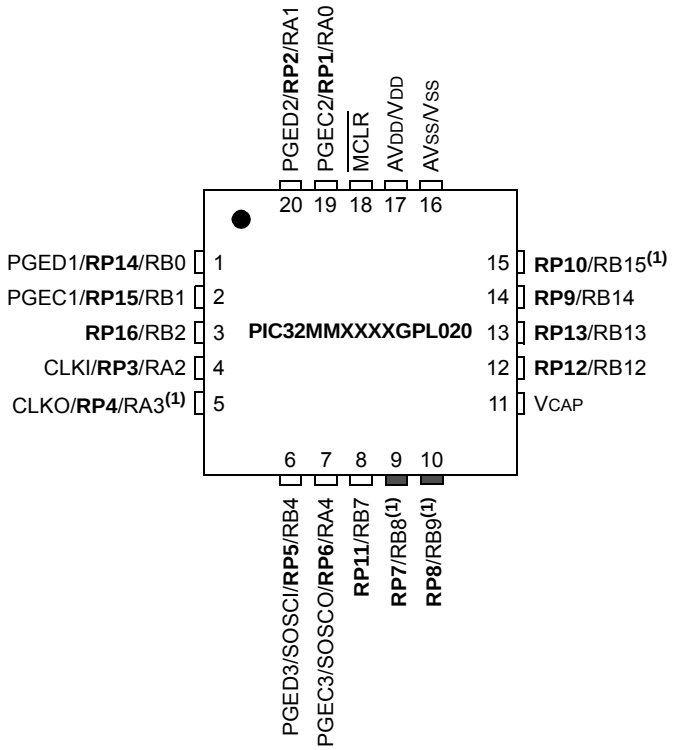
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-SQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl036t-i-m2

Pin Diagrams (Continued)

20-Pin QFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

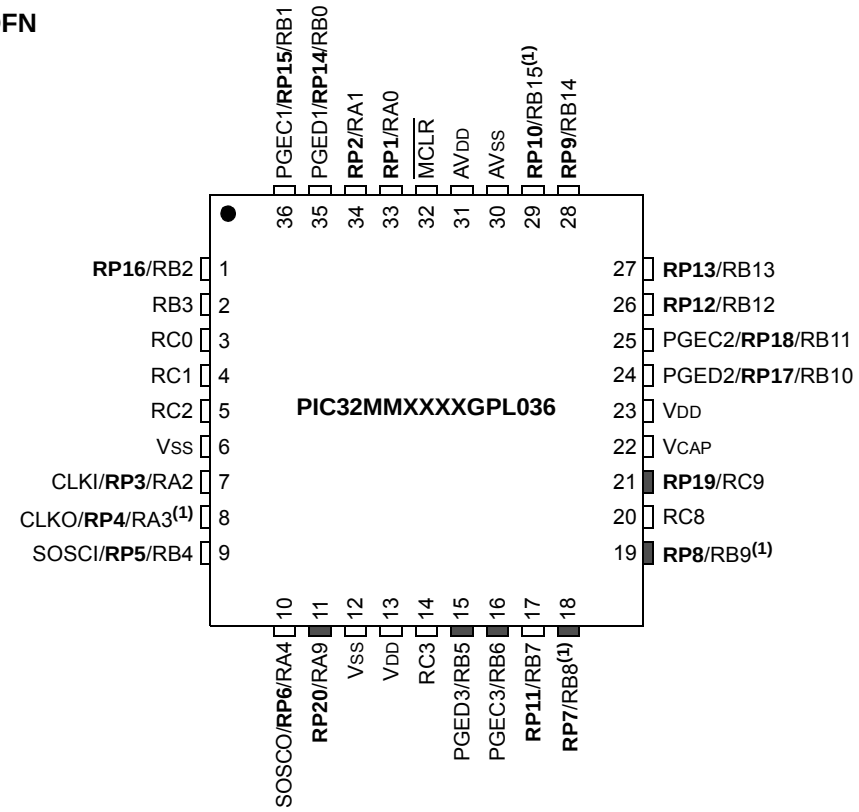
TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN QFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	11	VCAP
2	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	12	TDO/AN7/LVDIN/**RP12**/RB12
3	AN4/**RP16**/RB2	13	TDI/AN8/**RP13**/RB13
4	OSC1/CLKI/AN5/C1INB/**RP3**/OCM1C/RA2	14	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
5	OSC2/CLKO/AN6/C1INA/**RP4**/OCM1D/RA3(1)	15	AN10/REFCLKO/**RP10**/U1RX/$\overline{SS1}$/FSYNC1/INT0/RB15(1)
6	PGED3/SOSCI/**RP5**/RB4	16	AVSS/VSS
7	PGEC3/SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	17	AVDD/VDD
8	**RP11**/RB7	18	$\overline{MCLR}$
9	TCK/**RP7**/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	19	PGEC2/VREF+/AN0/**RP1**/OCM1E/INT3/RA0
10	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)	20	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

36-Pin VQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN VQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP16**/RB2	19	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	AN11/C1INA/RB3	20	RC8
3	AN12/RC0	21	**RP19**/RC9
4	AN13/RC1	22	VCAP
5	RC2	23	VDD
6	VSS	24	PGED2/TDO/**RP17**/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	PGEC2/TDI/**RP18**/RB11
8	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	26	AN7/LVDIN/**RP12**/RB12
9	SOSCI/**RP5**/RB4	27	AN8/**RP13**/RB13
10	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	28	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
11	**RP20**/RA9	29	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
12	VSS	30	AVSS
13	VDD	31	AVDD
14	RC3	32	MCLR
15	PGED3/RB5	33	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	PGEC3/RB6	34	VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP11**/RB7	35	PGED1/AN2/C1IND/C2INB/**RP14**/RB0
18	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1

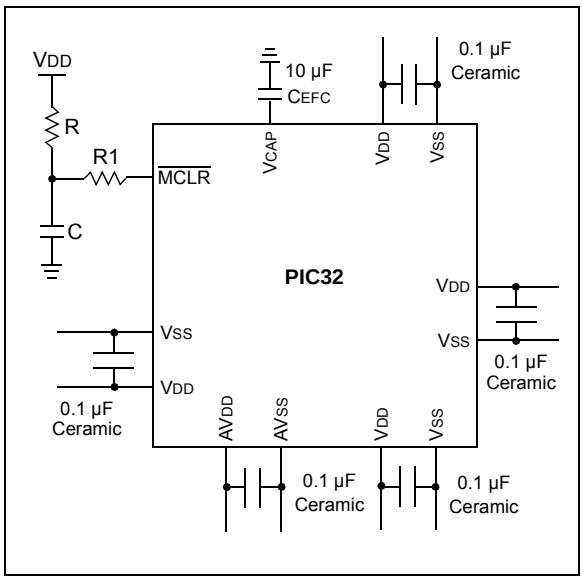
Note 1: Pin has an increased current drive strength.

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
VCAP	11	14	17	20	22	24	P	—	Core voltage regulator filter capacitor connection
VDD	17	20	10,25	13,28	13,23,31	13,26, 34	P	—	Digital modules power supply
VREF-	20	3	28	3	34	37	I	ANA	ADC negative reference
VREF+	19	2	27	2	33	36	I	ANA	ADC and DAC positive reference
VSS	16	19	5,24	8,27	6,12,30	6,12, 33	P	—	Digital modules ground

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides for two specific device functions:

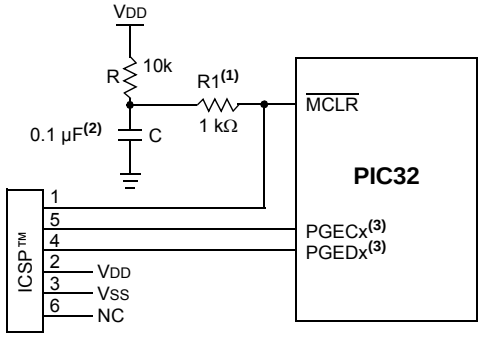
- Device Reset
- Device Programming and Debugging

Pulling The $\overline{MCLR}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{MCLR}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{MCLR}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS(1,2,3)



Note 1: $470\Omega \leq R1 \leq 1\ k\Omega$ will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met without interfering with the debug/programmer tools.

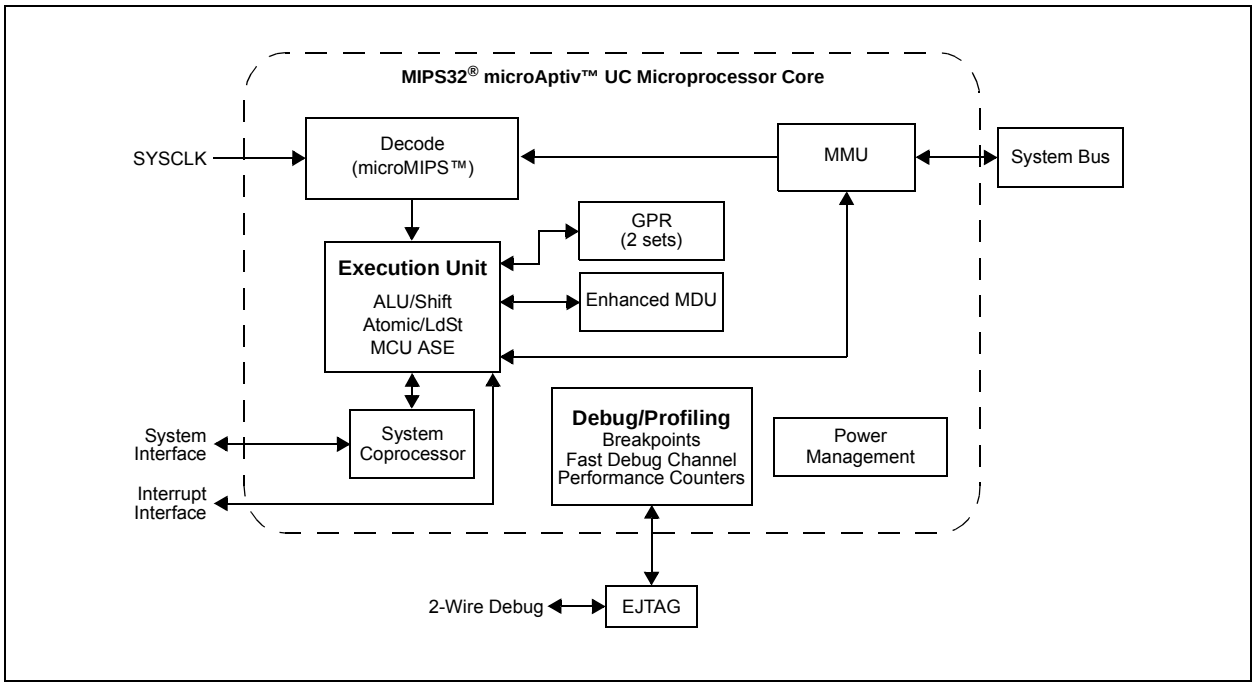
2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.4 Capacitor on Internal Voltage Regulator (V_{CAP})

A low-ESR (<1 Ohm) capacitor is required on the V_{CAP} pin, which is used to stabilize the internal voltage regulator output. The V_{CAP} pin must not be connected to V_{DD} and must have a C_{EFC} capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. The recommended value of the C_{EFC} capacitor is 10 µF. On the printed circuit board, it should be placed as close to the V_{CAP} pin as possible. If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to this capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF.

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



3.2 Architecture Overview

The MIPS32® microAptiv™ UC microprocessor core in the PIC32MM0064GPL036 family devices contains several logic blocks, working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Power Management
- microMIPS Instructions Decoder
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous Multiply/Divide Unit (MDU). The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid Stalls when executing instruction streams where data producing instructions are followed closely by consumers for their results
- Leading zero/one detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The microAptiv UC core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows the long-running MDU operations to be partially masked by system Stalls and/or other Integer Unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, Result/Accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the rs operand. The second number ('16' of 32x16) represents the rt operand. The microAptiv UC core only checks the value of the rt operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back, 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU. Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (rs) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit wide rs, 15 iterations are skipped, and for a 24-bit wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline Stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be re-issued), and latency (number of cycles until a result is available) for the microAptiv UC core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU`, `MADD/MADDU`, `MSUB/MSUBU`	16 bits	1	1
	32 bits	2	2
`MUL` (GPR destination)	16 bits	2	1
	32 bits	3	2
`DIV/DIVU`	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

REGISTER 5-4: NVMDATAx: NVM FLASH DATA x REGISTER (x = 0-1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATAx<31:0>:** NVM Flash Data x bits

Double-Word Program: Writes NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the least significant instruction word.

REGISTER 5-5: NVMSRCADDR: NVM SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** NVM Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	INTCON	31:16	—	—	—	—	—	—	—	—	—	VS<6:0>							0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
F010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
F020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
F030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
F040	IFS0	31:16	CCP2IF	CCT1IF	CCP1IF	—	—	—	U1EIF	U1TXIF	U1RXIF	SPI1RXIF	SPI1TXIF	SPI1EIF	CLC2IF	CLC1IF	LVDIF	CRCIF	0000
		15:0	AD1IF	RTCCIF	CMP2IF	CMP1IF	T1IF	CNCIF(2)	CNBIF	CNAIF	INT4IF	INT3IF	INT2IF	INT1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
F050	IFS1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CPCIF	NVMIF	—	—	—	U2EIF	U2TXIF	U2RXIF	SPI2RXIF	SPI2TXIF	SPI2EIF	—	—	CCT3IF	CCP3IF	CCT2IF	0000
F0C0	IEC0	31:16	CCP2IE	CCT1IE	CCP1IE	—	—	—	U1EIE	U1TXIE	U1RXIE	SPI1RXIE	SPI1TXIE	SPI1EIE	CLC2IE	CLC1IE	LVDIE	CRCIE	0000
		15:0	AD1IE	RTCCIE	CMP2IE	CMP1IE	T1IE	CNCIE(2)	CNBIE	CNAIE	INT4IE	INT3IE	INT2IE	INT1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
F0D0	IEC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CPCIE	NVMIE	—	—	—	U2EIE	U2TXIE	U2RXIE	SPI2RXIE	SPI2TXIE	SPI2EIE	—	—	CCT3IE	CCP3IE	CCT2IE	0000
F140	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
F150	IPC1	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
F160	IPC2	31:16	—	—	—	T1IP<2:0>			T1IS<1:0>		—	—	—	CNCIP<2:0>(2)			CNCIS<1:0>(2)		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
F170	IPC3	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
F180	IPC4	31:16	—	—	—	CLC2IP<2:0>			CLC2IS<1:0>		—	—	—	CLC1IP<2:0>			CLC1IS<1:0>		0000
		15:0	—	—	—	LVDIP<2:0>			LVDIS<1:0>		—	—	—	CRCIP<2:0>			CRCIS<1:0>		0000
F190	IPC5	31:16	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
		15:0	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		0000
F1A0	IPC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	U1EIP<2:0>			U1EIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
F1B0	IPC7	31:16				CCP2IP<2:0>			CCP2IS<1:0>		—	—	—	CCT1IP<2:0>			CCT1IS<1:0>		0000
		15:0	—	—	—	CCP1IP<2:0>			CCP1IS<1:0>		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 20-pin devices.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(3)
- 111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Reserved
- 010 = Primary Oscillator (POSC) (XT, HS or EC)
- 001 = System PLL (SPLL)
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit(4)
- 1 = Enables Secondary Oscillator
- 0 = Disables Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit(2)
- 1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits
- 0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

2: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

3: The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.

4: The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

REGISTER 8-5: CLKSTAT: CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	SPDIVRDY	FRCRDY

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **SPLLRDY**: PLL Lock bit
1 = PLL is locked and ready
0 = PLL is not locked

bit 6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY:** LPRC Oscillator Ready bit
1 = LPRC oscillator is stable and ready
0 = LPRC oscillator is not stable

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready bit
1 = SOSC is stable and ready
0 = SOSC is not stable

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready bit
1 = POSC is stable and ready
0 = POSC is not stable

bit 1 **SPDIVRDY:** System PLL (with postscaler, SPLLDIV) Clock Ready Status bit
1 = SPLLDIV is stable and ready
0 = SPLLDIV is not stable

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready bit
1 = FRC oscillator is stable and ready
0 = FRC oscillator is not stable

9.7 Pin Pull-up and Pull-Down

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source, or sink source, connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

9.8 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features, while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

9.8.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation, “RPn”, in their full pin designation, where “RP” designates a Remappable Peripheral and “n” is the remappable port number.

9.8.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (MCCP, SCCP) and others.

In comparison, some digital only peripheral modules are never included in the PPS feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

9.8.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

10.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

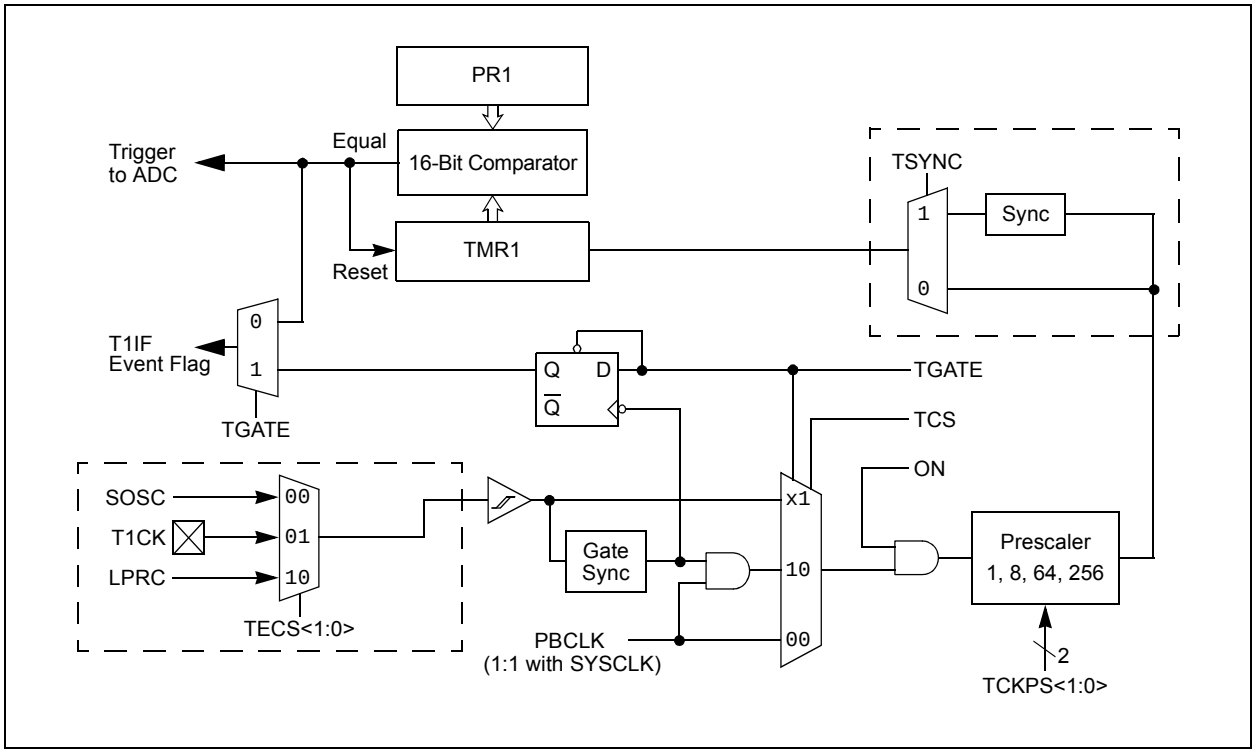
PIC32MM0064GPL036 family devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can be clocked from different sources, such as the Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK), Secondary Oscillator (SOSC), T1CK pin or LPRC oscillator.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

The timer has a selectable clock prescaler and can operate in Sleep and Idle modes.

FIGURE 10-1: TIMER1 BLOCK DIAGRAM



REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 7-6 **TMRPS<1:0>:** CCPx Time Base Prescale Select bits
11 = 1:64 prescaler
10 = 1:16 prescaler
01 = 1:4 prescaler
00 = 1:1 prescaler

bit 5 **T32:** 32-Bit Time Base Select bit
1 = 32-bit time base for timer, single edge output compare or input capture function
0 = 16-bit time base for timer, single edge output compare or input capture function

bit 4 **CCSEL:** Capture/Compare Mode Select bit
1 = Input Capture mode
0 = Output Compare/PWM or Timer mode (exact function is selected by the MOD<3:0> bits)

bit 3-0 **MOD<3:0>:** CCPx Mode Select bits
CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)
CCSEL = 0 (Output Compare modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode
0110 = Center-Aligned Pulse Compare mode, buffered
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode: Toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode: Drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode: Drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode: Output functions are disabled

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

REGISTER 12-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>		
15:8	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
	PWMRSEN	ASDGM	—	SSDG	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ASDG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **OC<F:A>EN:** Output Enable/Steering Control bits(1)
1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 23-22 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 21 **Unimplemented:** Read as '0'

bit 20-19 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output depends on module operating mode
01 = Time base rollover event (all modes)
00 = Disabled

bit 18-16 **ICS<2:0>:** Input Capture Source Select bits
111 = Reserved
110 = Reserved
101 = CLC2 output
100 = CLC1 output
011 = Reserved
010 = Comparator 2 output
001 = Comparator 1 output
000 = ICMx pin (remappable)

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0 = ASEVT must be cleared in software to resume PWM activity on output pins

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.

REGISTER 18-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits

For CLC1:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART1 RX input
011 = SPI1 SDO output
010 = Comparator 2 output
001 = CLC1 output
000 = CLCINA I/O pin

For CLC2:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART2 RX input
011 = SPI2 SDO output
010 = Comparator 2 output
001 = CLC2 output
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits

For CLC1:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion (EOC) event
011 = UART1 TX output
010 = Comparator 1 output
001 = CLC2 output
000 = CLCINB I/O pin

For CLC2:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion event
011 = UART2 TX output
010 = Comparator 1 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits

111 = MCCP1 OCM1C output
110 = MCCP1 OCM1B output
101 = MCCP1 OCM1A output
100 = REFCLKO output
011 = LPRC clock source
010 = SOSC clock source
001 = System clock (FSYS)
000 = CLCINA I/O pin

REGISTER 19-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	ON	COE	CPOL	—	—	—	CEVT	COUT
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Enable bit
- 1 = Comparator is enabled
- 0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is present on the CxOUT pin
- 0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
- 1 = Comparator output is inverted
- 0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
- 1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
- 0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit

When CPOL = 0:
- 1 = $V_{IN+} > V_{IN-}$
- 0 = $V_{IN+} < V_{IN-}$

When CPOL = 1:
- 1 = $V_{IN+} < V_{IN-}$
- 0 = $V_{IN+} > V_{IN-}$

24.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

24.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

24.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

24.9 PICkit 3 In-Circuit Debugger/ Programmer

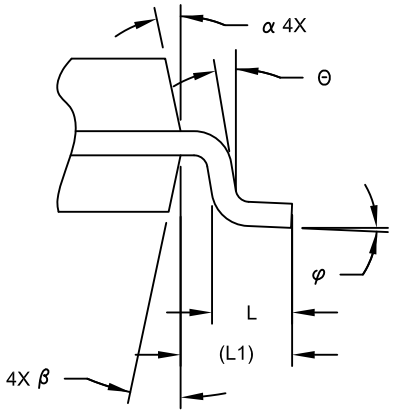
The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

24.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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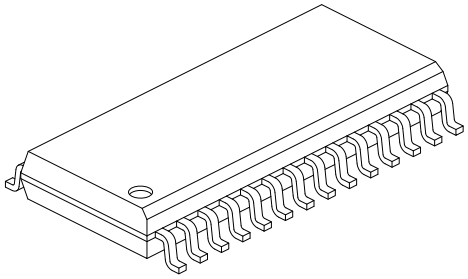

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision A (February 2015)

This is the initial version of the document.

Revision B (May 2016)

This revision incorporates the following updates:

- Registers:
  - Updates Register 5-1, Register 5-3, Register 5-6, Register 5-7, Register 6-3, Register 6-4, Register 7-2, Register 8-2, Register 8-3, Register 8-5, Register 8-6, Register 11-1, Register 13-1, Register 14-1, Register 15-1, Register 15-5, Register 15-6, Register 16-1, Register 16-2, Register 16-3, Register 16-5, Register 18-2, Register 19-1, Register 19-2 and Register 23-7
- Tables:
  - Updates Table 1-1, Table 5-1, Table 6-1,Table 7-2, Table 7-3, Table 9-3, Table 9-7, Table 15-1, Table 16-1, Table 19-1, Table 22-1, Table 23-4, Table 23-5 Table 26-2, Table 26-3, Table 26-4 and Table 26-6 through Table 26-33
  - Adds Table 23-8
- Figures:
  - Updates Figure 1-1, Figure 3-1, Figure 8-1, Figure 10-1, Figure 14-1, Figure 13-1, Figure 14-1, Figure 14-1, Figure 15-1, Figure 17-1, Figure 18-1, Figure 18-3, Figure 26-1, Figure 26-3, Figure 26-4, Figure 26-9, Figure 26-10, Figure 26-11 and Figure 26-12
- Updates pin function descriptions in **Section 1.0 “Device Overview”**
- Updates text in **Section 9.6 “Input Change Notification (ICN)”**, **Section 9.8.4 “Input Mapping”**, **Section 23.7 “Unique Device Identifier (UDID)”**, **Section 22.5 “Low-Power Brown-out Reset”** and **Section 27.0 “Packaging Information”**
- Adds **Section 5.1 “Flash Controller Registers Write Protection”**, **Section 8.0 “Oscillator Configuration”**, **Section 23.4 “System Registers Write Protection”**, reference to **Section 22.1 “Sleep Mode”**, **Section 22.2 “Idle Mode”** and **Section 23.8 “Reserved Registers”**
- Updates the Absolute Maximum Ratings in **Section 26.0 “Electrical Characteristics”**

This revision also includes minor typographical and formatting changes throughout the data sheet text.

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