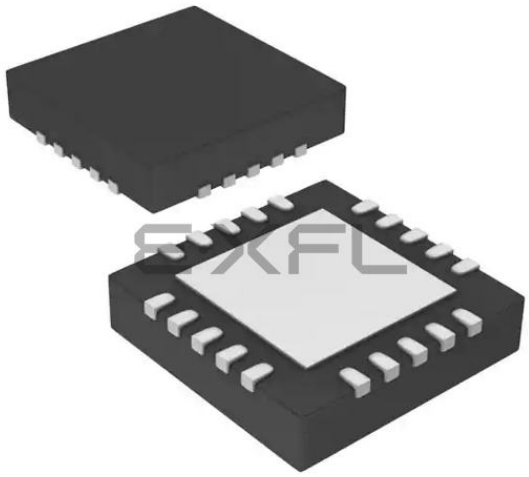

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## What is "Embedded - Microcontrollers"?

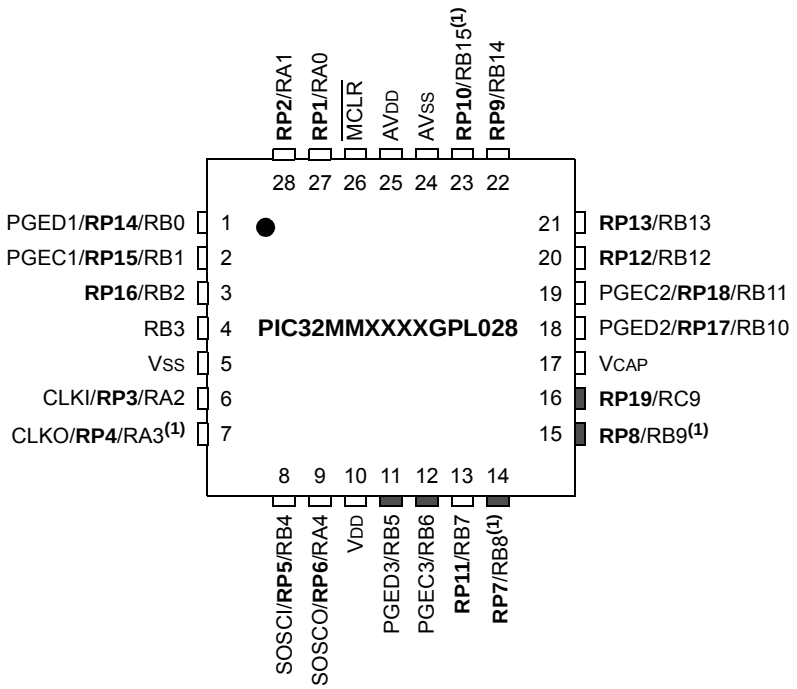
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 11x10/12b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-VFQFN Exposed Pad |
| Supplier Device Package | 20-QFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl020-e-ml |

## Pin Diagrams (Continued)

**28-Pin QFN/UQFN**




**Legend:** Shaded pins are up to 5V tolerant.

**Note 1:** Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

### TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | PGED1/AN2/C1IND/C2INB/**RP14**/RB0 | 15 | TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1) |
| 2 | PGEC1/AN3/C1INC/C2INA/**RP15**/RB1 | 16 | **RP19**/RC9 |
| 3 | AN4/C1INB/**RP16**/RB2 | 17 | VCAP |
| 4 | AN11/C1INA/RB3 | 18 | PGED2/TDO/**RP17**/RB10 |
| 5 | VSS | 19 | PGEC2/TDI/**RP18**/RB11 |
| 6 | OSC1/CLKI/AN5/**RP3**/OCM1C/RA2 | 20 | AN7/LVDIN/**RP12**/RB12 |
| 7 | OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1) | 21 | AN8/**RP13**/RB13 |
| 8 | SOSCI/**RP5**/RB4 | 22 | CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14 |
| 9 | SOSCO/SCLKI/**RP6**/PWRLCLK/RA4 | 23 | AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1) |
| 10 | VDD | 24 | AVSS |
| 11 | PGED3/RB5 | 25 | AVDD |
| 12 | PGEC3/RB6 | 26 | MCLR |
| 13 | **RP11**/RB7 | 27 | VREF+/AN0/**RP1**/OCM1E/INT3/RA0 |
| 14 | TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1) | 28 | VREF-/AN1/**RP2**/OCM1F/RA1 |

**Note 1:** Pin has an increased current drive strength.


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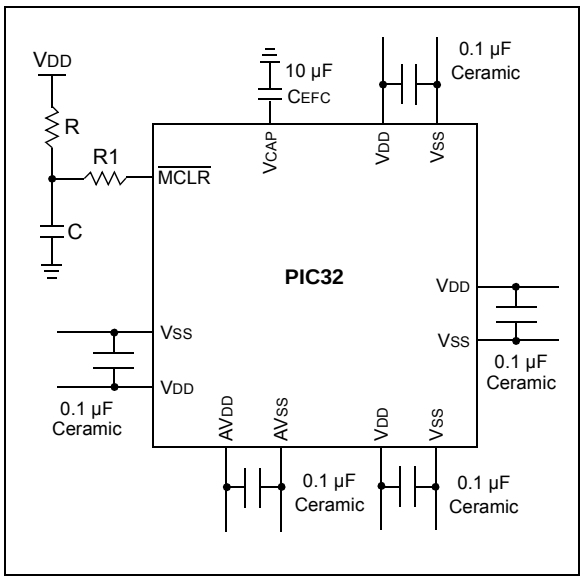
**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**




### 2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

## 2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides for two specific device functions:

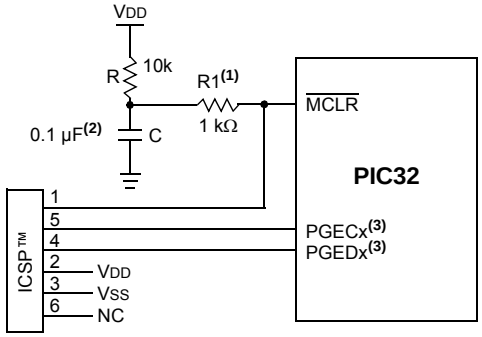
- Device Reset
- Device Programming and Debugging

Pulling The $\overline{MCLR}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{MCLR}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels ($V_{IH}$ and $V_{IL}$) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{MCLR}$ pin.

**FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS(1,2,3)**




**Note 1:** $470\Omega \leq R1 \leq 1\ k\Omega$ will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin $V_{IH}$ and $V_{IL}$ specifications are met without interfering with the debug/programmer tools.

**2:** The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

**3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

## 2.4 Capacitor on Internal Voltage Regulator ($V_{CAP}$)

A low-ESR (<1 Ohm) capacitor is required on the $V_{CAP}$ pin, which is used to stabilize the internal voltage regulator output. The $V_{CAP}$ pin must not be connected to $V_{DD}$ and must have a $C_{EFC}$ capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. The recommended value of the $C_{EFC}$ capacitor is 10 µF. On the printed circuit board, it should be placed as close to the $V_{CAP}$ pin as possible. If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to this capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF.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**REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-1 |
| | — | — | — | — | — | — | — | NF |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented


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**REGISTER 6-4: PWRCON: POWER CONTROL REGISTER(1)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | SBOREN(3) | RETEN(2) | VREGS(2) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **SBOREN:** BOR During Sleep Control bit(3)
- 1 = BOR is turned on
- 0 = BOR is turned off

bit 1 **RETEN:** Output Level of the Regulator During Sleep Selection bit(2)
- 1 = Writing a '1' to this bit will cause the main regulator to be put in a low-power state during Sleep mode
- 0 = Writing a '0' to this bit will have no effect

bit 0 **VREGS:** Voltage Regulator Standby Enable bit(2)
- 1 = Voltage regulator will remain active during Sleep mode
- 0 = Voltage regulator will go to Standby mode during Sleep mode

**Note 1:** Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

**2:** Refer to **Section 22.4 "On-Chip Voltage Regulator Low-Power Modes"** for details.

**3:** This bit is enabled only when the BOREN<1:0> Configuration bits (FPOR<1:0>) are set to '01'.


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**REGISTER 8-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(3)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = REFCLKI pin
1000 = Reserved
0111 = System PLL output (not divided)
0110 = Reserved
0101 = Secondary Oscillator (SOSC)
0100 = Low-Power RC Oscillator (LPRC)
0011 = Fast RC Oscillator (FRC)
0010 = Primary Oscillator (POSC)
0001 = Instruction/System Clock (SYSCLK)
0000 = Instruction/System Clock (SYSCLK)

**Note 1:** Do not write to this register when the ON bit is not equal to the ACTIVE bit.

**2:** This bit is ignored when the ROSEL<3:0> bits = 0000.

**3:** The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.


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## 9.9 I/O Ports Control Registers

**TABLE 9-4: PORTA REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(3) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2600 | ANSELA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | ANSA<3:0> | | | | 000F |
| 2610 | TRISA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISA9(1,2) | — | — | — | — | TRISA<4:0> | | | | | 021F |
| 2620 | PORTA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RA9(1,2) | — | — | — | — | RA<4:0> | | | | | xxxx |
| 2630 | LATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATA9(1,2) | — | — | — | — | LATA<4:0> | | | | | 0000 |
| 2640 | ODCA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCA9(1,2) | — | — | — | — | ODCA<4:0> | | | | | 0000 |
| 2650 | CNPUA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPUA9(1,2) | — | — | — | — | CNPUA<4:0> | | | | | 0000 |
| 2660 | CNPDA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPDA9(1,2) | — | — | — | — | CNPDA<4:0> | | | | | 0000 |
| 2670 | CNCONA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | CNSTYLE | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2680 | CNEN0A | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNIEA9(1,2) | — | — | — | — | CNIEA<4:0> | | | | | 0000 |
| 2690 | CNSTATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNSTATA9(1,2) | — | — | — | — | CNSTATA<4:0> | | | | | 0000 |
| 26A0 | CNEN1A | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNIE1A9(1,2) | — | — | — | — | CNIE1A<4:0> | | | | | 0000 |
| 26B0 | CNFA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNFA9(1,2) | | — | — | — | CNFA<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These bits are not implemented in 20-pin devices.

**2:** These bits are not implemented in 28-pin devices.

**3:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.



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**TABLE 9-5: PORTB REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(2) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2700 | ANSELB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ANSB<15:12> | | | | — | — | — | — | — | — | — | — | ANSB<3:0>(1) | | | | F00F |
| 2710 | TRISB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISB<15:0>(1) | | | | | | | | | | | | | | | | FFFF |
| 2720 | PORTB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 2730 | LATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 2740 | ODCB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 2750 | CNPUB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 2760 | CNPDB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 2770 | CNCONB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | CNSTYLE | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 2780 | CNEN0B | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 2790 | CNSTATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNSTATB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 27A0 | CNEN1B | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIE1B<15:0>(1) | | | | | | | | | | | | | | | | 0000 |
| 27B0 | CNFB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNFB<15:0>(1) | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Bits<11:10,6:5,3> are not implemented in 20-pin devices.

**2:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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## 14.1 UART Control Registers

**TABLE 14-1: UART1 AND UART2 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0600 | U1MODE(1) | 31:16 | — | — | — | — | — | — | — | — | SLPEN | ACTIVE | — | — | — | CLKSEL<1:0> | | OVFDIS | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 0610 | U1STA(1) | 31:16 | UART1 MASK<7:0> | | | | | | | | UART1 ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 0620 | U1TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | UART1 Transmit Register | | | | | | | | 0000 |
| 0630 | U1RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | UART1 Receive Register | | | | | | | | 0000 |
| 0640 | U1BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 0680 | U2MODE(1) | 31:16 | — | — | — | — | — | — | — | — | SLPEN | ACTIVE | — | — | — | CLKSEL<1:0> | | OVFDIS | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 0690 | U2STA(1) | 31:16 | UART2 MASK<7:0> | | | | | | | | UART2 ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 06A0 | U2TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | UART2 Transmit Register | | | | | | | | 0000 |
| 06B0 | U2RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | UART2 Receive Register | | | | | | | | 0000 |
| 06C0 | U2BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These registers have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.



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**REGISTER 14-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits(1)
11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start Bit Detect During Sleep Mode bit
1 = Wake-up is enabled
0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement is disabled or has completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock is enabled
0 = Standard Speed mode – 16x baud clock is enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

**Note 1:** These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).


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**REGISTER 15-3: RTCSTAT: RTCC STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R-0, HS, HC | U-0 | U-0 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | — | — | ALMEVT | — | — | SYNC | ALMSYNC | HALFSEC |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
- 1 = An alarm event has occurred
- 0 = An alarm event has not occurred

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Synchronization Status bit
- 1 = Time registers may change during software read
- 0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization status bit
- 1 = Alarm registers (ALMTIME and ALMDATE) and RTCCON1 should not be modified; the ALRMEN and ALMRPT<7:0> bits may change during software read
- 0 = Alarm registers and Alarm Control registers may be modified safely

bit 0 **HALFSEC:** Half Second Status bit
- 1 = Second half of 1-second period
- 0 = First half of 1-second period


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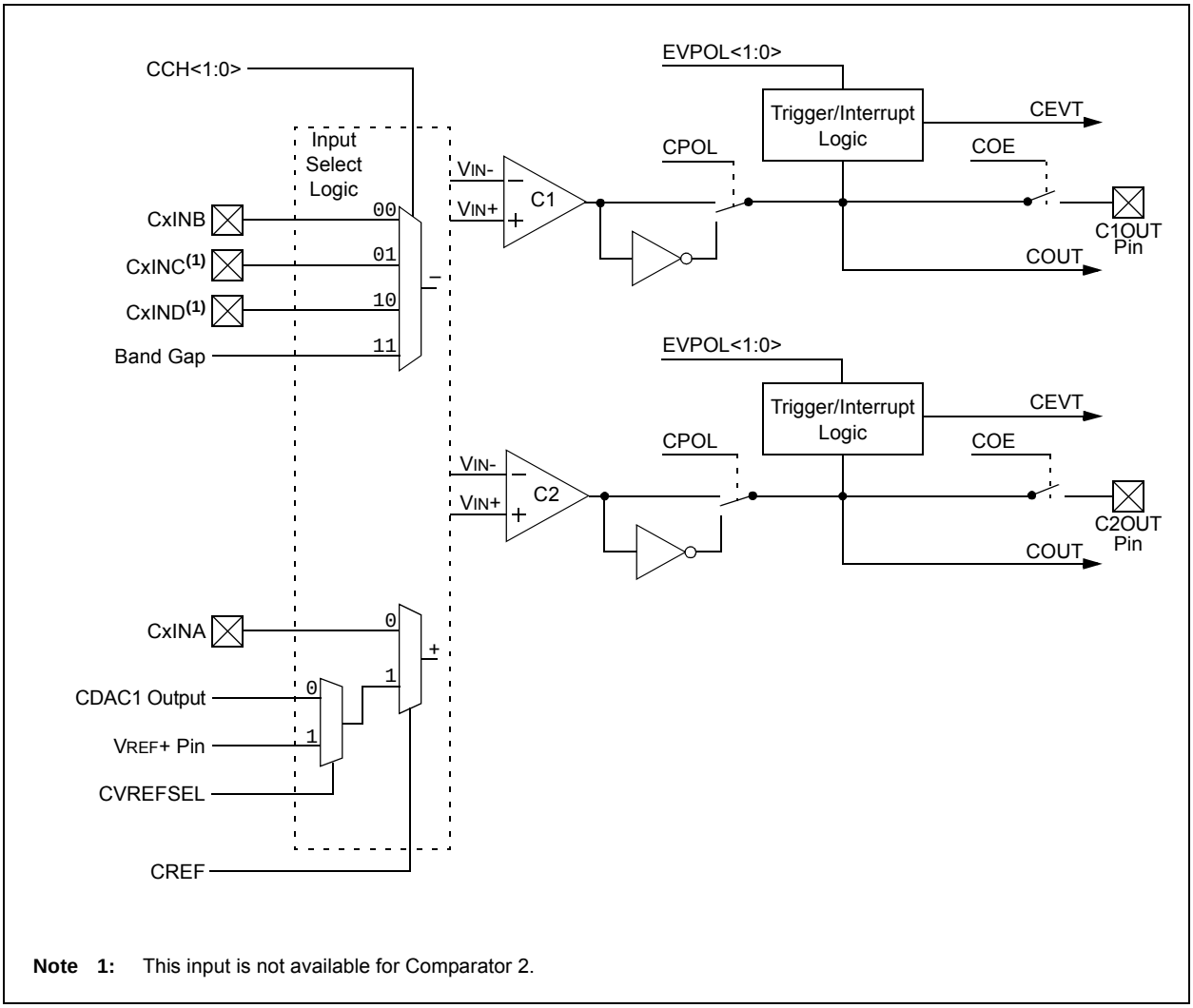
## 19.0 COMPARATOR

**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides two dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 19-1. Each comparator has its own control register, CMxCON (Register 19-2), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (Register 19-1).

**FIGURE 19-1: DUAL COMPARATOR MODULE BLOCK DIAGRAM**




**Note 1:** This input is not available for Comparator 2.

## 19.1 Comparator Control Registers

**TABLE 19-1: COMPARATOR 1 AND 2 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0900 | CMSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | C2EVT | C1EVT | 0000 |
| | | 15:0 | — | — | SIDL | — | — | — | — | CVREFSEL | — | — | — | — | — | — | C2OUT | C1OUT | 0000 |
| 0910 | CM1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 0000 |
| 0930 | CM2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.



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## 24.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 24.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 24.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 24.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

## 24.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

## 25.0 INSTRUCTION SET

The PIC32MM0064GPL036 family instruction set complies with the MIPS® Release 3 instruction set architecture. Only microMIPS32™ instructions are supported. The PIC32MM0064GPL036 family does not have the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

**Note:** Refer to the *"MIPS® Architecture for Programmers Volume II-B: The microMIPS32™ Instruction Set"* at www.imgtec.com for more information.

**TABLE 26-9: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS**

| **Operating Conditions:** 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Max.** | **Units** | **Conditions** |
| DI60a | IICL | **Input Low Injection Current** | 0 | -5**(1,4)** | mA | This parameter applies to all pins. |
| DI60b | IICH | **Input High Injection Current** | 0 | +5**(2,3,4)** | mA | This parameter applies to all pins, with the exception of all 5V tolerant pins and SOSCI. Maximum IICH current for these exceptions is 0 mA. |
| DI60c | ∑IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20**(5)** | +20**(5)** | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins, ( \| IICL + \| IICH \| ) ≤ ∑IICT |

**Note 1:** VIL Source < (VSS – 0.3). Characterized but not tested.

**2:** VIH Source > (VDD + 0.3) for non-5V tolerant pins only.

**3:** Digital 5V tolerant pins do not have an internal high-side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

**4:** Injection currents can affect the ADC results.

**5:** Any number and/or combination of I/O pins, not excluded under IICL or IICH conditions, are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit.

**TABLE 26-22: RESET, BROWN-OUT RESET AND SLEEP MODES TIMING SPECIFICATIONS**

| **Operating Conditions:** 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| SY10 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (Low) | 2 | — | — | µs | |
| SY13 | TIOZ | I/O High-Impedance from $\overline{\text{MCLR}}$ Low | — | 1 | — | µs | |
| SY25 | TBOR | Brown-out Reset Pulse Width | 1 | — | — | µs | VDD ≤ VBOR |
| SY45 | TRST | Reset State Time | — | 25 | — | µs | |
| SY71 | TWAKE(2) | Wake-up Time with Main Voltage Regulator | — | 22 | — | µs | Sleep wake-up with VREGS = 0, RETEN = 0, RETVR = 1 |
| | | | — | 3.8 | — | µs | Sleep wake-up with VREGS = 1, RETEN = 0, RETVR = 1 |
| SY72 | TWAKELVR(2) | Wake-up Time with Retention Low-Voltage Regulator | — | 163 | — | µs | Sleep wake-up with VREGS = 0, RETEN = 1, RETVR = 0 |
| | | | — | 23 | — | µs | Sleep wake-up with VREGS = 1, RETEN = 1, RETVR = 0 |

**Note 1:** Data in the “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The parameters are measured with the external clock source (EC). To get the full wake-up time, the oscillator start-up time must be added.

**FIGURE 26-9: MCCP AND SCCP PWMx MODE TIMING CHARACTERISTICS**

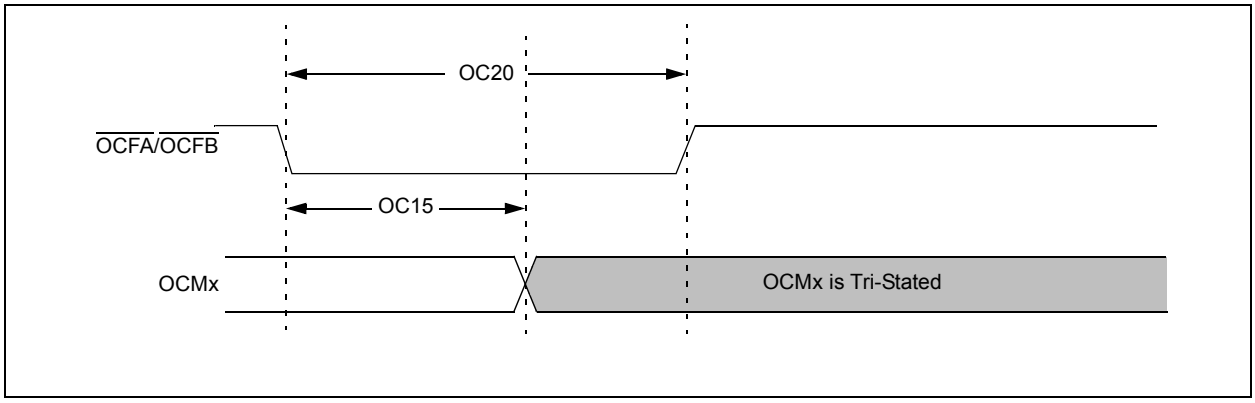



**TABLE 26-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS**

| **Operating Conditions:** 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated) | | | | | |
|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics(1)** | **Min** | **Max** | **Units** |
| OC15 | TFD | Fault Input to PWM I/O Change | — | 30 | ns |
| OC20 | TFLT | Fault Input Pulse Width | 10 | — | ns |

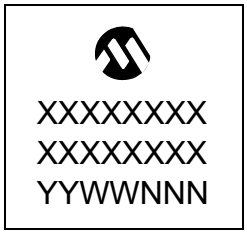
**Note 1:** These parameters are characterized but not tested in manufacturing.

### 27.1 Package Marking Information (Continued)

28-Lead SSOP

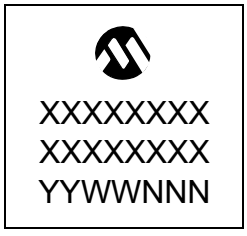

Example


28-Lead QFN



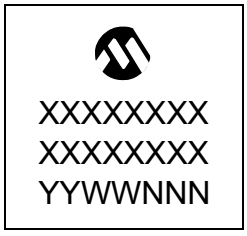

Example


28-Lead UQFN



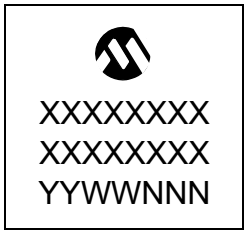

Example


36-Lead VQFN




Example


40-Lead UQFN




Example



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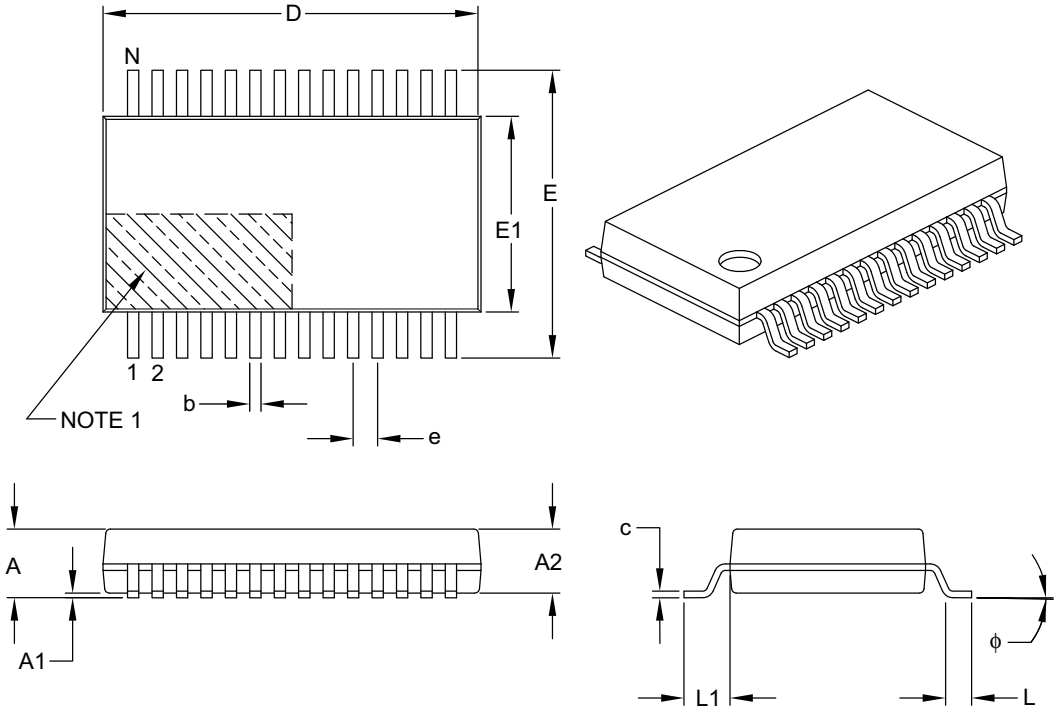
### 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | | 1.25 REF | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B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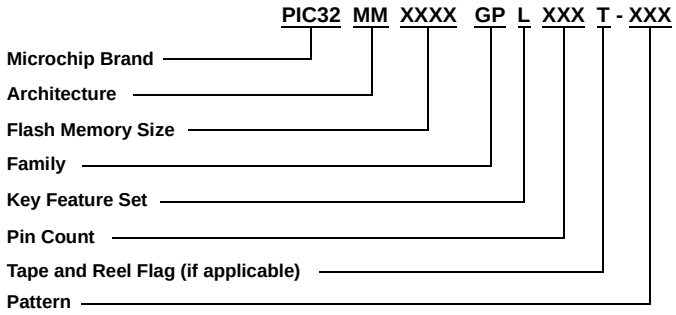
## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.




| | | |
|---|---|---|
| Architecture | MM | = MIPS32® microAptiv™ UC CPU Core |
| Flash Memory Size | 0016<br>0032<br>0064 | = 16 Kbytes<br>= 32 Kbytes<br>= 64 Kbytes |
| Family | GP | = General Purpose Family |
| Key Feature | L | = Up to 25 MHz operating frequency with basic peripheral set of 2 UART and 2 SPI modules |
| Pin Count | 020<br>028<br>036 | = 20-pin<br>= 28-pin<br>= 36/40-pin |
| Pattern | Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)<br>ES | = Engineering Sample |

**Example:**

PIC32MM0064GPL036-I/M2: PIC32 General Purpose Device with MIPS32® microAptiv™ UC Core, 64-Kbyte Program Memory, 36-Pin Package.