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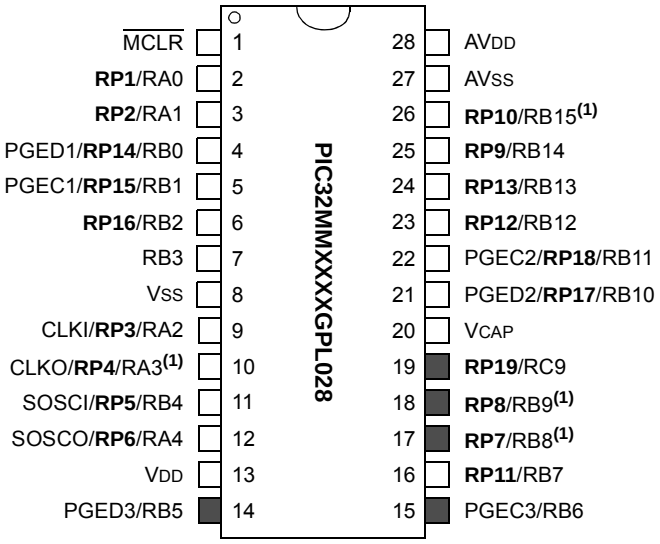
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl020-e-ss

Pin Diagrams (Continued)

28-Pin SPDIP(2)/SSOP/SOIC



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

2: Only PIC32MM0064GPL028 comes in a 28-pin SPDIP package.

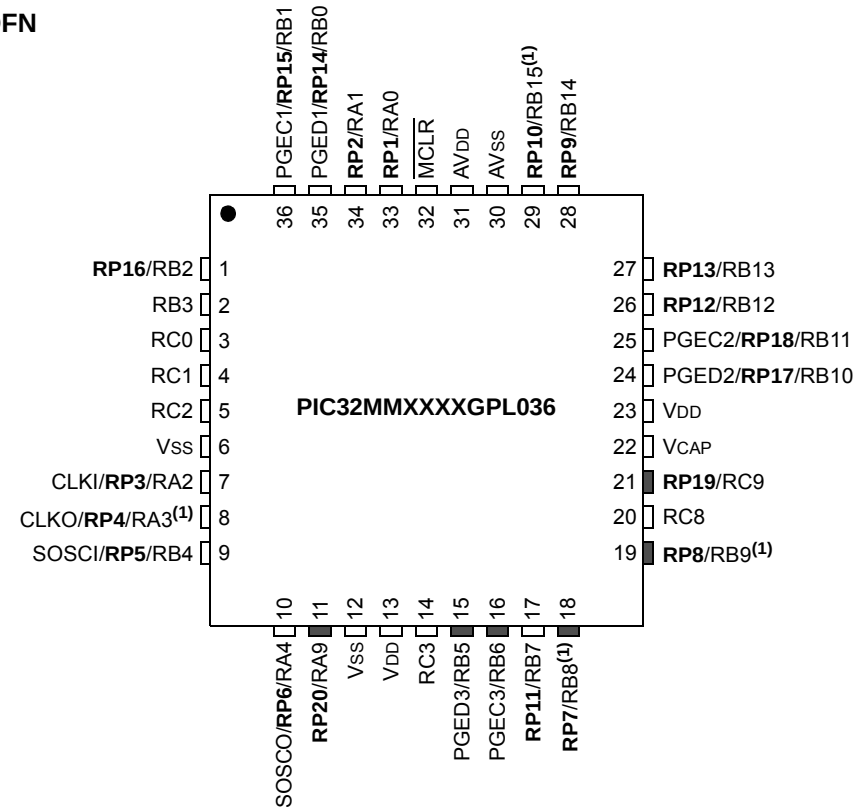
TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN SPDIP/SSOP/SOIC DEVICES

Pin	Function	Pin	Function
1	MCLR	15	PGEC3/RB6
2	VREF+/AN0/**RP1**/OCM1E/INT3/RA0	16	**RP11**/RB7
3	VREF-/AN1/**RP2**/OCM1F/RA1	17	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)
4	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	18	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
5	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	19	**RP19**/RC9
6	AN4/C1INB/**RP16**/RB2	20	VCAP
7	AN11/C1INA/RB3	21	PGED2/TDO/**RP17**/RB10
8	VSS	22	PGEC2/TDI/**RP18**/RB11
9	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	23	AN7/LVDIN/**RP12**/RB12
10	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	24	AN8/**RP13**/RB13
11	SOSCI/**RP5**/RB4	25	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
12	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	26	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
13	VDD	27	AVSS
14	PGED3/RB5	28	AVDD

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

36-Pin VQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN VQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP16**/RB2	19	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	AN11/C1INA/RB3	20	RC8
3	AN12/RC0	21	**RP19**/RC9
4	AN13/RC1	22	VCAP
5	RC2	23	VDD
6	VSS	24	PGED2/TDO/**RP17**/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	PGEC2/TDI/**RP18**/RB11
8	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	26	AN7/LVDIN/**RP12**/RB12
9	SOSCI/**RP5**/RB4	27	AN8/**RP13**/RB13
10	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	28	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
11	**RP20**/RA9	29	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
12	VSS	30	AVSS
13	VDD	31	AVDD
14	RC3	32	MCLR
15	PGED3/RB5	33	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	PGEC3/RB6	34	VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP11**/RB7	35	PGED1/AN2/C1IND/C2INB/**RP14**/RB0
18	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1

Note 1: Pin has an increased current drive strength.

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NOTES:

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The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information is available by accessing the CP0 registers listed in Table 3-2.

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REGISTER 6-4: PWRCON: POWER CONTROL REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SBOREN(3)	RETEN(2)	VREGS(2)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **SBOREN:** BOR During Sleep Control bit(3)
- 1 = BOR is turned on
- 0 = BOR is turned off

bit 1 **RETEN:** Output Level of the Regulator During Sleep Selection bit(2)
- 1 = Writing a '1' to this bit will cause the main regulator to be put in a low-power state during Sleep mode
- 0 = Writing a '0' to this bit will have no effect

bit 0 **VREGS:** Voltage Regulator Standby Enable bit(2)
- 1 = Voltage regulator will remain active during Sleep mode
- 0 = Voltage regulator will go to Standby mode during Sleep mode

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

2: Refer to **Section 22.4 "On-Chip Voltage Regulator Low-Power Modes"** for details.

3: This bit is enabled only when the BOREN<1:0> Configuration bits (FPOR<1:0>) are set to '01'.

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REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER (CONTINUED)

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>(1)				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
11111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

9.7 Pin Pull-up and Pull-Down

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source, or sink source, connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

9.8 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features, while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

9.8.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation, “RPn”, in their full pin designation, where “RP” designates a Remappable Peripheral and “n” is the remappable port number.

9.8.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (MCCP, SCCP) and others.

In comparison, some digital only peripheral modules are never included in the PPS feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

9.8.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

TABLE 9-6: PORTC REGISTER MAP

Virtual Address (BF80_#)	Register Name(3)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2800	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC<1:0>(1,2)		0003
2810	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISC<9:8>(1,2)		—	—	—	—	TRISC<3:0>(1,2)				030F
2820	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RC<9:8>(1,2)		—	—	—	—	RC<3:0>(1,2)				0000
2830	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATC<9:8>(1,2)		—	—	—	—	LATC<3:0>(1,2)				0000
2840	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCC<9:8>(1,2)		—	—	—	—	ODCC<3:0>(1,2)				0000
2850	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUC<9:8>(1,2)		—	—	—	—	CNPUC<3:0>(1,2)				0000
2860	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDC<9:8>(1,2)		—	—	—	—	CNPDC<3:0>(1,2)				0000
2870	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON(1)	—	—	—	CNSTYLE(1)	—	—	—	—	—	—	—	—	—	—	—	0000
2880	CNEN0C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIE0C<9:8>(1,2)		—	—	—	—	CNIE0C<3:0>(1,2)				0000
2890	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNSTATC<9:8>(1,2)		—	—	—	—	CNSTATC<3:0>(1,2)				0000
28A0	CNEN1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIE1C<9:8>(1,2)		—	—	—	—	CNIE1C<3:0>(1,2)				0000
28B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFC<9:8>(1,2)		—	—	—	—	CNFC<3:0>(1,2)				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits<15,11,9:8,3:0> are not implemented in 20-pin devices.

2: Bits<8,3:0> are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 15-1: RTCCON1: RTCC CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	WRLOCK(2)	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RTCOE	OUTSEL<2:0>			—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits(1)
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: To clear this bit, an unlock sequence is required. Refer to **Section 23.4 "System Registers Write Protection"** for details.

REGISTER 16-6: AD1CSS: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	—	CSS<30:28>			—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CSS<13:8>(1,2)					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-28 **CSS<30:28>:** ADC Input Pin Scan Selection bits
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

bit 27-14 **Unimplemented:** Read as '0'

bit 13-0 **CSS<13:0>:** ADC Input Pin Scan Selection bits(1,2)
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

Note 1: The CSS<13:11> bits are not implemented in 20-pin devices.
2: The CSS<13:12> bits are not implemented in 28-pin devices.

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23.5 Band Gap Voltage Reference

PIC32MM0064GPL036 family devices have a precision voltage reference band gap circuit used by many modules. The analog buffers are implemented between the band gap circuit and these modules. The buffers are automatically enabled by the hardware if some part of the device needs the band gap reference. The stabilization time is required when the buffer is switched on. The software can enable these buffers in advance to allow the band gap voltage to stabilize before the module uses it. The ANCFG register contains bits to enable the band gap buffers for the comparators (VBGCMP bit) and ADC (VBGADC bit). Refer to Table 23-6 and Register 23-10 for more information.

23.6 Programming and Diagnostics

PIC32MM0064GPL036 family devices provide a complete range of programming and diagnostic features:

- Simplified Field Programmability using Two-Wire In-Circuit Serial Programming™ (ICSP™) Interfaces
- Debugging using ICSP
- Programming and Debugging Capabilities using the EJTAG Extension of JTAG
- JTAG Boundary Scan Testing for Device and Board Diagnostics

23.7 Unique Device Identifier (UDID)

PIC32MM0064GPL036 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 32-bit program words. When taken together, these fields form a unique 160-bit identifier.

The UDID is stored in five read-only locations, located from 0xBFC41840 to 0xBFC41854 in the device configuration space. Table 23-7 lists the addresses of the Identifier Words.

23.8 Reserved Registers

PIC32MM0064GPL036 family devices have 3 reserved registers, located at 0xBF800400, 0xBF800480 and 0xBF802280. The application code must not modify these reserved locations. Table 23-8 lists the addresses of these reserved registers.

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23.9 Configuration Words and System Registers

TABLE 23-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
17D4	FOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

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TABLE 23-4: ALTERNATE CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
1740	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1744	AFDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
1748	AFICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
174C	AFPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
1750	AFWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
1754	AFOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
1758	AFSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
175C	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1760	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1764	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

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TABLE 23-7: UNIQUE DEVICE IDENTIFIER (UDID) REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1840	UDID1	31:16	UDID Word 1<31:0>																xxxx
		15:0																	xxxx
1844	UDID2	31:16	UDID Word 2<31:0>																xxxx
		15:0																	xxxx
1848	UDID3	31:16	UDID Word 3<31:0>																xxxx
		15:0																	xxxx
184C	UDID4	31:16	UDID Word 4<31:0>																xxxx
		15:0																	xxxx
1850	UDID5	31:16	UDID Word 5<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 23-8: RESERVED REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	RESERVED1	31:16	Reserved Register 1<31:0>																0000
		15:0																	0000
0480	RESERVED2	31:16	Reserved Register 2<31:0>																0000
		15:0																	0000
2280	RESERVED3	31:16	Reserved Register 3<31:0>																0C00
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 26-14: COMPARATOR SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
D300	VIOFF	Input Offset Voltage	-20	—	20	mV
D301	VICM	Input Common-Mode Voltage	AVSS – 0.3V	—	AVDD + 0.3V	V
D307	TRESP(1)	Response Time	—	150	—	ns

Note 1: Measured with one input at VDD/2 and the other transitioning from VSS to VDD.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-15: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
VRD310	TSET	Settling Time(1)	—	—	10	µs
VRD311	VRA	Accuracy	-1	—	1	LSb
VRD312	VRUR	Unit Resistor Value (R)	—	4.5	—	kΩ

Note 1: Measures the interval while VRDAT<4:0> transitions from '11111' to '00000'.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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FIGURE 26-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

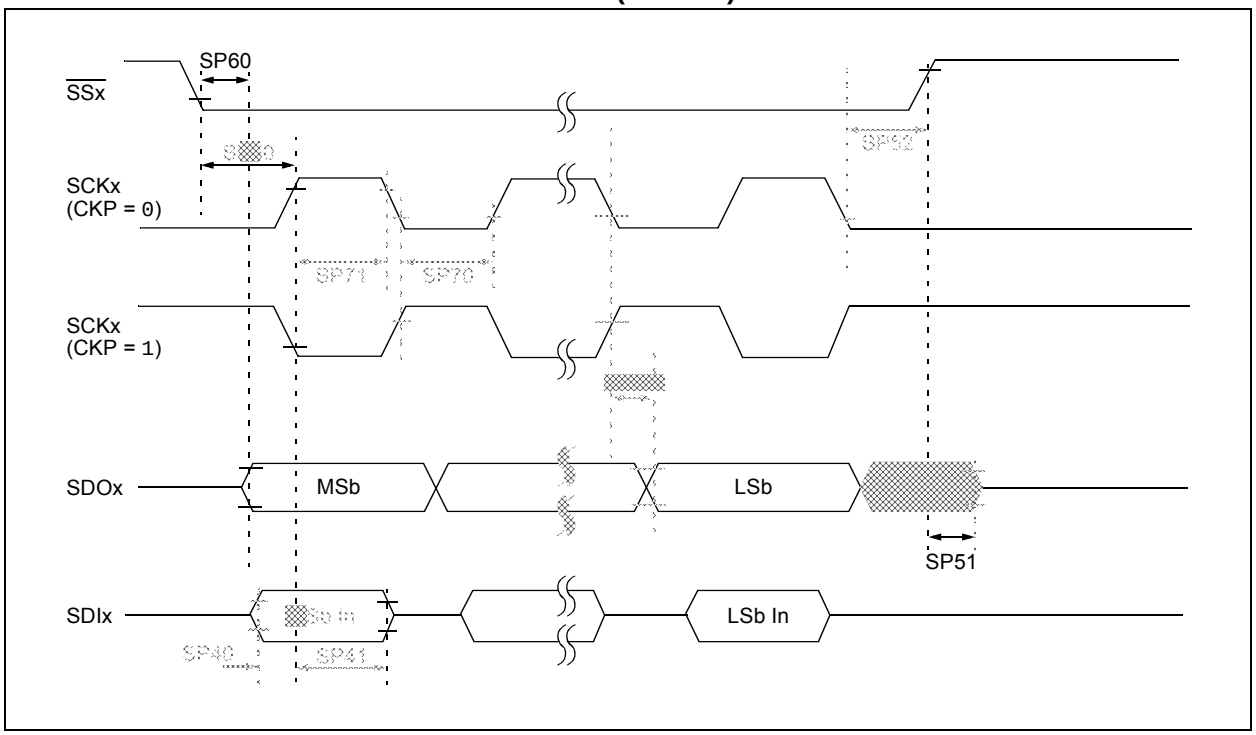

TABLE 26-29: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C (unless otherwise stated)					
Param.No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
SP70	TscL	SCKx Input Low Time	10	—	ns
SP71	TscH	SCKx Input High Time	10	—	ns
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	ns
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	ns
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	40	—	ns
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	2.5	12	ns
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	ns
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	12.5	ns

Note 1: These parameters are characterized but not tested in manufacturing.

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NOTES:

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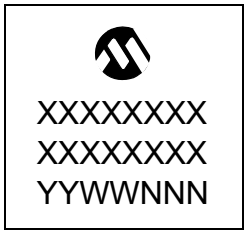
27.1 Package Marking Information (Continued)

28-Lead SSOP

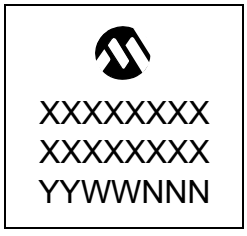
Example

28-Lead QFN



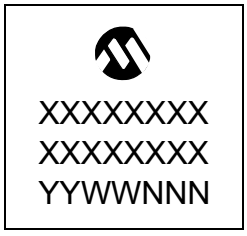
Example

28-Lead UQFN



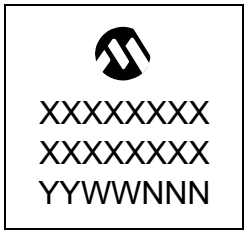
Example

36-Lead VQFN



Example

40-Lead UQFN



Example

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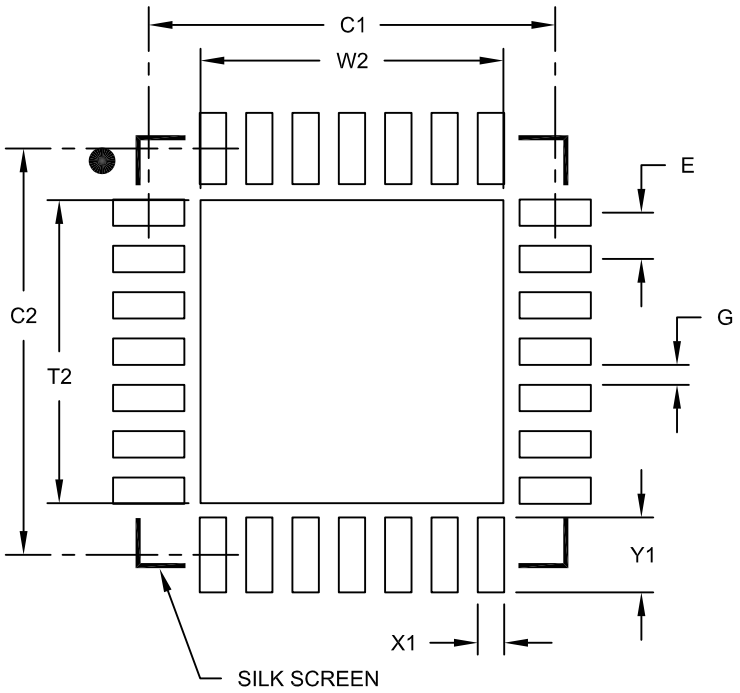
28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A