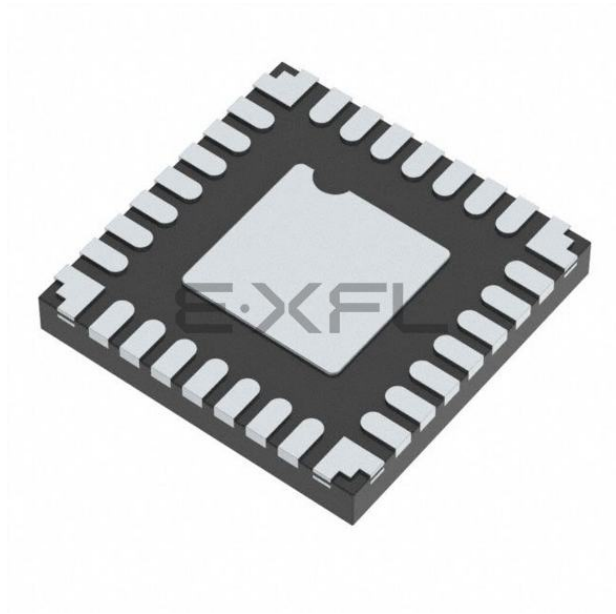
Microchip Technology - PIC32MM0032GPL028-E/M6 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl028-e-m6

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32® microAptiv™ UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32® microAptiv™ UC microprocessor core is the heart of the PIC32MM0064GPL036 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

3.1 Features

The PIC32MM0064GPL036 family processor core key features include:

- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
  - Multiply-add and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero and one detect instructions
  - `WAIT` instruction
  - Conditional move instructions
  - Vectored interrupts
  - Atomic interrupt enable/disable
  - One GPR shadow set to minimize latency of interrupts
  - Bit field manipulation instructions
- microMIPS™ Instruction Set:
  - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
  - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
  - Added seventeen new and thirty-five MIPS32® corresponding commonly used instructions in 16-bit opcode format.
  - Stack Pointer implicit in instruction.
  - MIPS32 assembly and ABI compatible.
- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
  - Configurable using high-performance multiplier array.
  - Maximum issue rate of one 32x16 multiply per clock.
  - Maximum issue rate of one 32x32 multiply every other clock.
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
  - No minimum frequency: 0 MHz.
  - Power-Down mode (triggered by `WAIT` instruction).
- EJTAG Debug/Profiling:
  - CPU control with start, stop and single stepping.
  - Software breakpoints via the `SDBBP` instruction.
  - Optional simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
  - PC and/or load/store address sampling for profiling.
  - Performance counters.
  - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0064GPL036 family processor core is shown in Figure 3-1.

REGISTER 5-1: NVMCON: NVM PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	r-0	U-0	U-0	U-0
	WR(1,4)	WREN(1)	WRERR(1,2)	LVDERR(1,2)	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	NVMOP<3:0>(3)			

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit(1,4)
This bit cannot be cleared and can be set only when WREN = 1, and the unlock sequence has been performed.
1 = Initiates a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)
1 = Enables writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disables writes to the WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1,2)
This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1,2)
This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low voltage is detected (possible data corruption if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **Reserved:** Maintain as '0'

bit 10-4 **Unimplemented:** Read as '0'

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.
2: These bits are cleared by setting NVMOP<3:0> = 0000 and initiating a Flash operation (i.e., WR).
3: NVMOP<3:0> bits are write-protected if the WREN bit is set.
4: Writes to the WR bit require an unlock sequence. Refer to **Section 5.1 "Flash Controller Registers Write Protection"** for details.

REGISTER 5-2: NVMKEY: NVM PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** NVM Unlock Register bits
These bits are write-only and read as '0' on any read.

REGISTER 5-3: NVMADDR: NVM FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** NVM Flash Address bits

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<10:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<7:0> are ignored).
Double-Word Program	Address identifies the double-word (64-bit) to program (NVMADDR<1:0> bits are ignored).

REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 3 **SLEEP:** Wake from Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake from Idle Flag bit(2)
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear bits in this register to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep mode.

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enables Software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 23.4 "System Registers Write Protection"** for details.
2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

REGISTER 8-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 8-1 for details). A value of '0' selects no divider.

bit 15 **ON:** Reference Oscillator Output Enable bit(1)
1 = Reference oscillator module is enabled
0 = Reference oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on the REFCLKO pin
0 = Reference clock is not driven out on the REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference oscillator module output continues to run in Sleep
0 = Reference oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 8-5: CLKSTAT: CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	SPDIVRDY	FRCRDY

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **SPLLRDY**: PLL Lock bit
1 = PLL is locked and ready
0 = PLL is not locked

bit 6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY:** LPRC Oscillator Ready bit
1 = LPRC oscillator is stable and ready
0 = LPRC oscillator is not stable

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready bit
1 = SOSC is stable and ready
0 = SOSC is not stable

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready bit
1 = POSC is stable and ready
0 = POSC is not stable

bit 1 **SPDIVRDY:** System PLL (with postscaler, SPLLDIV) Clock Ready Status bit
1 = SPLLDIV is stable and ready
0 = SPLLDIV is not stable

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready bit
1 = FRC oscillator is stable and ready
0 = FRC oscillator is not stable

TABLE 12-1: MCCP/SCCP REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	CCP1CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0110	CCP1CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0120	CCP1CON3	31:16	OETRIG	OSCNT<2:0>			—	OUTM<2:0>			—	—	POLACE	POLBDF	PSSACE<1:0>		PSSBDF<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	DT<5:0>						0000
0130	CCP1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0140	CCP1TMR	31:16	CCP1 TMRH<15:0>																0000
		15:0	CCP1 TMRL<15:0>																0000
0150	CCP1PR	31:16	CCP1 PRH<15:0>																0000
		15:0	CCP1 PRL<15:0>																0000
0160	CCP1RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0170	CCP1RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0180	CCP1BUF	31:16	CCP1 BUFH<15:0>																0000
		15:0	CCP1 BUFL<15:0>																0000
0200	CCP2CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0210	CCP2CON2	31:16	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0220	CCP2CON3	31:16	OETRIG	—	—	—	—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0230	CCP2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0240	CCP2TMR	31:16	CCP2 TMRH<15:0>																0000
		15:0	CCP2 TMRL<15:0>																0000
0250	CCP2PR	31:16	CCP2 PRH<15:0>																0000
		15:0	CCP2 PRL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL(1)	—	—	—	—	—	SPIFE	ENHBUF(1)
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO(4)	MODE32	MODE16	SMP	CKE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP(3)	MSTEN	DISSDI(4)	STXISEL<1:0>		SRXISEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
- 1 = Framed SPI support is enabled ($\overline{SSx}$ pin is used as the FSYNC1 input/output)
- 0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ Pin bit (Framed SPI mode only)
- 1 = Frame sync pulse input (Slave mode)
- 0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
- 1 = Frame pulse is active-high
- 0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
- 1 = Slave select SPI support is enabled; the $\overline{SSx}$ pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
- 0 = Slave select SPI support is disabled

bit 27 **FRMSYPW:** Frame Sync Pulse-Width bit
- 1 = Frame sync pulse is one character wide
- 0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits

Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
- 111 = Reserved
- 110 = Reserved
- 101 = Generates a frame sync pulse on every 32 data characters
- 100 = Generates a frame sync pulse on every 16 data characters
- 011 = Generates a frame sync pulse on every 8 data characters
- 010 = Generates a frame sync pulse on every 4 data characters
- 001 = Generates a frame sync pulse on every 2 data characters
- 000 = Generates a frame sync pulse on every data character

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 14-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MASK<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **MASK<7:0>:** UARTx Address Match Mask bits
Used to mask the ADDR<7:0> bits.
For MASK<x>:
1 = ADDR<x> is used to detect the address match
0 = ADDR<x> is not used to detect the address match

bit 23-16 **ADDR<7:0>:** UARTx Automatic Address Mask bits
When the ADDEN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** UARTx TX Interrupt Mode Selection bits
11 = Reserved, do not use
10 = Interrupt is generated and asserted while the transmit buffer is empty
01 = Interrupt is generated and asserted when all characters have been transmitted
00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** UARTx Transmit Polarity Inversion bit
If IrDA mode is Disabled (i.e., IREN (UxMODE<12>) is '0'):
1 = UxTX Idle state is '0'
0 = UxTX Idle state is '1'
If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
1 = IrDA® encoded UxTX Idle state is '1'
0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** UARTx Receiver Enable bit
1 = UARTx receiver is enabled, UxRX pin is controlled by UARTx (if ON = 1)
0 = UARTx receiver is disabled, UxRX pin is ignored by the UARTx module

bit 11 **UTXBRK:** UARTx Transmit Break bit
1 = Sends Break on next transmission; Start bit, followed by twelve '0' bits, followed by Stop bit, cleared by hardware upon completion
0 = Break transmission is disabled or has completed

bit 10 **UTXEN:** UARTx Transmit Enable bit
1 = UARTx transmitter is enabled, UxTX pin is controlled by UARTx (if ON = 1)
0 = UARTx transmitter is disabled, any pending transmission is aborted and the buffer is reset

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
1 = Transmit buffer is full
0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register (TSR) is Empty bit (read-only)
1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit Shift Register is not empty, a transmission is in progress or queued in the transmit buffer

15.1 RTCC Control Registers

TABLE 15-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	RTCCON1	31:16	ALRMEN	CHIME	—	—	AMASK<3:0>				ALMRPT<7:0>								0000
		15:0	ON	—	—	—	WRLOCK	—	—	—	RTCOE	OUTSEL<2:0>			—	—	—	—	0000
0010	RTCCON2	31:16	DIV<15:0>																0000
		15:0	FDIV<4:0>					—	—	—	—	—	—	—	—	—	CLKSEL<1:0>		0000
0030	RTCSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC	0000
0040	RTCTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0050	RTCDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000
0060	ALMTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0070	ALMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 18-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits

For CLC1:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART1 RX input
011 = SPI1 SDO output
010 = Comparator 2 output
001 = CLC1 output
000 = CLCINA I/O pin

For CLC2:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART2 RX input
011 = SPI2 SDO output
010 = Comparator 2 output
001 = CLC2 output
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits

For CLC1:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion (EOC) event
011 = UART1 TX output
010 = Comparator 1 output
001 = CLC2 output
000 = CLCINB I/O pin

For CLC2:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion event
011 = UART2 TX output
010 = Comparator 1 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits

111 = MCCP1 OCM1C output
110 = MCCP1 OCM1B output
101 = MCCP1 OCM1A output
100 = REFCLKO output
011 = LPRC clock source
010 = SOSC clock source
001 = System clock (FSYS)
000 = CLCINA I/O pin

REGISTER 23-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>				
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15 **FWDTEN:** Watchdog Timer Enable bit
1 = WDT is enabled
0 = WDT is disabled

bit 14-13 **RCLKSEL<1:0>:** Run Mode Watchdog Timer Clock Source Selection bits
11 = Clock source is the LPRC oscillator (same as for Sleep mode)
10 = Clock source is the FRC oscillator
01 = Reserved
00 = Clock source is the system clock

bit 12-8 **RWDTPS<4:0>:** Run Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Windowed mode is disabled
0 = Windowed mode is enabled

REGISTER 23-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	r-0	U-0	r-0	r-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EXECADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-y	U-0	r-1	r-1
	—	—	—	—	JTAGEN	—	—	—

Legend:	r = Reserved bit	y = Value set from Configuration bits on Reset
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **Reserved:** Must be written as '0'

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **Reserved:** Must be written as '0'

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits

11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)
•
•
•
00000010 = RAM program space starts at the 2-Kbyte boundary (from 0xA0000800)
00000001 = RAM program space starts at the 1-Kbyte boundary (from 0xA0000400)
00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit

1 = JTAG port is enabled
0 = JTAG port is disabled
The Reset value of this bit is the value of the JTAGEN (FICD<2>) Configuration bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Must be written as '1'

REGISTER 23-8: DEVID: DEVICE ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	VER<3:0>(1)				ID<27:24>(1)			
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<23:16>(1)							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<15:8>(1)							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

Note 1: Reset values are dependent on the device variant.

REGISTER 23-9: SYSKEY: SYSTEM UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SYSKEY<31:0>:** Unlock and Lock Key bits

24.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

24.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

24.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

24.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

24.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

24.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

24.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

NOTES:

TABLE 26-10: I/O PIN OUTPUT SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**				
DO10		I/O Ports	—	0.36	V	IOL = 6.0 mA, VDD = 3.6V
			—	0.21	V	IOL = 3.0 mA, VDD = 2V
DO16		RA3, RB8, RB9 and RB15 I/O Ports	—	0.16	V	IOL = 6.0 mA, VDD = 3.6V
			—	0.12	V	IOL = 3.0 mA, VDD = 2V
	VOH	**Output High Voltage**				
DO20		I/O Ports	3.25	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.4	—	V	IOH = -3.0 mA, VDD = 2V
DO26		RA3, RB8, RB9 and RB15 I/O Ports	3.3	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.55	—	V	IOH = -3.0 mA, VDD = 2V

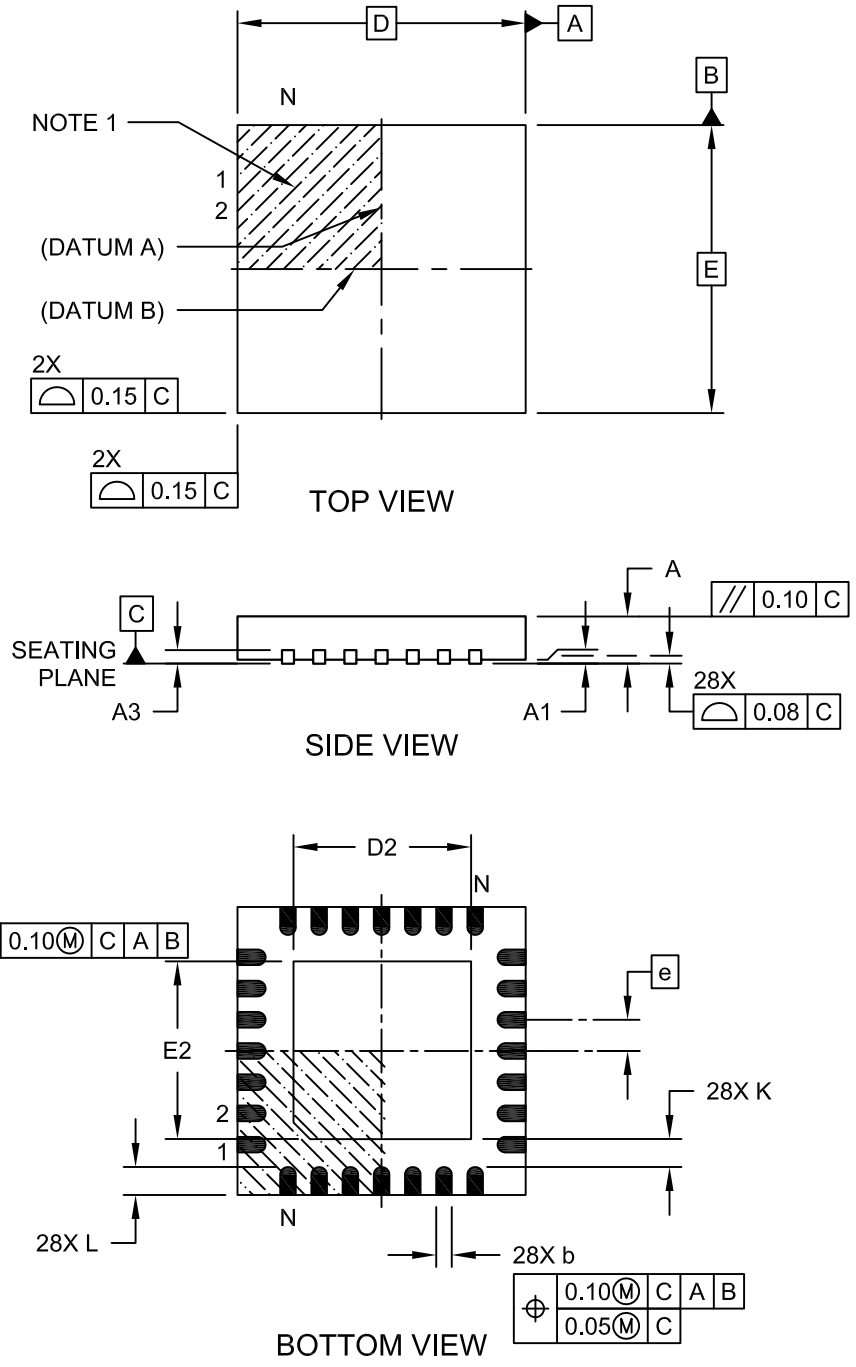
TABLE 26-11: PROGRAM FLASH MEMORY SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D130	EP	Cell Endurance	10000	20000	—	E/W	
D131	VICSP	VDD for In-Circuit Serial Programming™ (ICSP™)	VBOR	—	3.6	V	
D132	VRTSP	VDD for Run-Time Self-Programming (RTSP)	2.0	—	3.6	V	
D133	TIW	Self-Timed Double-Word Write Cycle Time	19.7	21.0	22.3	µs	8 bytes, data is not all ‘1’s
		Self-Timed Row Write Cycle Time	1.3	1.4	1.5	ms	256 bytes, data is not all ‘1’s, SYSCLK > 2 MHz
D133	TIE	Self-Timed Page Erase Time	15.0	16.0	17.0	ms	2048 bytes
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D136	TCE	Self-Timed Chip Erase Time	16.0	17.0	18.0	ms	

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

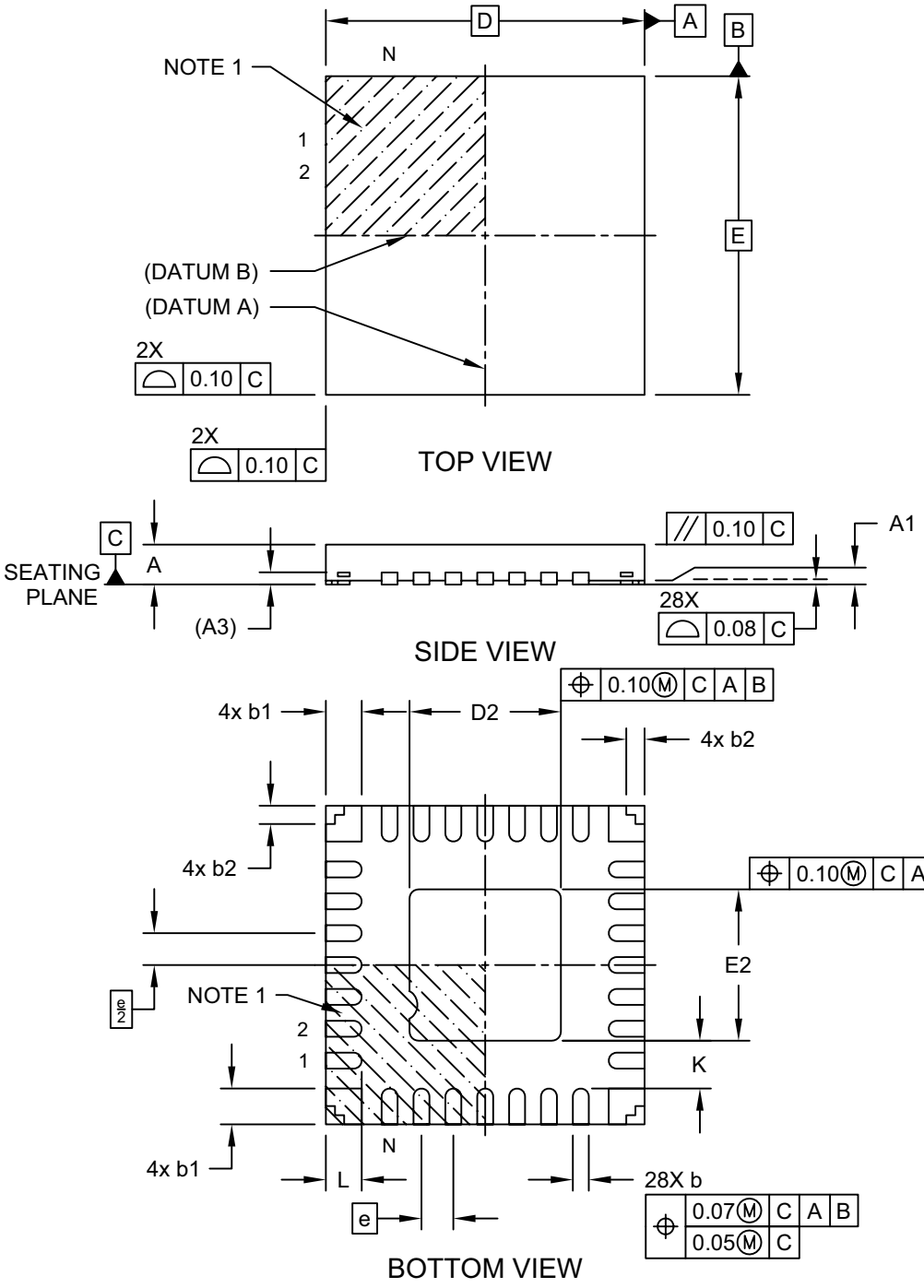
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-105C Sheet 1 of 2

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-333-M6 Rev B Sheet 1 of 2