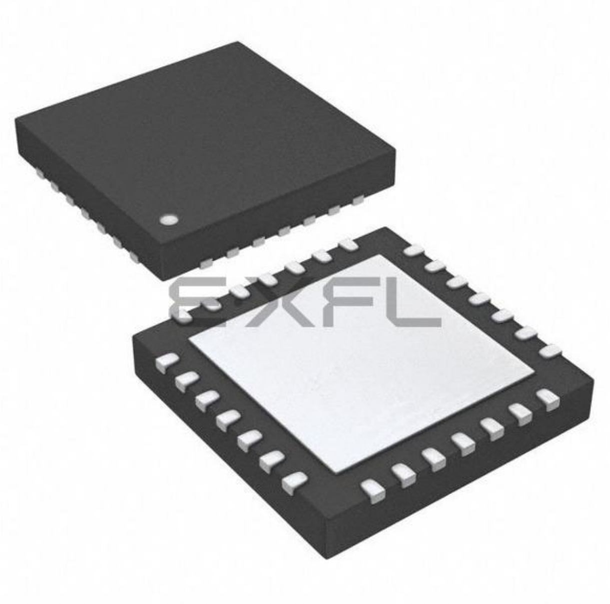


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

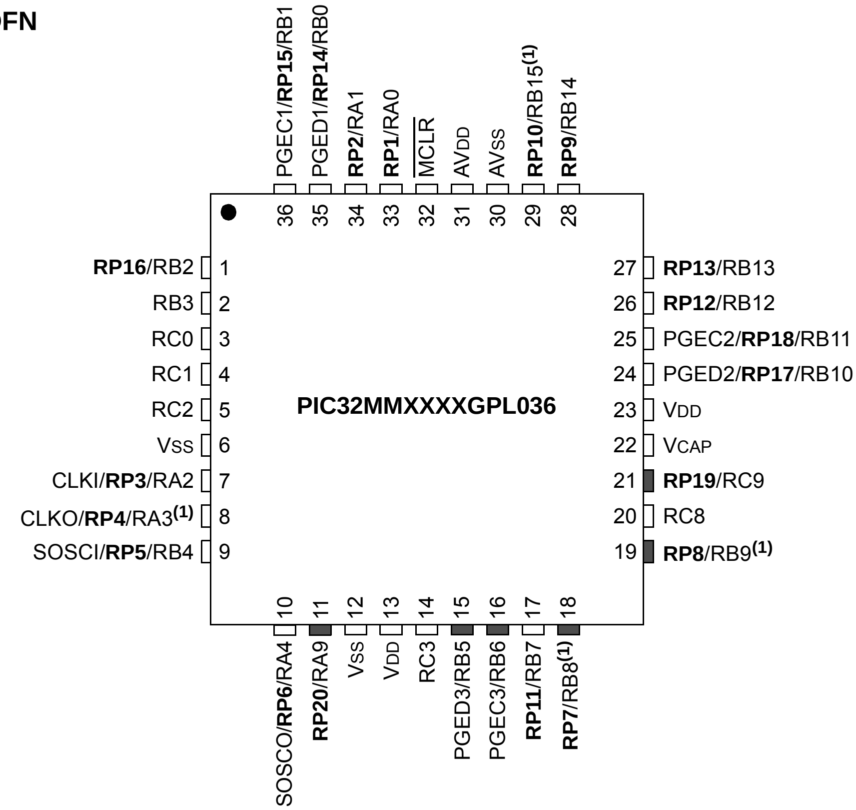
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl028-e-ml

Pin Diagrams (Continued)

36-Pin VQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN VQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP16**/RB2	19	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	AN11/C1INA/RB3	20	RC8
3	AN12/RC0	21	**RP19**/RC9
4	AN13/RC1	22	V_{CAP}
5	RC2	23	V_{DD}
6	V_{SS}	24	PGED2/TDO/**RP17**/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	PGEC2/TDI/**RP18**/RB11
8	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	26	AN7/LVDIN/**RP12**/RB12
9	SOSCI/**RP5**/RB4	27	AN8/**RP13**/RB13
10	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	28	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
11	**RP20**/RA9	29	AN10/REFCLKO/**RP10**/U1RX/$\overline{\text{SS1}}$/FSYNC1/INT0/RB15(1)
12	V_{SS}	30	AV_{SS}
13	V_{DD}	31	AV_{DD}
14	RC3	32	$\overline{\text{MCLR}}$
15	PGED3/RB5	33	V_{REF+}/AN0/**RP1**/OCM1E/INT3/RA0
16	PGEC3/RB6	34	V_{REF-}/AN1/**RP2**/OCM1F/RA1
17	**RP11**/RB7	35	PGED1/AN2/C1IND/C2INB/**RP14**/RB0
18	TCK/**RP7**/$\overline{\text{U1CTS}}$/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1

Note 1: Pin has an increased current drive strength.

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note:	This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0064GPL036 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pin (see **Section 2.4 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **Section 2.7 "External Oscillator Pins"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note:	The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

3.2 Architecture Overview

The MIPS32® microAptiv™ UC microprocessor core in the PIC32MM0064GPL036 family devices contains several logic blocks, working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Power Management
- microMIPS Instructions Decoder
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous Multiply/Divide Unit (MDU). The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid Stalls when executing instruction streams where data producing instructions are followed closely by consumers for their results
- Leading zero/one detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The microAptiv UC core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows the long-running MDU operations to be partially masked by system Stalls and/or other Integer Unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, Result/Accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the rs operand. The second number ('16' of 32x16) represents the rt operand. The microAptiv UC core only checks the value of the rt operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back, 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU. Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (rs) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit wide rs, 15 iterations are skipped, and for a 24-bit wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline Stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be re-issued), and latency (number of cycles until a result is available) for the microAptiv UC core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU`, `MADD/MADDU`, `MSUB/MSUBU`	16 bits	1	1
	32 bits	2	2
`MUL` (GPR destination)	16 bits	2	1
	32 bits	3	2
`DIV/DIVU`	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

REGISTER 5-2: NVMKEY: NVM PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** NVM Unlock Register bits
These bits are write-only and read as ‘0’ on any read.

REGISTER 5-3: NVMADDR: NVM FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** NVM Flash Address bits

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<10:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<7:0> are ignored).
Double-Word Program	Address identifies the double-word (64-bit) to program (NVMADDR<1:0> bits are ignored).

TABLE 7-3: INTERRUPT REGISTER MAP

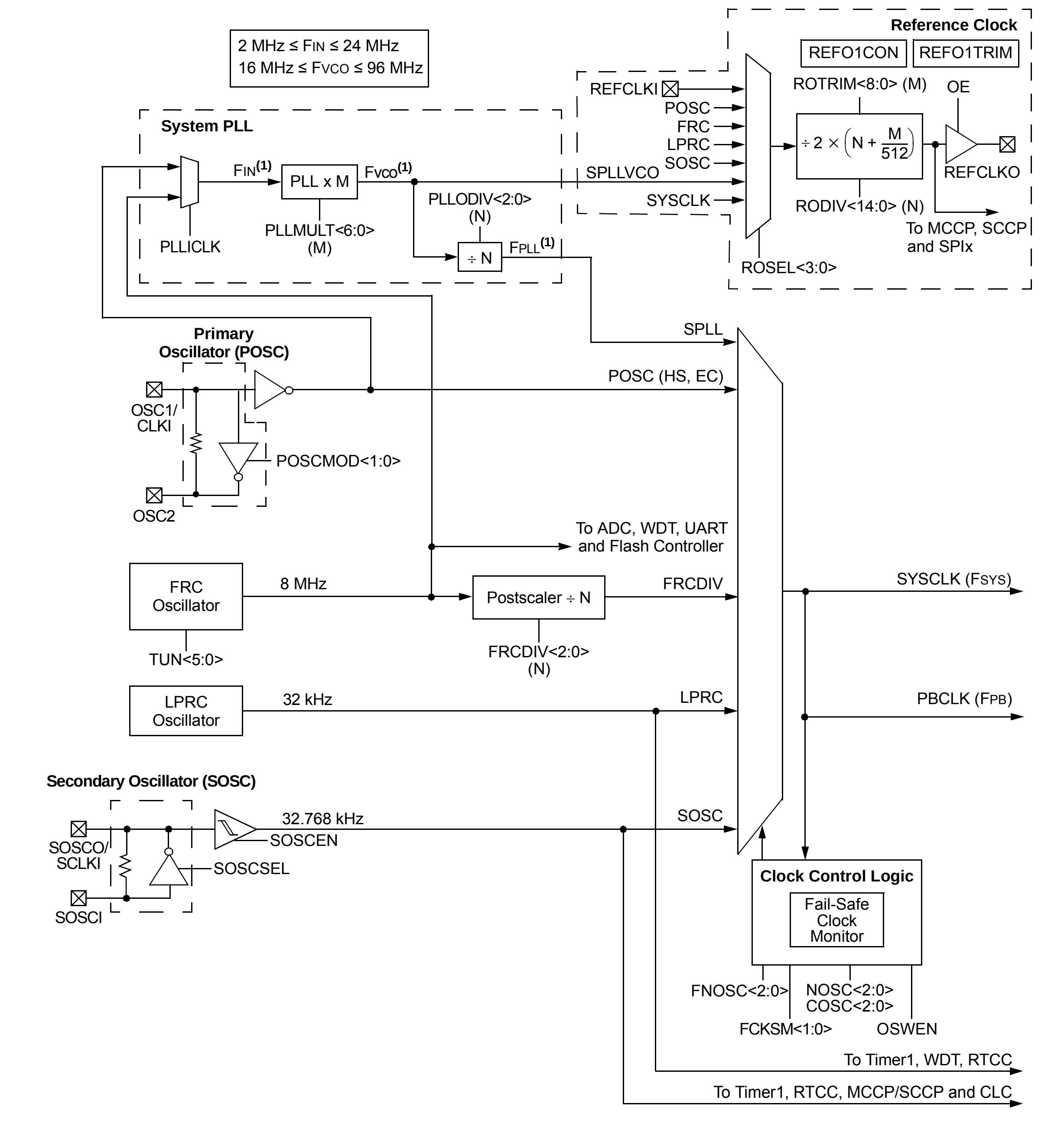
Virtual Address (BF80_#)	Register Name(1)	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F000	INTCON	31:16	—	—	—	—	—	—	—	—	—	VS<6:0>							0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
F010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
F020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
F030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
F040	IFS0	31:16	CCP2IF	CCT1IF	CCP1IF	—	—	—	U1EIF	U1TXIF	U1RXIF	SPI1RXIF	SPI1TXIF	SPI1EIF	CLC2IF	CLC1IF	LVDIF	CRCIF	0000
		15:0	AD1IF	RTCCIF	CMP2IF	CMP1IF	T1IF	CNCIF(2)	CNBIF	CNAIF	INT4IF	INT3IF	INT2IF	INT1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
F050	IFS1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CPCIF	NVMIF	—	—	—	U2EIF	U2TXIF	U2RXIF	SPI2RXIF	SPI2TXIF	SPI2EIF	—	—	CCT3IF	CCP3IF	CCT2IF	0000
F0C0	IEC0	31:16	CCP2IE	CCT1IE	CCP1IE	—	—	—	U1EIE	U1TXIE	U1RXIE	SPI1RXIE	SPI1TXIE	SPI1EIE	CLC2IE	CLC1IE	LVDIE	CRCIE	0000
		15:0	AD1IE	RTCCIE	CMP2IE	CMP1IE	T1IE	CNCIE(2)	CNBIE	CNAIE	INT4IE	INT3IE	INT2IE	INT1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
F0D0	IEC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CPCIE	NVMIE	—	—	—	U2EIE	U2TXIE	U2RXIE	SPI2RXIE	SPI2TXIE	SPI2EIE	—	—	CCT3IE	CCP3IE	CCT2IE	0000
F140	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
F150	IPC1	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
F160	IPC2	31:16	—	—	—	T1IP<2:0>			T1IS<1:0>		—	—	—	CNCIP<2:0>(2)			CNCIS<1:0>(2)		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
F170	IPC3	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
F180	IPC4	31:16	—	—	—	CLC2IP<2:0>			CLC2IS<1:0>		—	—	—	CLC1IP<2:0>			CLC1IS<1:0>		0000
		15:0	—	—	—	LVDIP<2:0>			LVDIS<1:0>		—	—	—	CRCIP<2:0>			CRCIS<1:0>		0000
F190	IPC5	31:16	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
		15:0	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		0000
F1A0	IPC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	U1EIP<2:0>			U1EIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
F1B0	IPC7	31:16				CCP2IP<2:0>			CCP2IS<1:0>		—	—	—	CCT1IP<2:0>			CCT1IS<1:0>		0000
		15:0	—	—	—	CCP1IP<2:0>			CCP1IS<1:0>		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 20-pin devices.

FIGURE 8-1: PIC32MM0064GPL036 FAMILY OSCILLATOR DIAGRAM



Note 1: Refer to Table 26-18 in **Section 26.0 "Electrical Characteristics"** for frequency limitations.

TABLE 9-6: PORTC REGISTER MAP

Virtual Address (BF80_#)	Register Name[3]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2800	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC<1:0>[1,2]		0003
2810	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISC<9:8>[1,2]		—	—	—	—	TRISC<3:0>[1,2]				030F
2820	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RC<9:8>[1,2]		—	—	—	—	RC<3:0>[1,2]				0000
2830	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATC<9:8>[1,2]		—	—	—	—	LATC<3:0>[1,2]				0000
2840	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCC<9:8>[1,2]		—	—	—	—	ODCC<3:0>[1,2]				0000
2850	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUC<9:8>[1,2]		—	—	—	—	CNPUC<3:0>[1,2]				0000
2860	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDC<9:8>[1,2]		—	—	—	—	CNPDC<3:0>[1,2]				0000
2870	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON[1]	—	—	—	CNSTYLE[1]	—	—	—	—	—	—	—	—	—	—	—	0000
2880	CNEN0C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIE0C<9:8>[1,2]		—	—	—	—	CNIE0C<3:0>[1,2]				0000
2890	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNSTATC<9:8>[1,2]		—	—	—	—	CNSTATC<3:0>[1,2]				0000
28A0	CNEN1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIE1C<9:8>[1,2]		—	—	—	—	CNIE1C<3:0>[1,2]				0000
28B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFC<9:8>[1,2]		—	—	—	—	CNFC<3:0>[1,2]				0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.
Note 1: Bits<15,11,9:8,3:0> are not implemented in 20-pin devices.
2: Bits<8,3:0> are not implemented in 28-pin devices.
3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL(1)	—	—	—	—	—	SPIFE	ENHBUF(1)
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO(4)	MODE32	MODE16	SMP	CKE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP(3)	MSTEN	DISSDI(4)	STXISEL<1:0>		SRXISEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{\text{SSx}}$ pin is used as the FSYNC1 input/output)
0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{\text{SSx}}$ Pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support is enabled; the $\overline{\text{SSx}}$ pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
0 = Slave select SPI support is disabled

bit 27 **FRMSYPW:** Frame Sync Pulse-Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits
Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
111 = Reserved
110 = Reserved
101 = Generates a frame sync pulse on every 32 data characters
100 = Generates a frame sync pulse on every 16 data characters
011 = Generates a frame sync pulse on every 8 data characters
010 = Generates a frame sync pulse on every 4 data characters
001 = Generates a frame sync pulse on every 2 data characters
000 = Generates a frame sync pulse on every data character

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.
2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
3: When AUDEN = 1, the SPI/I^{2}S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 15-5: RTCDATE: RTCC DATE REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	YRTEN<3:0>				YRONE<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YRTEN<3:0>:** Binary Coded Decimal Value of Years 10-Digit bits

bit 27-24 **YRONE<3:0>:** Binary Coded Decimal Value of Years 1-Digit bits

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

17.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

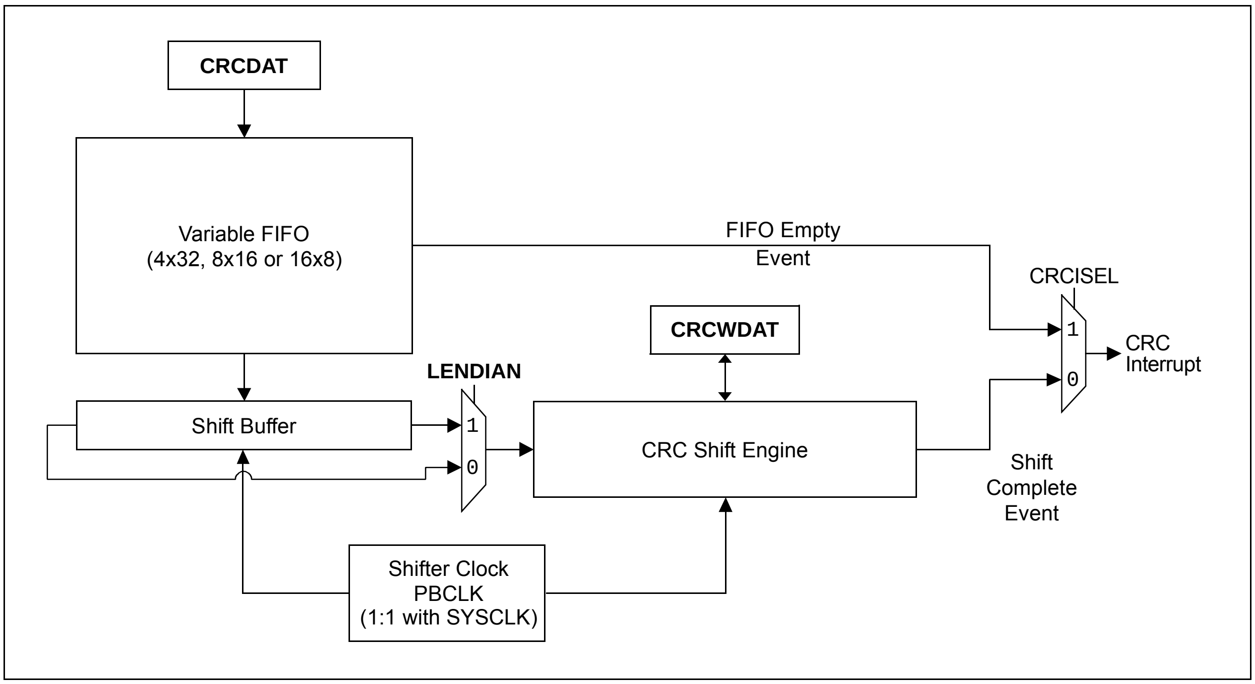
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 60. "32-Bit Programmable Cyclic Redundancy Check"** (DS60001336) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 17-1 displays a simplified block diagram of the CRC generator.

FIGURE 17-1: CRC BLOCK DIAGRAM



22.0 POWER-SAVING FEATURES

> **Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Modes"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes power-saving features for the PIC32MM0064GPL036 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

22.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted, and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a `WAIT` instruction is executed.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- If WDT is enabled, the Run mode counter is not cleared upon entry to Sleep and the Sleep mode counter is reset upon entering Sleep.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC and Timer1).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The on-chip regulator enters Standby mode if the VREGS bit (PWRCON<0>) is set.
- A separate special low-power, low-voltage/retention regulator is activated if the RETVR Configuration bit (FPOR<2>) is programmed to zero and the RETEN bit (PWRCON<1>) is set.

The processor will exit, or "wake-up", from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than, or equal to, the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

22.2 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than, or equal to, the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

22.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not take effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to ‘1’. To enable a peripheral, the associated PMDx bit must be cleared (default).

To prevent accidental configuration changes under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK bit in PMDCON register (PMDCON<11>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes. To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 23.4 “System Registers Write Protection”** for details.

Table 22-1 lists the module disable bits and locations for all modules.

TABLE 22-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name	Register Name and Bit Location
Analog-to-Digital Converter (ADC)	ADCMD	PMD1<0>
Voltage Reference (VR)	VREFMD	PMD1<12>
High/Low-Voltage Detect (HLVD)	HLVDMD	PMD1<20>
Comparator 1 (CMP1)	CMP1MD	PMD2<0>
Comparator 2 (CMP2)	CMP2MD	PMD2<1>
Configurable Logic Cell 1 (CLC1)	CLC1MD	PMD2<24>
Configurable Logic Cell 2 (CLC2)	CLC2MD	PMD2<25>
Multiple Outputs Capture/Compare/PWM/ Timer1 (MCCP1)	CCP1MD	PMD3<8>
Single Output Capture/Compare/PWM/Timer2 (SCCP2)	CCP2MD	PMD3<9>
Single Output Capture/Compare/PWM/Timer3 (SCCP3)	CCP3MD	PMD3<10>
Timer1 (TMR1)	T1MD	PMD4<0>
Universal Asynchronous Receiver Transmitter 1 (UART1)	U1MD	PMD5<0>
Universal Asynchronous Receiver Transmitter 2 (UART2)	U2MD	PMD5<1>
Serial Peripheral Interface 1 (SPI1)	SPI1MD	PMD5<8>
Serial Peripheral Interface 2 (SPI2)	SPI2MD	PMD5<9>
Real-Time Clock and Calendar (RTCC)	RTCCMD	PMD6<0>
Reference Clock Output (REFCLKO)	REFOMD	PMD6<8>
Programmable Cyclic Redundancy Check (CRC)	CRCMD	PMD7<3>

23.0 SPECIAL FEATURES

Note:	This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. “Programming and Diagnostics”** (DS61129) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

23.1 Configuration Bits

PIC32MM0064GPL036 family devices contain a Boot Flash Memory (BFM) with an associated configuration space. All Configuration Words are listed in Table 23-3 and Table 23-4; Register 23-1 through Register 23-6 describe the configuration options.

23.2 Code Execution from RAM

PIC32MM0064GPL036 family devices allow executing the code from RAM. The starting boundary of this special RAM space can be adjusted using the EXECADDR<7:0> bits in the CFGCON register with a 1-Kbyte step. Writing a non-zero value to these bits will move the boundary, effectively reducing the total amount of program memory space in RAM. Refer to Table 23-5 and Register 23-7 for more information.

23.3 Device ID

The Device ID identifies the device used. The ID can be read from the DEVID register. The Device IDs for PIC32MM0064GPL036 family devices are listed in Table 23-1. Also refer to Table 23-5 and Register 23-8 for more information.

TABLE 23-1: DEVICE IDs FOR PIC32MM0064GPL036 FAMILY DEVICES

Device	DEVID
PIC32MM0016GPL020	0x06B04053
PIC32MM0032GPL020	0x06B0C053
PIC32MM0064GPL020	0x06B14053
PIC32MM0016GPL028	0x06B02053
PIC32MM0032GPL028	0x06B0A053
PIC32MM0064GPL028	0x06B12053
PIC32MM0016GPL036	0x06B06053
PIC32MM0032GPL036	0x06B0E053
PIC32MM0064GPL036	0x06B16053

23.4 System Registers Write Protection

The critical registers in the PIC32MM0064GPL036 family devices are protected (locked) from an accidental write. If the registers are locked, a special unlock sequence is required to modify the content of these registers.

To unlock the registers, the following steps should be done:

1. Disable interrupts prior to the system unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the SYSKEY register, in two back-to-back assembly or ‘C’ instructions.
3. Write the new value to the required register.
4. Write a non-key value (such as 0x00000000) to the SYSKEY register to perform a lock.
5. Re-enable interrupts.

The registers that require this unlocking sequence are listed in Table 23-2.

TABLE 23-2: SYSTEM LOCKED REGISTERS

Register Name	Register Description	Peripheral
OSCCON	Oscillator Control	Oscillator
SPLLCON	System PLL Control	Oscillator
OSCTUN	FRC Tuning	Oscillator
PMDCON	Peripheral Module Disable Control	PMD
RSWRST	Software Reset	Reset
RPCON	Peripheral Pin Select Configuration	I/O Ports
RNMICON	Non-Maskable Interrupt Control	Reset
PWRCON	Power Control	Reset
RTCCON1	RTCC Control 1	RTCC

The SYSKEY register read value indicates the status. A value of ‘0’ indicates the system registers are locked. A value of ‘1’ indicates the system registers are unlocked. For more information about the SYSKEY register, refer to Table 23-5 and Register 23-9.

23.9 Configuration Words and System Registers

TABLE 23-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits 31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
17D4	FOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

24.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

24.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 26-14: COMPARATOR SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
D300	VIOFF	Input Offset Voltage	-20	—	20	mV
D301	VICM	Input Common-Mode Voltage	AVSS – 0.3V	—	AVDD + 0.3V	V
D307	TRESP(1)	Response Time	—	150	—	ns

Note 1: Measured with one input at VDD/2 and the other transitioning from VSS to VDD.
2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

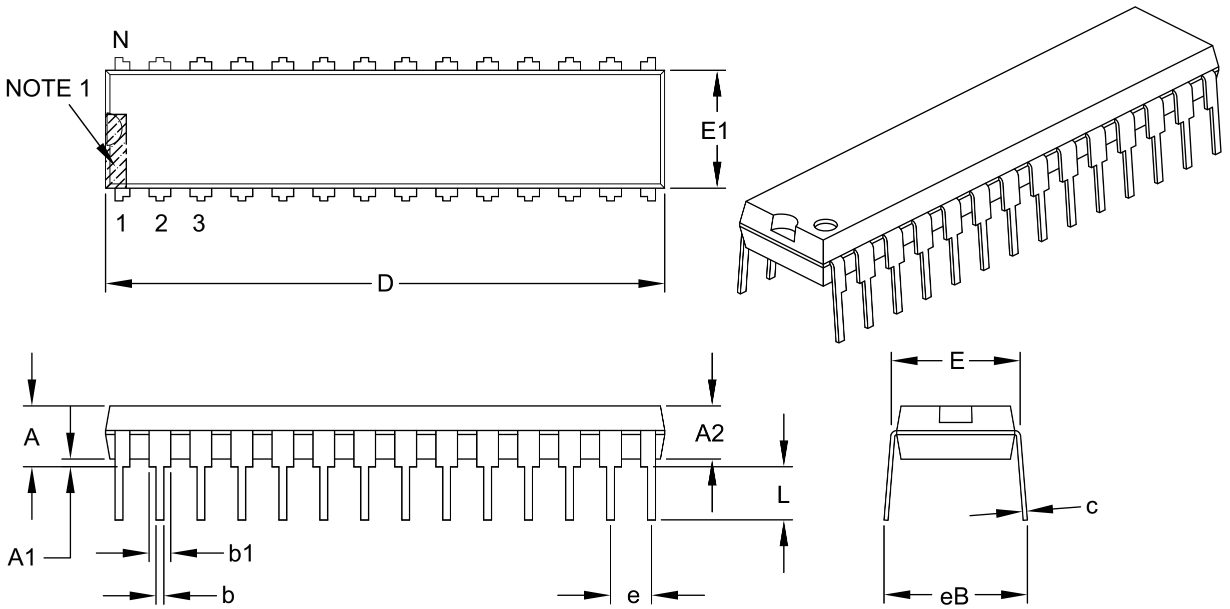
TABLE 26-15: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
VRD310	TSET	Settling Time(1)	—	—	10	μs
VRD311	VRA	Accuracy	-1	—	1	LSb
VRD312	VRUR	Unit Resistor Value (R)	—	4.5	—	kΩ

Note 1: Measures the interval while VRDAT<4:0> transitions from ‘11111’ to ‘00000’.
2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

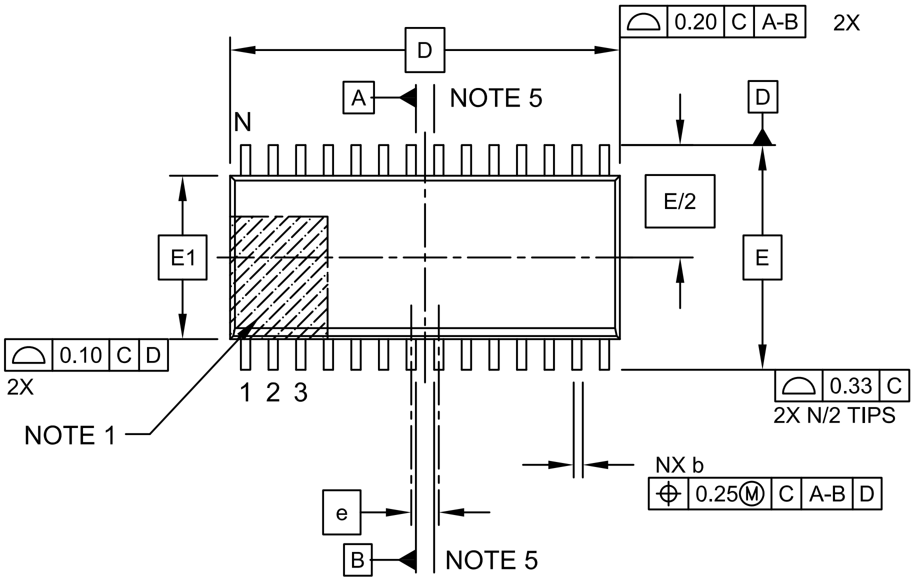
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

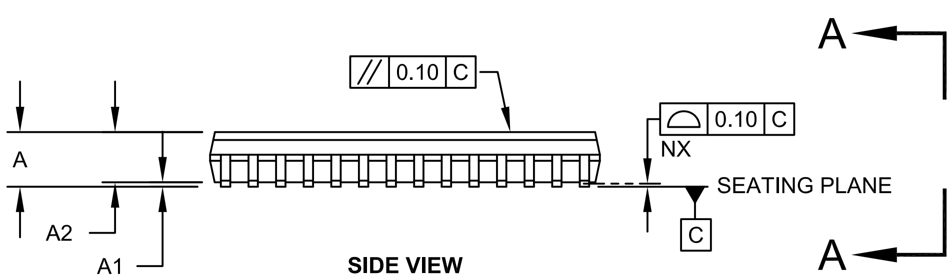
Microchip Technology Drawing C04-070B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

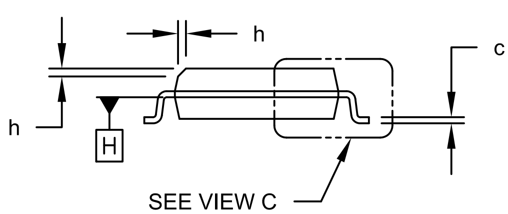
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

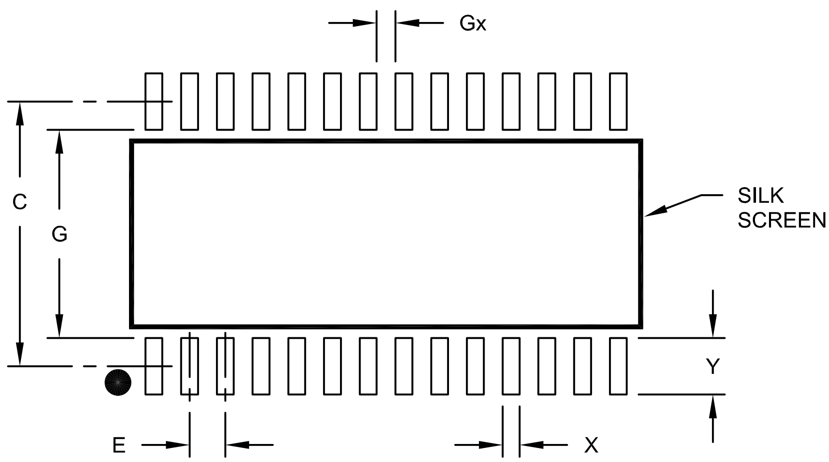


VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

APPENDIX A: REVISION HISTORY

Revision A (February 2015)

This is the initial version of the document.

Revision B (May 2016)

This revision incorporates the following updates:

- Registers:
  - Updates Register 5-1, Register 5-3, Register 5-6, Register 5-7, Register 6-3, Register 6-4, Register 7-2, Register 8-2, Register 8-3, Register 8-5, Register 8-6, Register 11-1, Register 13-1, Register 14-1, Register 15-1, Register 15-5, Register 15-6, Register 16-1, Register 16-2, Register 16-3, Register 16-5, Register 18-2, Register 19-1, Register 19-2 and Register 23-7
- Tables:
  - Updates Table 1-1, Table 5-1, Table 6-1,Table 7-2, Table 7-3, Table 9-3, Table 9-7, Table 15-1, Table 16-1, Table 19-1, Table 22-1, Table 23-4, Table 23-5 Table 26-2, Table 26-3, Table 26-4 and Table 26-6 through Table 26-33
  - Adds Table 23-8
- Figures:
  - Updates Figure 1-1, Figure 3-1, Figure 8-1, Figure 10-1, Figure 14-1, Figure 13-1, Figure 14-1, Figure 14-1, Figure 15-1, Figure 17-1, Figure 18-1, Figure 18-3, Figure 26-1, Figure 26-3, Figure 26-4, Figure 26-9, Figure 26-10, Figure 26-11 and Figure 26-12
- Updates pin function descriptions in **Section 1.0 “Device Overview”**
- Updates text in **Section 9.6 “Input Change Notification (ICN)”**, **Section 9.8.4 “Input Mapping”**, **Section 23.7 “Unique Device Identifier (UDID)”**, **Section 22.5 “Low-Power Brown-out Reset”** and **Section 27.0 “Packaging Information”**
- Adds **Section 5.1 “Flash Controller Registers Write Protection”**, **Section 8.0 “Oscillator Configuration”**, **Section 23.4 “System Registers Write Protection”**, reference to **Section 22.1 “Sleep Mode”**, **Section 22.2 “Idle Mode”** and **Section 23.8 “Reserved Registers”**
- Updates the Absolute Maximum Ratings in **Section 26.0 “Electrical Characteristics”**

This revision also includes minor typographical and formatting changes throughout the data sheet text.