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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I ² S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl028-e-ss

PIC32MM0064GPL036 FAMILY

Pin Diagrams (Continued)

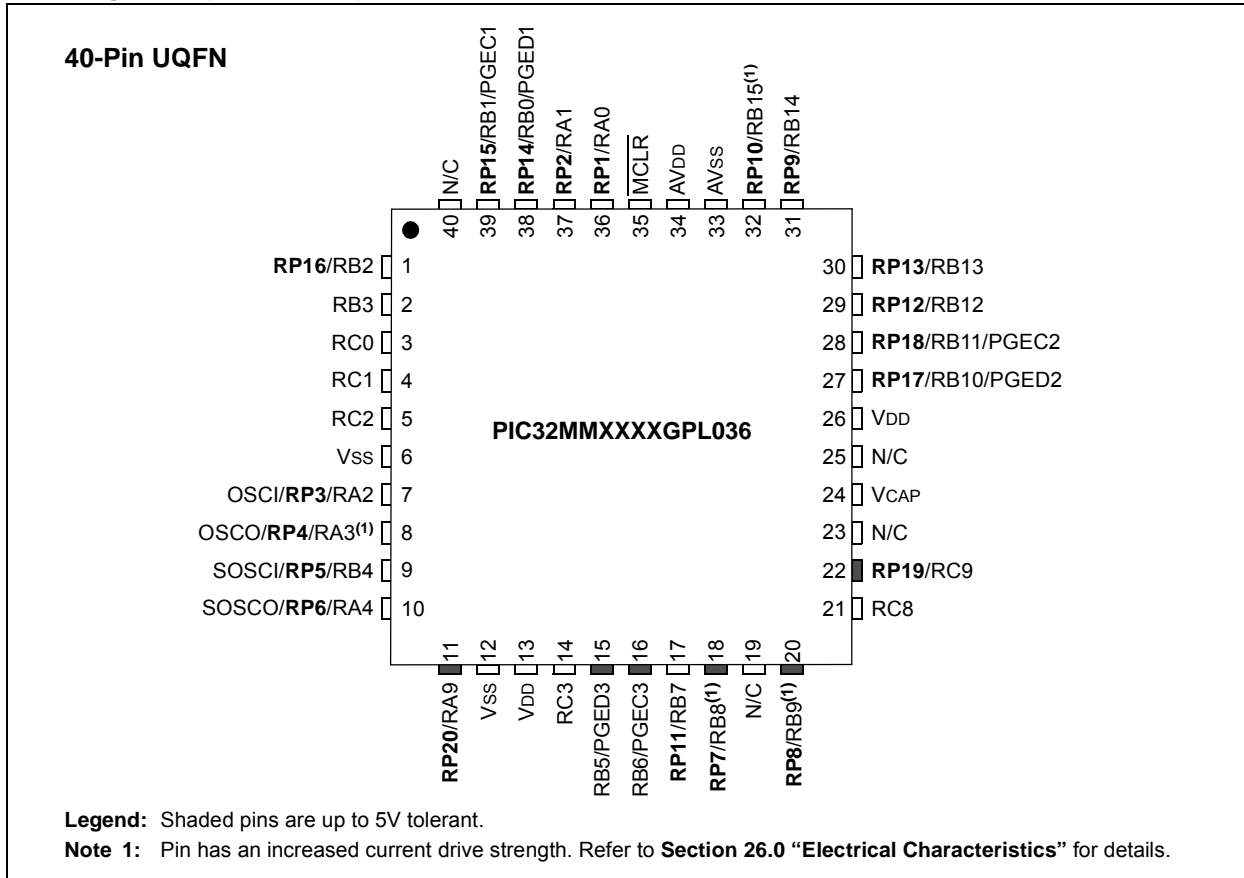


TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/RP16/RB2	21	RC8
2	AN11/C1INA/RB3	22	RP19/RC9
3	AN12/RC0	23	N/C
4	AN13/RC1	24	VCAP
5	RC2	25	N/C
6	Vss	26	VDD
7	OSC1/CLKI/AN5/RP3/OCM1C/RA2	27	PGED2/TDO/RP17/RB10
8	OSC2/CLKO/AN6/RP4/OCM1D/RA3 ⁽¹⁾	28	PGEC2/TDI/RP18/RB11
9	SOSCI/RP5/RB4	29	AN7/LVDIN/RP12/RB12
10	SOSCO/SCLKI/RP6/PWRLCLK/RA4	30	AN8/RP13/RB13
11	RP20/RA9	31	CDAC1/AN9/RP9/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
12	Vss	32	AN10/REFCLKO/RP10/U1RX/SS1/FSYNC1/INT0/RB15 ⁽¹⁾
13	VDD	33	AVss
14	RC3	34	AVDD
15	PGED3/RB5	35	MCLR
16	PGEC3/RB6	36	VREF+/AN0/RP1/OCM1E/INT3/RA0
17	RP11/RB7	37	VREF-/AN1/RP2/OCM1F/RA1
18	TCK/RP7/U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾	38	PGED1/AN2/C1IND/C2INB/RP14/RB0
19	N/C	39	PGEC1/AN3/C1INC/C2INA/RP15/RB1
20	TMS/REFCLKI/RP8/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9 ⁽¹⁾	40	N/C

Note 1: Pin has an increased current drive strength.

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NOTES:

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REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit

1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit

0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit

0 = No MIPS16e[®] are present

bit 1 **EP:** EJTAG Present bit

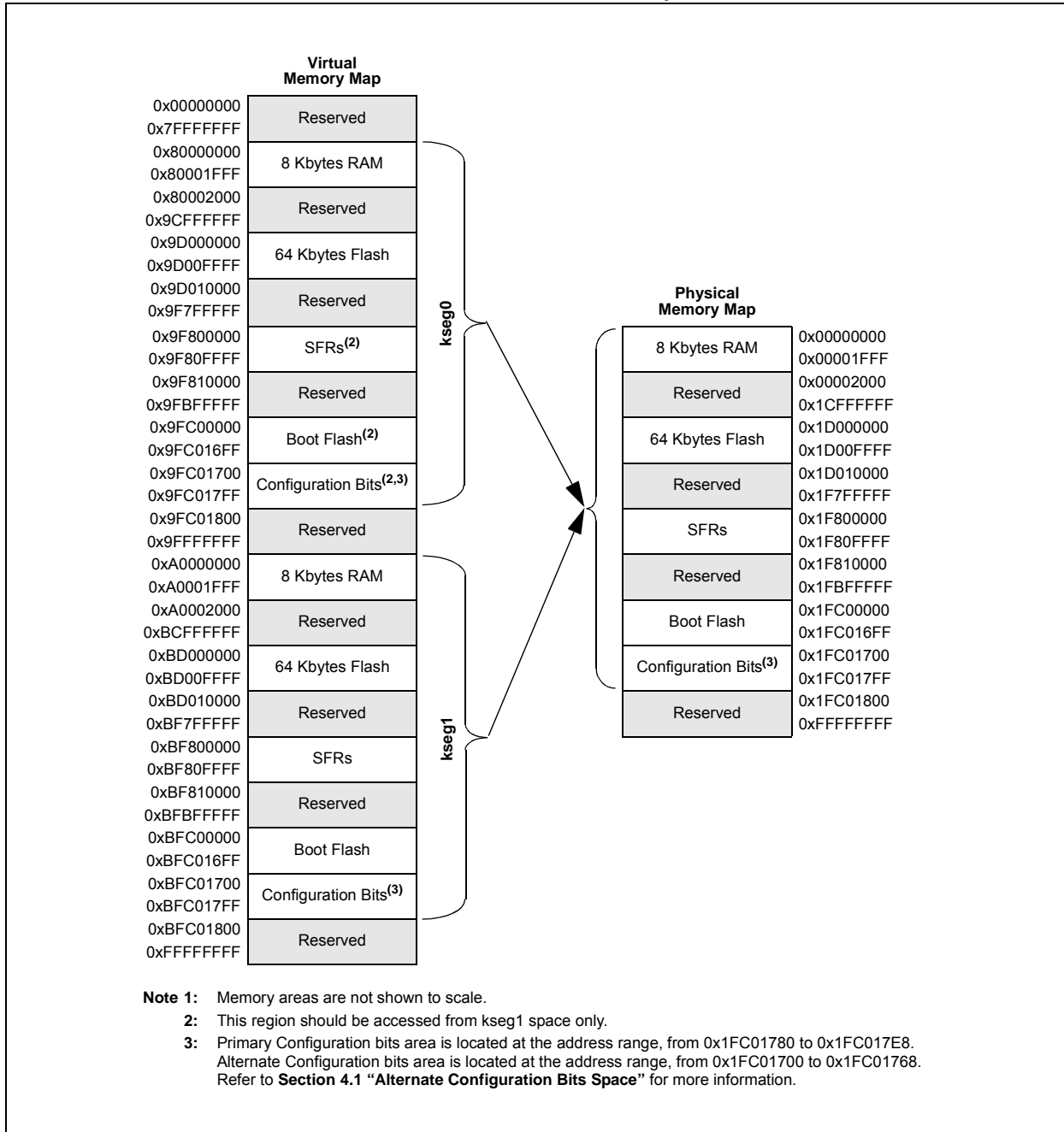
1 = Core implements EJTAG

bit 0 **FP:** Floating-Point Unit bit

0 = Floating-Point Unit is not implemented

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FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 64 Kbytes OF PROGRAM MEMORY⁽¹⁾



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REGISTER 5-7: NVMBWP: NVM BOOT FLASH (PAGE) WRITE-PROTECT REGISTER⁽¹⁾

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
	BWPULOCK	—	—	—	—	BWP2 ⁽²⁾	BWP1 ⁽²⁾	BWP0 ⁽²⁾
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BWPULOCK:** Boot Alias Write-Protect Unlock bit
 1 = BWPx bits are not locked and can be modified
 0 = BWPx bits are locked and cannot be modified
 This bit is only clearable and cannot be set except by any Reset.

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **BWP2:** Boot Alias Page 2 Write-Protect bit⁽²⁾
 1 = Write protection for physical address, 0x1FC00000 through 0x1FC007FF, is enabled
 0 = Write protection for physical address, 0x1FC00000 through 0x1FC007FF, is disabled

bit 9 **BWP1:** Boot Alias Page 1 Write-Protect bit⁽²⁾
 1 = Write protection for physical address, 0x1FC00800 through 0x1FC00FFF, is enabled
 0 = Write protection for physical address, 0x1FC00800 through 0x1FC00FFF, is disabled

bit 8 **BWP0:** Boot Alias Page 0 Write-Protect bit⁽²⁾
 1 = Write protection for physical address, 0x1FC01000 through 0x1FC017FF, is enabled
 0 = Write protection for physical address, 0x1FC01000 through 0x1FC017FF, is disabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an NVMKEY unlock sequence. Refer to **Section 5.1 “Flash Controller Registers Write Protection”** for details.

2: These bits can be modified only when the associated unlock bit (BWPULOCK) is set.

7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. “Interrupts”** (DS60001108) and **Section 50. “CPU for Devices with MIPS32® microAptiv™ and M-Class Cores”** (DS60001192) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM

PIC32MM0064GPL036 family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

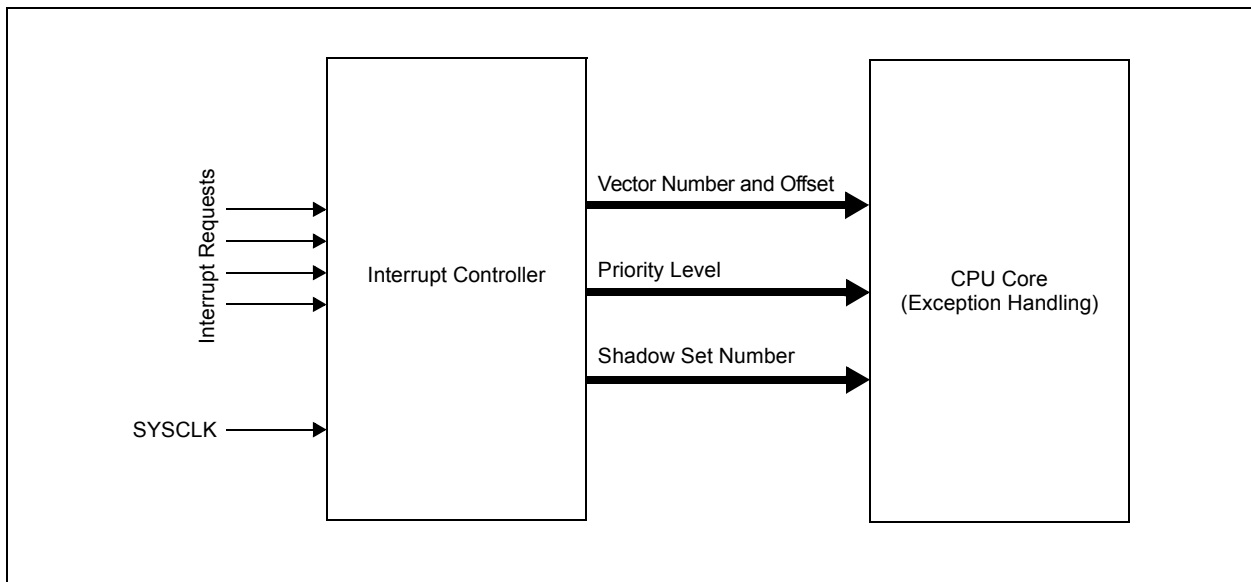
The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 “CPU Exceptions”**.

The PIC32MM0064GPL036 family device interrupt module includes the following features:

- Single Vector or Multivector mode Operation
- Five External Interrupts with Edge Polarity Control
- Interrupt Proximity Timer
- Module Freeze in Debug mode
- Seven User-Selectable Priority Levels for each Vector
- Four User-Selectable Subpriority Levels within each Priority
- One Shadow Register Set that can be used for any Priority Level, Eliminating Software Context Switching and Reducing Interrupt Latency
- Software can Generate any Interrupt
- User-Configurable Interrupt Vectors’ Offset and Vector Table Location

Figure 7-1 shows the block diagram for the interrupt controller and CPU exceptions.

FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



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9.1 CLR, SET and INV Registers

Every I/O module register has a corresponding CLR (Clear), SET (Set) and INV (Invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the effects of a write operation to a SET, CLR or INV register, the base register must be read.

9.2 Parallel I/O (PIO) Ports

All port pins have 14 registers directly associated with their operation as digital I/Os. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. The LATx register controls the pin level when it is configured as an output. Reads from the PORTx register read the port pins, while writes to the port pins write the latch, LATx. The I/Os state reflected in the PORTx register is synchronized with the system clock and delayed by 3 system clock cycles.

9.3 Open-Drain Configuration

In addition to the PORTx, LATx and TRISx registers for data control, the port pins can also be individually configured for either digital or open-drain outputs. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V), on any desired 5V tolerant pins, by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

9.4 Configuring Analog and Digital Port Pins

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications. The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as timers, UARTs, etc., the corresponding ANSELx bit must be cleared. The ANSELx register has a default value of 0xFFFF. Therefore, all pins that share analog functions are analog (not digital) by default. If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is used by an analog peripheral, such as the ADC or comparator module.

9.5 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

9.6 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows the PIC32MM devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State. Five control registers are associated with the Change Notification (CN) functionality of each I/O port. To enable the Change Notification feature for the port, the ON bit (CNCONx<15>) must be set.

The CNEN0x and CNEN1x registers contain the CN interrupt enable control bits for each of the input pins. The setting of these bits enables a CN interrupt for the corresponding pins. Also, these bits, in combination with the CNSTYLE bit (CNCONx<11>), define a type of transition when the interrupt is generated. Possible CN event options are listed in Table 9-1.

TABLE 9-1: CHANGE NOTIFICATION EVENT OPTIONS

CNSTYLE Bit (CNCONx<11>)	CNEN1x Bit	CNEN0x Bit	Change Notification Event Description
0	Does not matter	0	Disabled
0	Does not matter	1	Detects a mismatch between the last read state and the current state of the pin
1	0	0	Disabled
1	0	1	Detects a positive transition only (from '0' to '1')
1	1	0	Detects a negative transition only (from '1' to '0')
1	1	1	Detects both positive and negative transitions

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit. In addition to the CNSTATx register, the CNFxx register is implemented for each port. This register contains flags for Change Notification events. These flags are set if the valid transition edge, selected in the CNEN0x and CNEN1x registers, is detected. CNFxx stores the occurrence of the event. CNFxx bits must be cleared in software to get the next Change Notification interrupt. The CN interrupt is generated only for the I/Os configured as inputs (corresponding TRISx bits must be set).

12.0 CAPTURE/COMPARE/PWM/TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 30. “Capture/Compare/PWM/Timer (MCCP and SCCP)”** (DS60001381) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

12.1 Introduction

PIC32MM0064GPL036 family devices include three Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 32-bit microcontrollers. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all earlier PIC32 devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single Capture/Compare/PWM/Timer (SCCPs) output modules provide only one PWM output. Multiple Capture/Compare/PWM/Timer (MCCPs) output modules can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features:

- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for module Interrupt Events or Triggers
- Synchronization Output Signal for Coordinating other MCCP/SCCP modules with User-Configurable Alternate and Auxiliary Source Options

- Fully Asynchronous Operation in all modes and in Low-Power Operation
- Special Output Trigger for ADC Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture modes:
 - Backward compatible with previous input capture peripherals of the PIC32 family
 - 16-bit or 32-bit capture of time base on external event
 - Up to four-level deep FIFO capture buffer
 - Capture source input multiplexer
 - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
 - Backward compatible with previous output compare peripherals of the PIC32 family
 - Single Edge and Dual Edge Compare modes
 - Center-Aligned Compare mode
 - Variable Frequency Pulse mode
 - External Input mode

MCCP modules also include these extended PWM features:

- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can be operated in only one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in Figure 12-1. All three modes use the time base generator and the common Timer register pair (CCPxTMR). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

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REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

- bit 7-6 **TMRPS<1:0>**: CCPx Time Base Prescale Select bits
11 = 1:64 prescaler
10 = 1:16 prescaler
01 = 1:4 prescaler
00 = 1:1 prescaler
- bit 5 **T32**: 32-Bit Time Base Select bit
1 = 32-bit time base for timer, single edge output compare or input capture function
0 = 16-bit time base for timer, single edge output compare or input capture function
- bit 4 **CCSEL**: Capture/Compare Mode Select bit
1 = Input Capture mode
0 = Output Compare/PWM or Timer mode (exact function is selected by the MOD<3:0> bits)
- bit 3-0 **MOD<3:0>**: CCPx Mode Select bits
CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)
CCSEL = 0 (Output Compare modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode
0110 = Center-Aligned Pulse Compare mode, buffered
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode: Toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode: Drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode: Drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode: Output functions are disabled

- Note 1:** This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

PIC32MM0064GPL036 FAMILY

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL ⁽¹⁾	—	—	—	—	—	SPIFE	ENHBUF ⁽¹⁾
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO ⁽⁴⁾	MODE32	MODE16	SMP	CKE ⁽²⁾
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP ⁽³⁾	MSTEN	DISSDI ⁽⁴⁾	STXISEL<1:0>		SRXISEL<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **FRMEN**: Framed SPI Support bit

- 1 = Framed SPI support is enabled (\overline{SSx} pin is used as the FSYNC1 input/output)
- 0 = Framed SPI support is disabled

bit 30 **FRMSYNC**: Frame Sync Pulse Direction Control on \overline{SSx} Pin bit (Framed SPI mode only)

- 1 = Frame sync pulse input (Slave mode)
- 0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL**: Frame Sync Polarity bit (Framed SPI mode only)

- 1 = Frame pulse is active-high
- 0 = Frame pulse is active-low

bit 28 **MSEN**: Master Mode Slave Select Enable bit

- 1 = Slave select SPI support is enabled; the \overline{SSx} pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
- 0 = Slave select SPI support is disabled

bit 27 **FRMSYPW**: Frame Sync Pulse-Width bit

- 1 = Frame sync pulse is one character wide
- 0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>**: Frame Sync Pulse Counter bits

Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.

- 111 = Reserved
- 110 = Reserved
- 101 = Generates a frame sync pulse on every 32 data characters
- 100 = Generates a frame sync pulse on every 16 data characters
- 011 = Generates a frame sync pulse on every 8 data characters
- 010 = Generates a frame sync pulse on every 4 data characters
- 001 = Generates a frame sync pulse on every 2 data characters
- 000 = Generates a frame sync pulse on every data character

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 15-1: RTCCON1: RTCC CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0> ⁽¹⁾							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	WRLOCK ⁽²⁾	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RTCOE	OUTSEL<2:0>			—	—	—	—

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit

1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits

11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits⁽¹⁾

11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
...
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit

1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: To clear this bit, an unlock sequence is required. Refer to **Section 23.4 "System Registers Write Protection"** for details.

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REGISTER 15-6: ALMDATE: ALARM DATE REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MHTTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MHTTEN:** Binary Coded Decimal Value of Months 10-Digit bit

Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits

Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits

Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits

Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits

Contains a value from 0 to 6.

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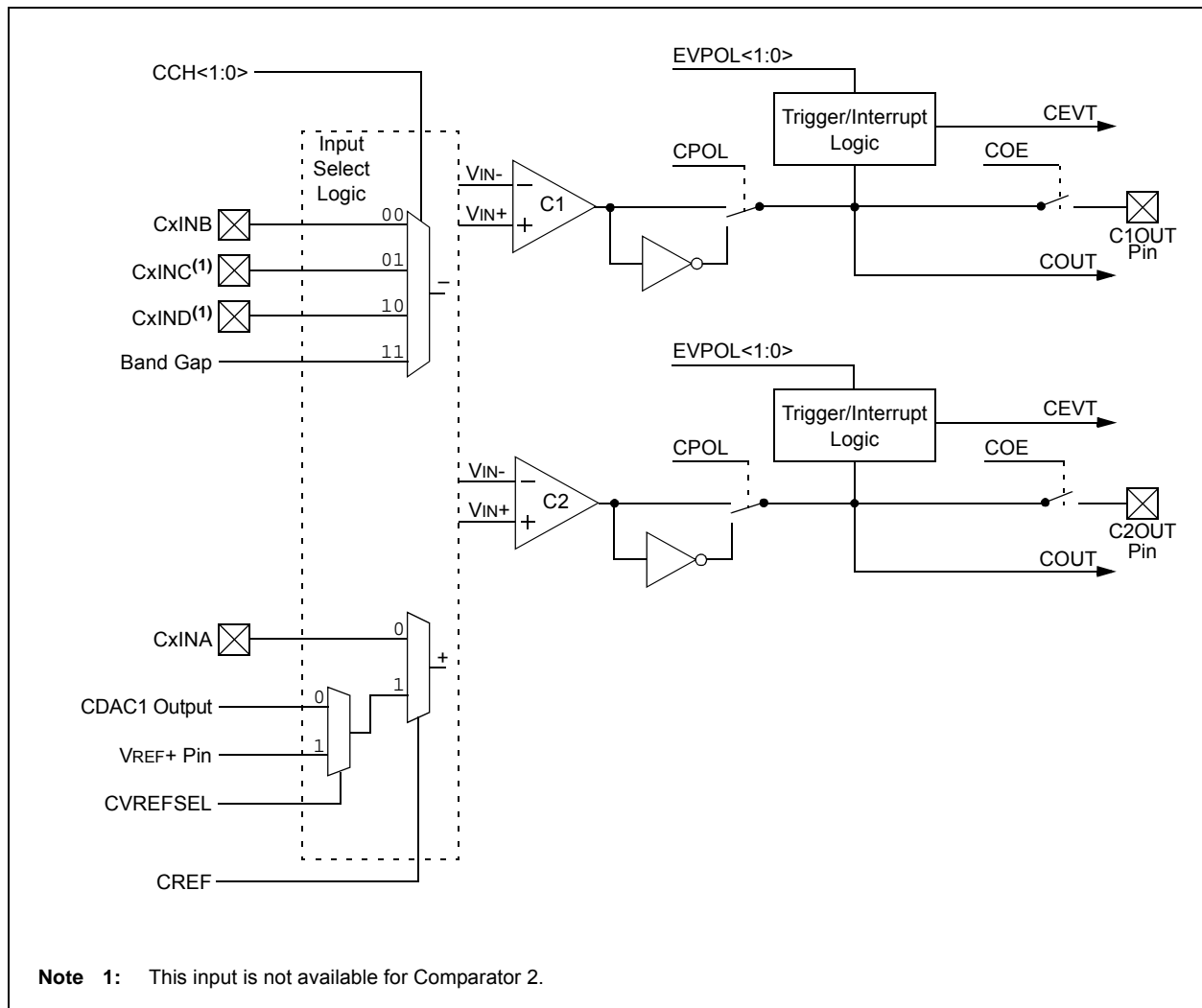
19.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS600011110) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides two dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals ‘1’, the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 19-1. Each comparator has its own control register, CMxCON (Register 19-2), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (Register 19-1).

FIGURE 19-1: DUAL COMPARATOR MODULE BLOCK DIAGRAM



23.9 Configuration Words and System Registers

TABLE 23-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>			SWDTPS<4:0>			
17D4	FOSCSSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSSEL	r-1	OSCI OFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

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24.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

24.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

24.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

24.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

25.0 INSTRUCTION SET

The PIC32MM0064GPL036 family instruction set complies with the MIPS® Release 3 instruction set architecture. Only microMIPS32™ instructions are supported. The PIC32MM0064GPL036 family does not have the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to the “MIPS® Architecture for Programmers Volume II-B: The microMIPS32™ Instruction Set” at www.imgtec.com for more information.

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FIGURE 26-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

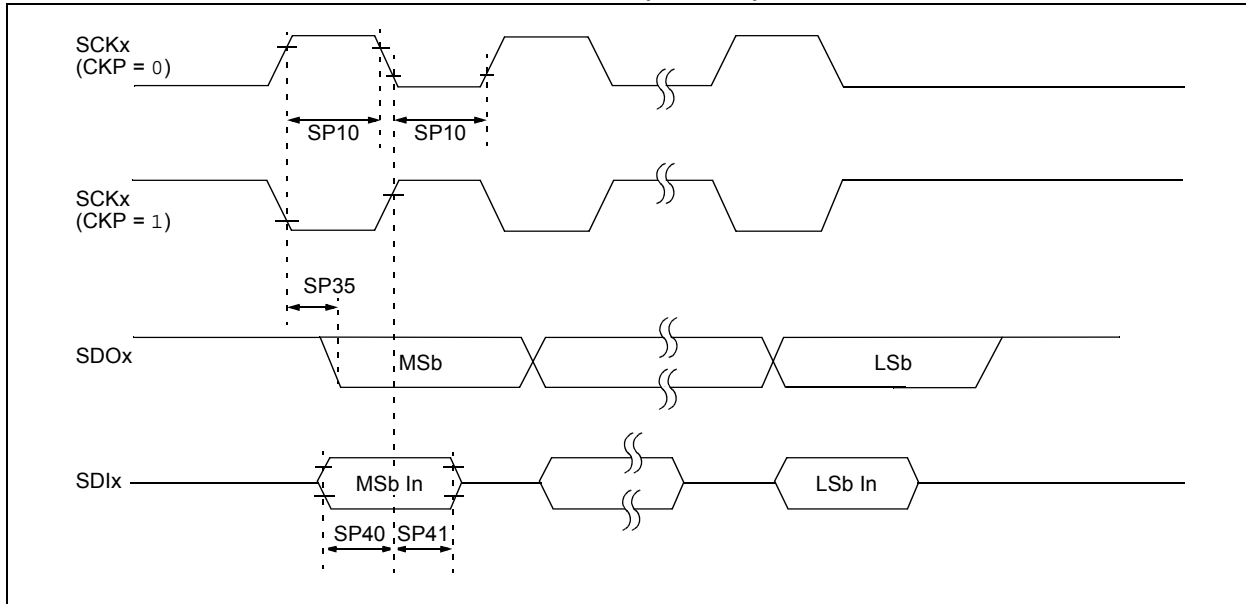
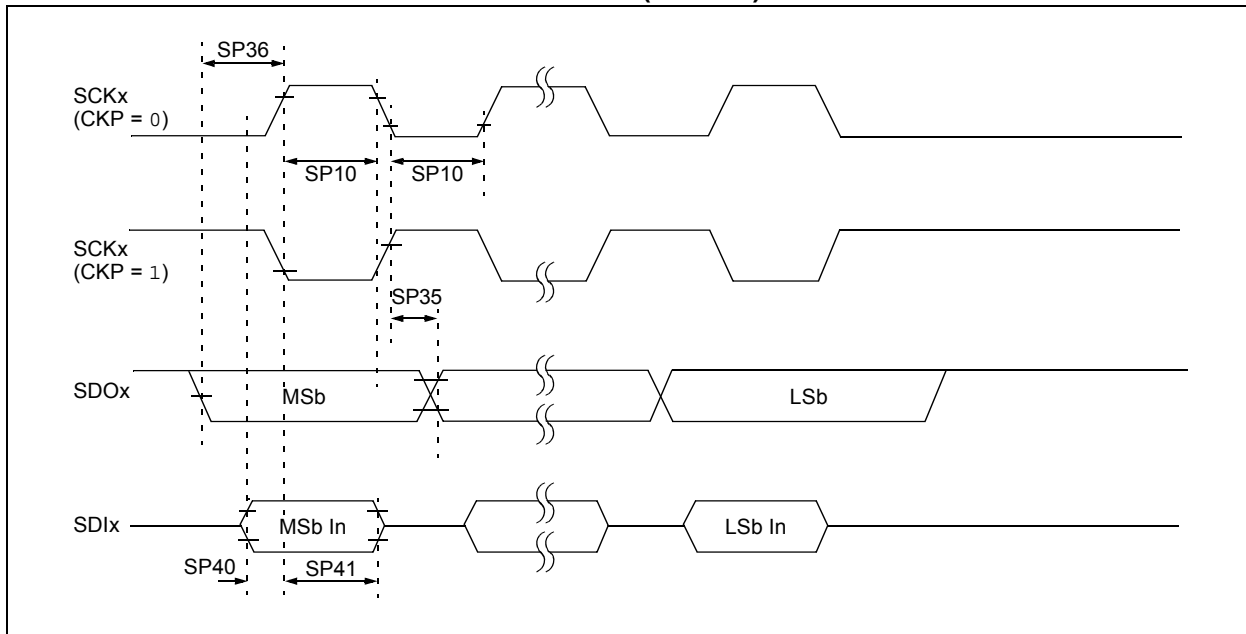


FIGURE 26-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



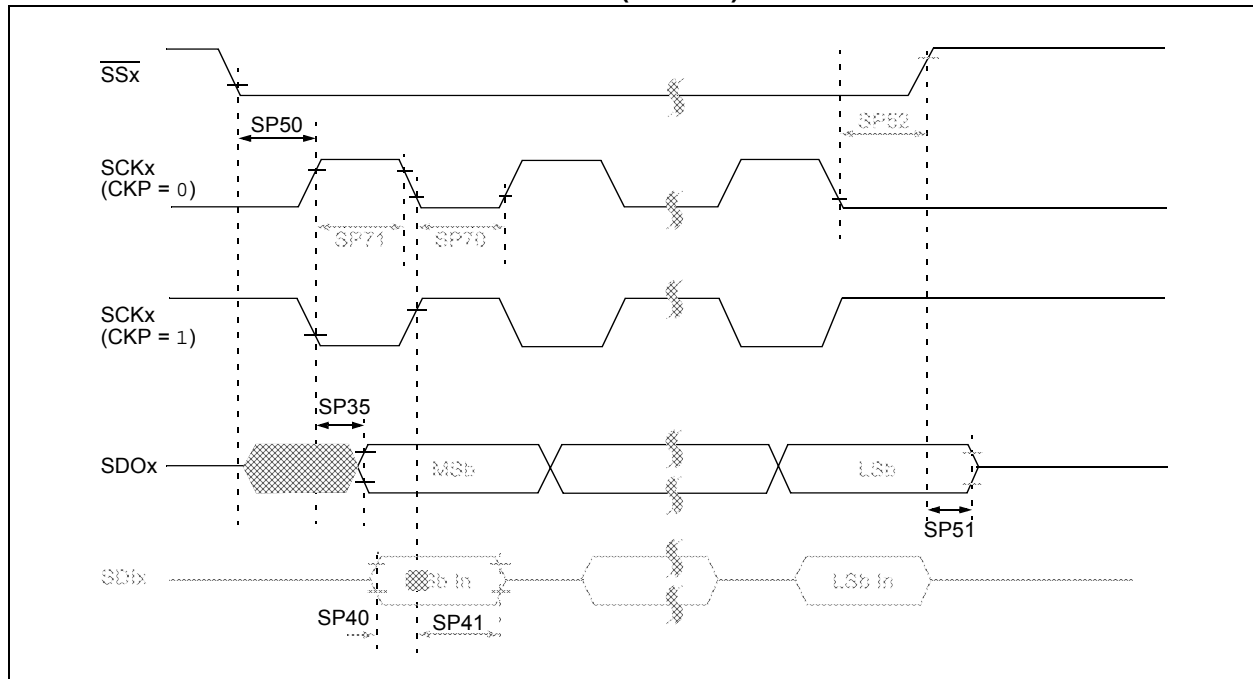
PIC32MM0064GPL036 FAMILY

TABLE 26-28: SPIx MODULE MASTER MODE TIMING REQUIREMENTS

Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ (unless otherwise stated)					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min	Max	Units
SP10	TsCL, Tsch	SCKx Output Low or High Time	10	—	ns
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	7	ns
SP36	TdoV2sc, TdoV2scl	SDOx Data Output Setup to First SCKx Edge	7	—	ns
SP40	TdIV2sch, TdIV2scl	Setup Time of SDIx Data Input to SCKx Edge	7	—	ns
SP41	Tsch2dIL, TscL2dIL	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns

Note 1: These parameters are characterized but not tested in manufacturing.

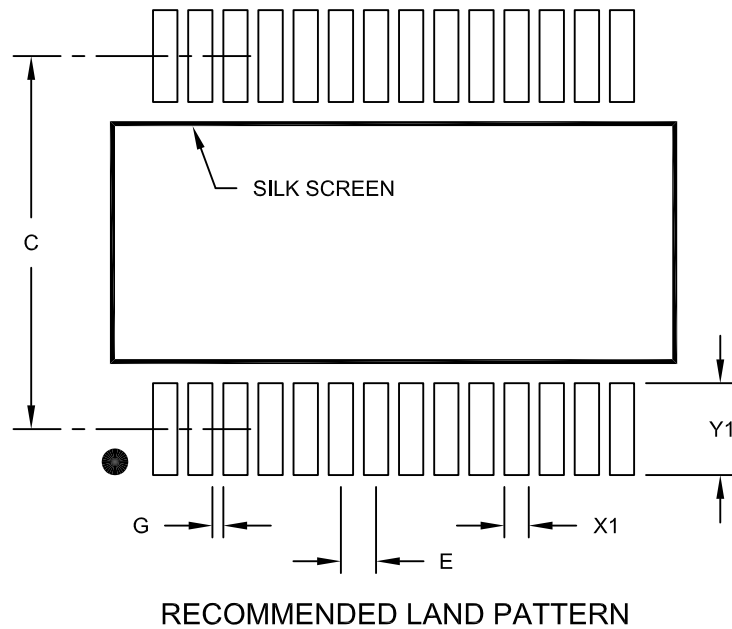
FIGURE 26-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A