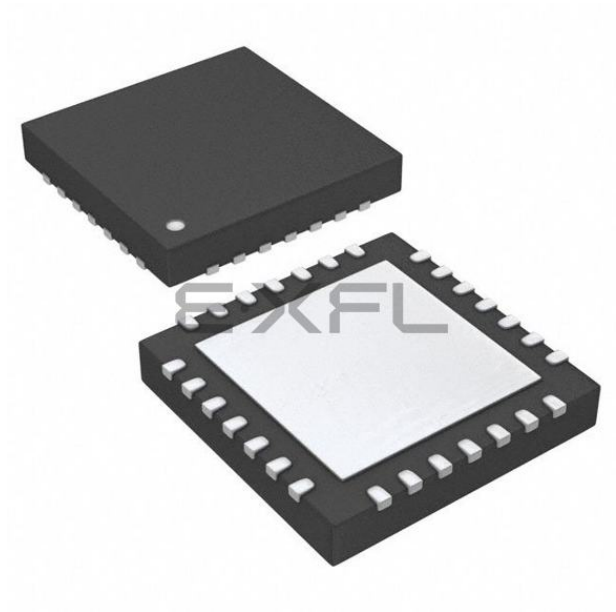
Microchip Technology - PIC32MM0032GPL028-I/ML Datasheet



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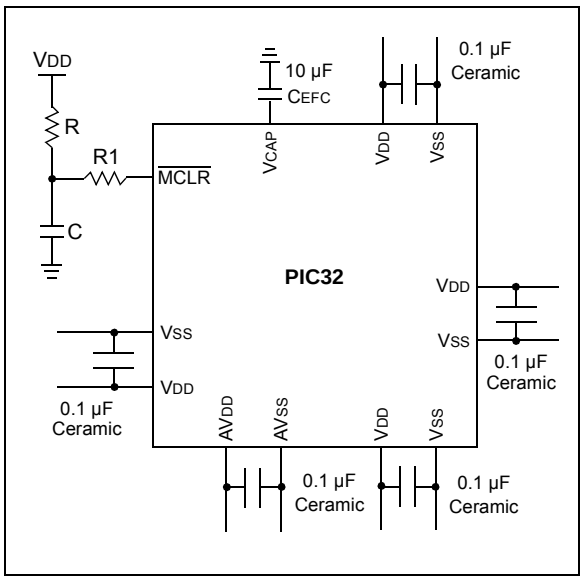
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl028-i-ml

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides for two specific device functions:

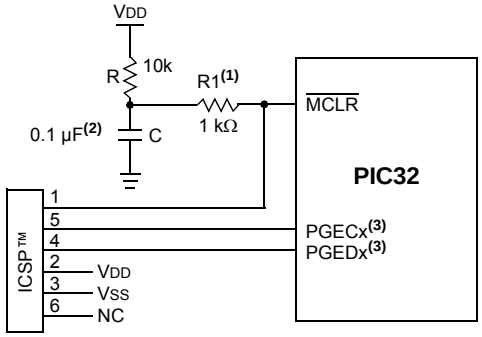
- Device Reset
- Device Programming and Debugging

Pulling The $\overline{MCLR}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{MCLR}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{MCLR}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS(1,2,3)



Note 1: $470\Omega \leq R1 \leq 1\ k\Omega$ will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met without interfering with the debug/programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.4 Capacitor on Internal Voltage Regulator (V_{CAP})

A low-ESR (<1 Ohm) capacitor is required on the V_{CAP} pin, which is used to stabilize the internal voltage regulator output. The V_{CAP} pin must not be connected to V_{DD} and must have a C_{EFC} capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. The recommended value of the C_{EFC} capacitor is 10 µF. On the printed circuit board, it should be placed as close to the V_{CAP} pin as possible. If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to this capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF.

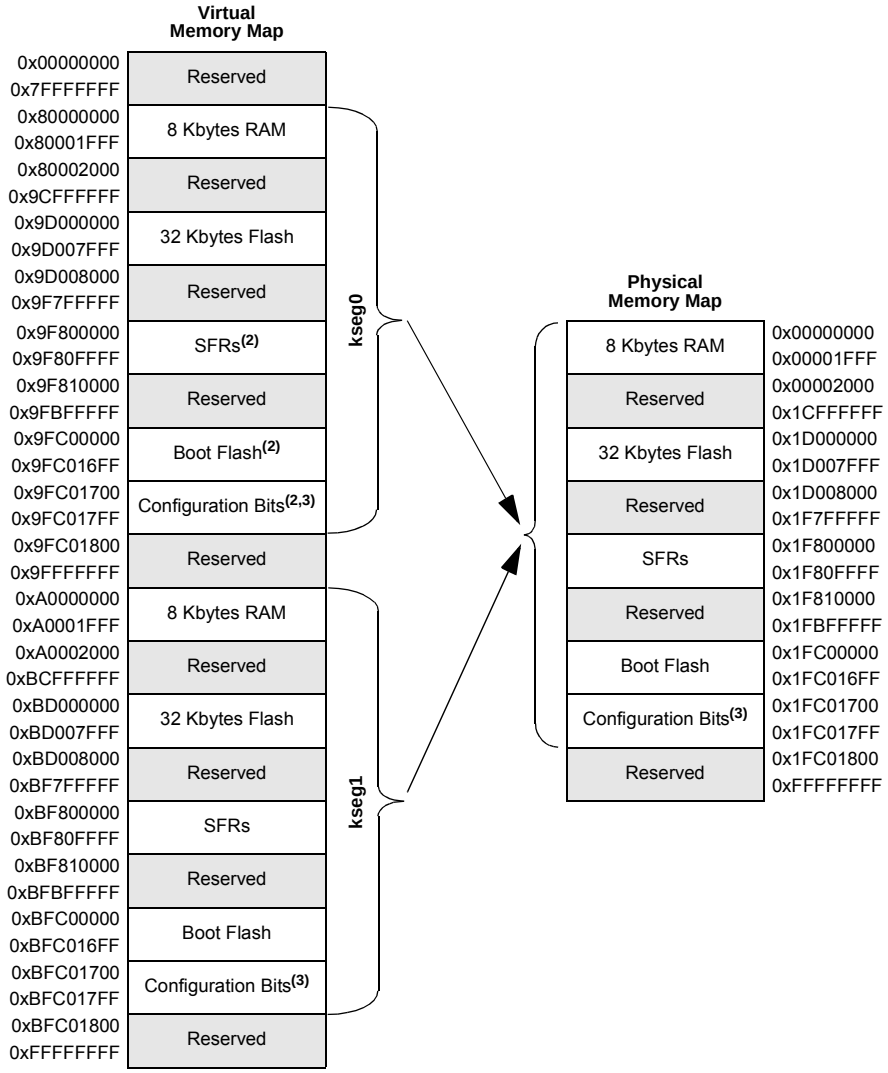
TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-3	Reserved	Reserved in the microAptiv™ UC.
4	UserLocal	User information that can be written by privileged software and read via RDHWR, Register 29.
5-6	Reserved	Reserved in the microAptiv UC.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-Privileged mode.
8	BadVAddr(1)	Reports the address for the most recent address related exception.
9	Count(1)	Processor cycle count.
10	Reserved	Reserved in the microAptiv UC.
11	Compare(1)	Timer interrupt control.
12	Status/ IntCtl/ SRSCtl/ SRSMap1/ View_IPL/ SRSMAP2	Processor status and control; interrupt control and shadow set control.
13	Cause(1)/ View_RIPL	Cause of last exception.
14	EPC(1)	Program Counter at last exception.
15	PRId/ EBase/ CDMMBase	Processor identification and revision; exception base address; Common Device Memory Map Base register.
16	CONFIG/ CONFIG1/ CONFIG2/ CONFIG3/ CONFIG7	Configuration registers.
7-22	Reserved	Reserved in the microAptiv UC.
23	Debug/ Debug2/ TraceControl/ TraceControl2/ UserTraceData1/ TraceBPC(2)	EJTAG Debug register. EJTAG Debug Register 2. EJTAG Trace Control register. EJTAG Trace Control Register 2. EJTAG User Trace Data 1 register. EJTAG Trace Breakpoint register.
24	DEPC(2)/ UserTraceData2	Program Counter at last debug exception. EJTAG User Trace Data 2 register.
25	PerfCtl0/ PerfCnt0/ PerfCtl1/ PerfCnt1	Performance Counter 0 control. Performance Counter 0. Performance Counter 1 control. Performance Counter 1.
26	ErrCtl	Software parity check enable.
27	CacheErr	Records information about SRAM parity errors.
28-29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC(1)	Program Counter at last error.
31	DeSAVE(2)	Debug Handler Scratchpad register.

Note 1: Registers used in exception processing.

2: Registers used in debug.

FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 32 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

5.2 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2380	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	—	—	—	—	NVMOP<3:0>				0000
2390	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
23A0	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
23B0	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
23C0	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
23D0	NVMSRCADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
23E0	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
23F0	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BWPULOCK	—	—	—	—	BWP<2:0>			—	—	—	—	—	—	—	—	8700

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

7.1 CPU Exceptions

CPU Coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion of $\overline{\text{MCLR}}$.	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Execution of a RESET instruction.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DINT	—	—
NMI	Non-maskable interrupt.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2	IPL<2:0>	—	Int (0x00)	See Table 7-2
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIB	—	—
AdEL	Load address alignment error.	EBASE + 0x180	EXL	—	ADEL (0x04)	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE + 0x180	EXL	—	IBE (0x06)	_general_exception_handler
DBp	EJTAG breakpoint (execution of SDBBP instruction).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	DBp	—	—	—
Sys	Execution of SYSCALL instruction.	EBASE + 0x180	EXL	—	Sys (0x08)	_general_exception_handler
Bp	Execution of BREAK instruction.	EBASE + 0x180	EXL	—	Bp (0x09)	_general_exception_handler

9.0 I/O PORTS

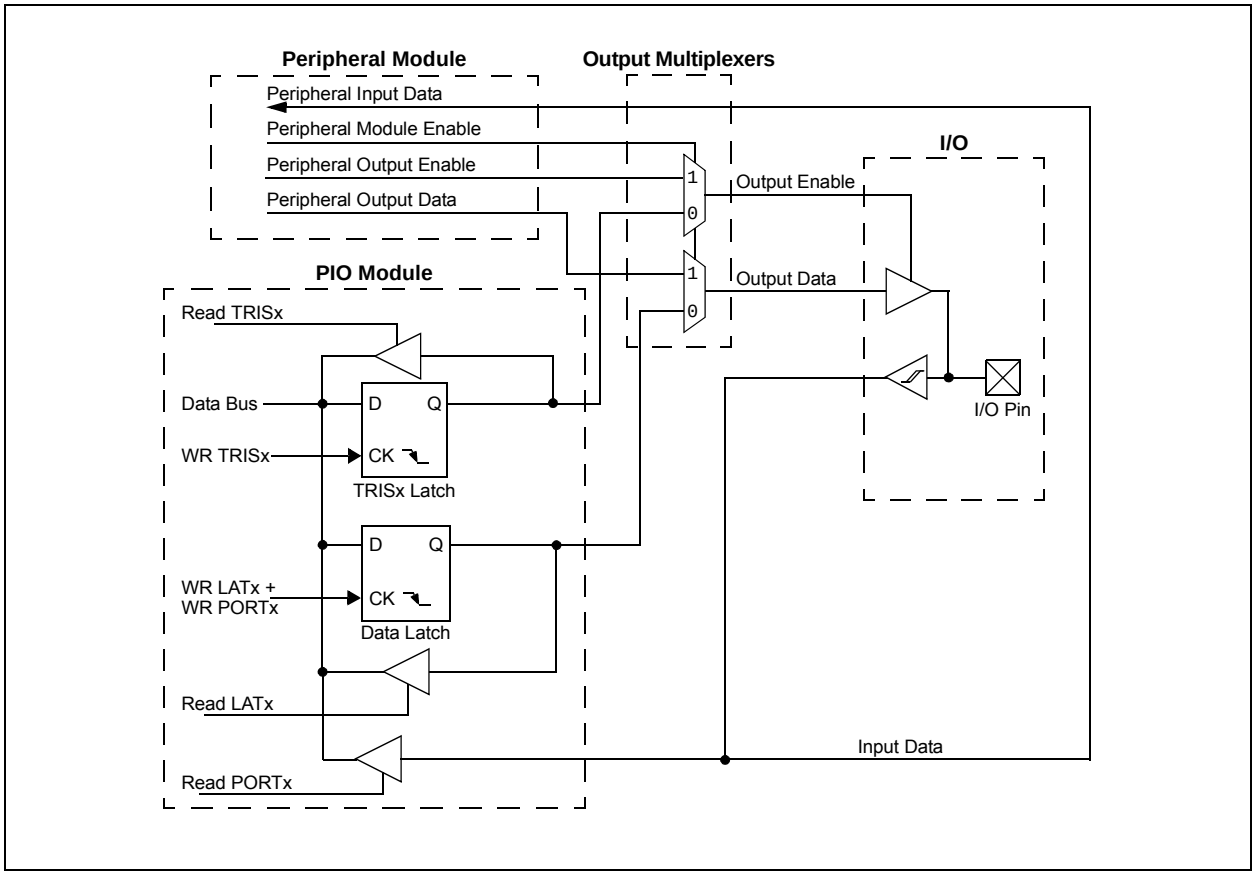
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

Many of the device pins are shared among the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. Some pins in the devices are 5V tolerant pins. Some of the key features of the I/O ports are:

- Individual Output Pin Open-Drain Enable/Disable
- Individual Input Pin Weak Pull-up and Pull-Down
- Monitor Selective Inputs and Generate Interrupt when Change-in-Pin State is Detected
- Operation during Sleep and Idle modes
- Fast Bit Manipulation using the CLR, SET and INV registers

Figure 9-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 9-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 23 **MCLKSEL:** Master Clock Enable bit(1)
1 = REFCLKO is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator (1:1 with SYSCLK)

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** SPIx Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPIx Module On bit
1 = SPIx module is enabled
0 = SPIx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues operation when CPU enters Idle mode
0 = Continues operation in Idle mode

bit 12 **DISSDO:** Disable SDOx Pin bit(4)
1 = SDOx pin is not used by the module; the pin is controlled by the associated PORTx register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16/8-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
1	0	32-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
0	1	16-bit data, 16-bit FIFO, 32-bit channel/64-bit frame
0	0	16-bit data, 16-bit FIFO, 16-bit channel/32-bit frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPIx is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPIx Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER (CONTINUED)

bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB, is empty
0 = Transmit buffer, SPIxTXB, is not empty
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit buffer is not full
Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.
Enhanced Buffer mode:
Set when the CPU Write Pointer (CWPTR) + 1 = SPI Read Pointer (SRPTR); cleared otherwise.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB, is full
0 = Receive buffer, SPIxRXB, is not full
Standard Buffer mode:
Automatically set in hardware when the SPIx module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise.

REGISTER 15-5: RTCDATE: RTCC DATE REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	YRTEN<3:0>				YRONE<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YRTEN<3:0>:** Binary Coded Decimal Value of Years 10-Digit bits

bit 27-24 **YRONE<3:0>:** Binary Coded Decimal Value of Years 1-Digit bits

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

REGISTER 15-6: ALMDATE: ALARM DATE REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—		—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

REGISTER 16-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	BUFREGEN(1)	CSCNA	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BUFS	—	SMPI<3:0>				BUFM	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC VR+	ADC VR-
000	AVDD	AVSS
001	AVDD	External VREF- Pin
010	External VREF+ Pin	AVSS
011	External VREF+ Pin	External VREF- Pin
1xx	Unimplemented; do not use	

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference
0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit(1)

1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Mode bit

1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1 (ADC buffers split into 2 x 8-word buffers).
1 = ADC is currently filling Buffers 8-15, user should access data in 0-7
0 = ADC is currently filling Buffers 0-7, user should access data in 8-15

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF(0...7), ADC1BUF(8...15)
0 = Buffer configured as one 16-word buffer, ADC1BUF(0...15)

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit only takes effect when the auto-scan feature is enabled (ASEN (AD1CON5<15>) = 1.

REGISTER 17-1: CRCCON: CRC CONTROL REGISTER (CONTINUED)

bit 2 **MOD:** CRC Calculation Mode bit
1 = Alternate mode
0 = Legacy mode

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 17-2: CRCXOR:CRC XOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	X<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **X<31:1>:** XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented:** Read as '0'

REGISTER 20-1: DAC1CON: CDAC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DACDAT<4:0>				
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON	—	—	—	—	—	—	DACOE
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **DACDAT<4:0>:** CDAC Voltage Reference Selection bits

11111 = (DACDAT<4:0> * VREF+/32) or (DACDAT<4:0> * AVDD/32) volts depending on the REFSEL<1:0> bits
•
•
•
00000 = 0.0 volts

bit 15 **ON:** Voltage Reference Enable bit

1 = Voltage reference is enabled
0 = Voltage reference is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** CDAC Voltage Reference Output Enable bit

1 = Voltage level is output on the CDAC1 pin
0 = Voltage level is disconnected from the CDAC1 pin

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** CDAC Voltage Reference Source Select bits

11 = Reference voltage is AVDD
10 = No reference is selected – output is AVSS
01 = Reference voltage is the VREF+ input pin voltage
00 = No reference is selected – output is AVSS

TABLE 26-4: OPERATING CURRENT (I_{DD})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC19	0.45	0.65	mA	2.0V	FSYS = 1 MHz
	0.45	0.65	mA	3.3V	
DC23	2.5	3.5	mA	2.0V	FSYS = 8 MHz
	2.5	3.5	mA	3.3V	
DC24	7.0	9.2	mA	2.0V	FSYS = 25 MHz
	7.0	9.2	mA	3.3V	
DC25	0.26	0.35	mA	2.0V	FSYS = 32 kHz
	0.26	0.35	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IDD current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins (except OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- NOP instructions are executed

FIGURE 26-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

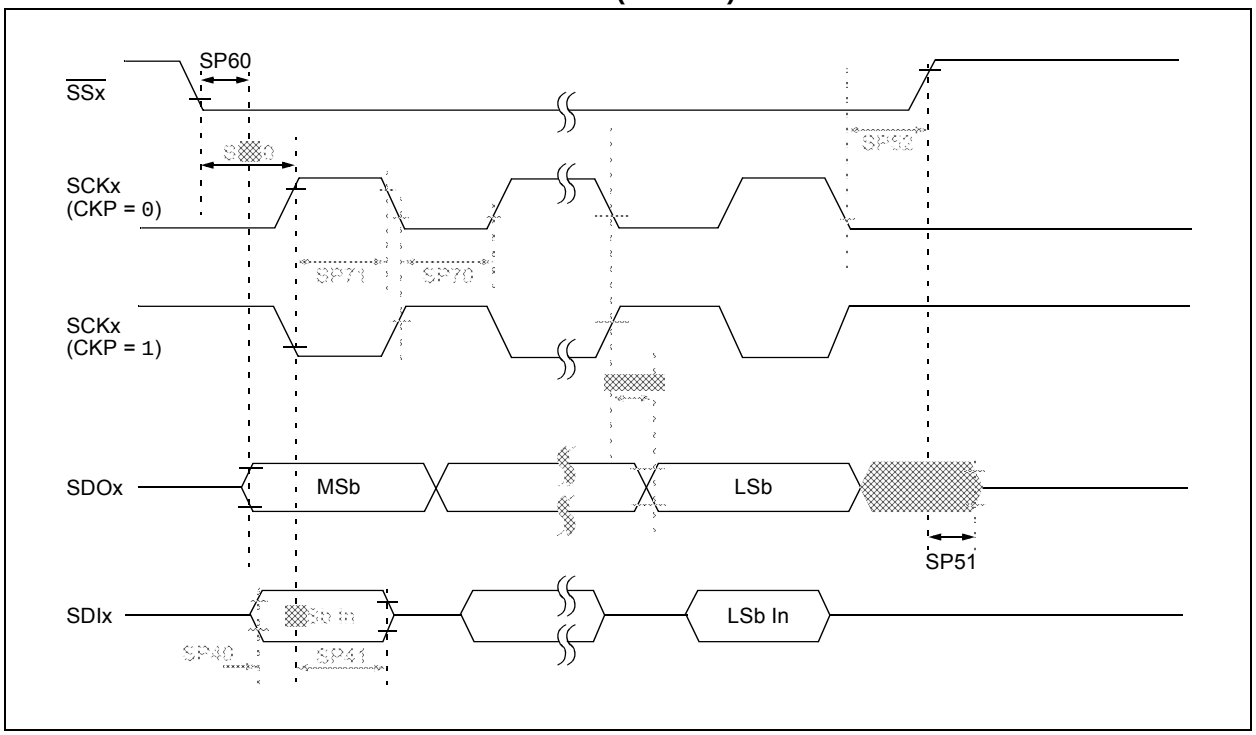


TABLE 26-29: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS

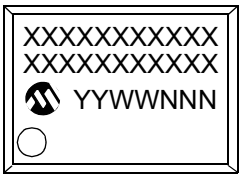
Operating Conditions: 2.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C (unless otherwise stated)					
Param.No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
SP70	TscL	SCKx Input Low Time	10	—	ns
SP71	TscH	SCKx Input High Time	10	—	ns
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	ns
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	ns
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	40	—	ns
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	2.5	12	ns
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	ns
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	12.5	ns

Note 1: These parameters are characterized but not tested in manufacturing.

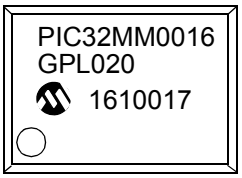
27.0 PACKAGING INFORMATION

27.1 Package Marking Information

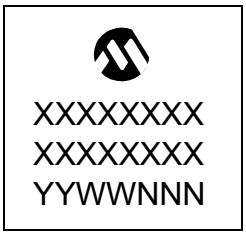
20-Lead SSOP



Example

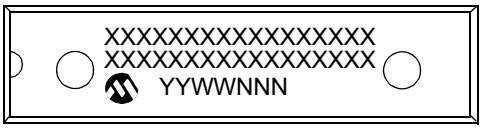


20-Lead QFN

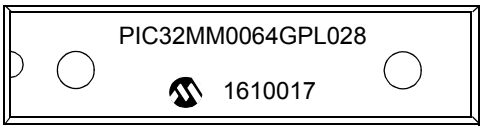


Example

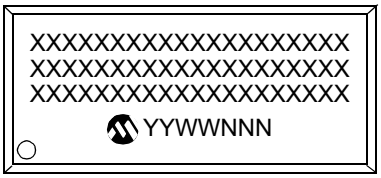
28-Lead SPDIP



Example



28-Lead SOIC (7.5 mm)



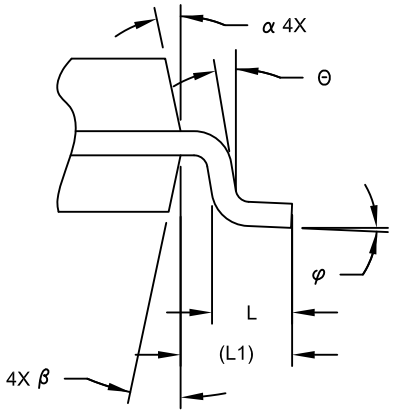
Example

Legend:	XX...X	Customer-specific information
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	*****	All packages are Pb-free

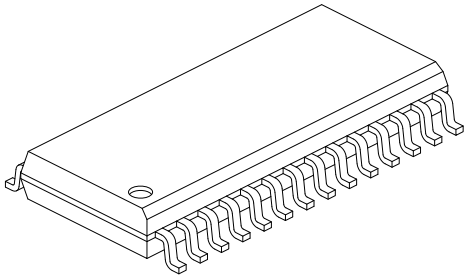
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

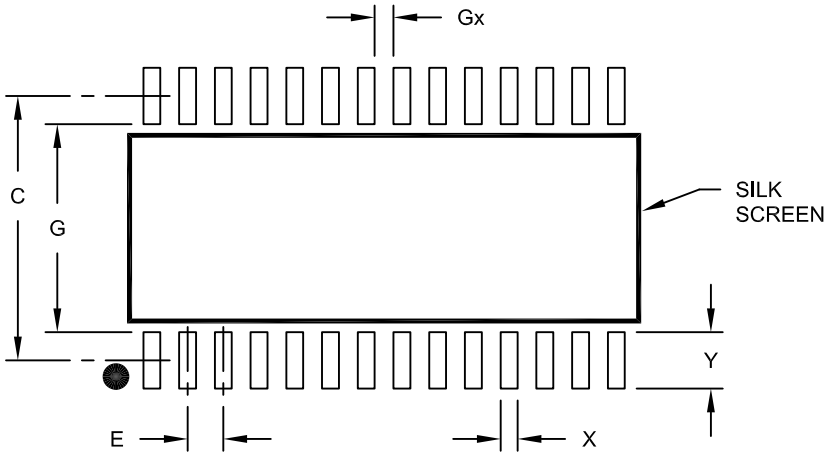
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

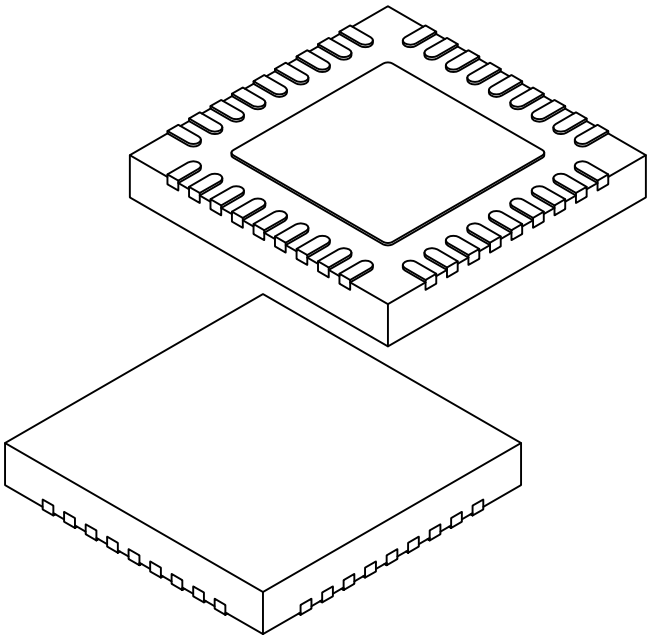
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.45	0.55	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-272B-M2 Sheet 2 of 2

NOTES: