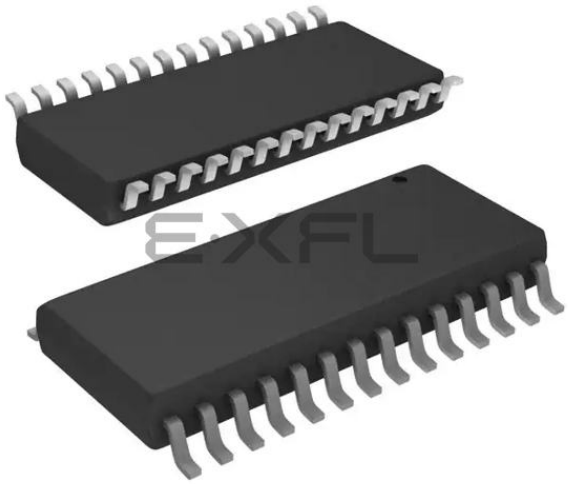

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl028-i-so

7.2 Interrupts

The PIC32MM0064GPL036 family uses fixed offset for vector spacing. For details, refer to **Section 8. "Interrupts"** (DS60001108) in the *"PIC32 Family Reference Manual"*. Table 7-2 provides the interrupt related vectors and bits information.

TABLE 7-2: INTERRUPTS

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
Core Timer	_CORE_TIMER_VECTOR	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software 0	_CORE_SOFTWARE_0_VECTOR	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software 1	_CORE_SOFTWARE_1_VECTOR	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External 0	_EXTERNAL_0_VECTOR	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
External 1	_EXTERNAL_1_VECTOR	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
External 2	_EXTERNAL_2_VECTOR	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	No
External 3	_EXTERNAL_3_VECTOR	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	No
External 4	_EXTERNAL_4_VECTOR	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
PORTA Change Notification	_CHANGE_NOTICE_A_VECTOR	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
PORTB Change Notification	_CHANGE_NOTICE_B_VECTOR	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
PORTC Change Notification	_CHANGE_NOTICE_C_VECTOR	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	No
Timer1	_TIMER_1_VECTOR	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	No
Comparator 1	_COMPARATOR_1_VECTOR	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
Comparator 2	_COMPARATOR_2_VECTOR	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Real-Time Clock Alarm	_RTCC_VECTOR	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
ADC Conversion	_ADC_VECTOR	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	No
CRC	_CRC_VECTOR	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
High/Low-Voltage Detect	_HLVD_VECTOR	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	Yes
Logic Cell 1	_CLC1_VECTOR	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Logic Cell 2	_CLC2_VECTOR	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
SPI1 Error	_SPI1_ERR_VECTOR	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
SPI1 Transmission	_SPI1_TX_VECTOR	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes
SPI1 Reception	_SPI1_RX_VECTOR	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	Yes

TABLE 9-5: PORTB REGISTER MAP

Virtual Address (BF80_#)	Register Name(2)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2700	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB<15:12>				—	—	—	—	—	—	—	—	ANSB<3:0>(1)				F00F
2710	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB<15:0>(1)																FFFF
2720	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB<15:0>(1)																0000
2730	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB<15:0>(1)																0000
2740	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB<15:0>(1)																0000
2750	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB<15:0>(1)																0000
2760	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB<15:0>(1)																0000
2770	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—	0000
2780	CNEN0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB<15:0>(1)																0000
2790	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATB<15:0>(1)																0000
27A0	CNEN1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1B<15:0>(1)																0000
27B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB<15:0>(1)																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits<11:10,6:5,3> are not implemented in 20-pin devices.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 9-1: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER (x = A-C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	CNSTYLE	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notification (CN) Control On bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit
1 = Edge style (detects edge transitions, CNFx bits are used for a Change Notice event)
0 = Mismatch style (detects change from last PORTx read, CNSTATx bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 11-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R/W-y
	CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on Reset		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to this location using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RWDTPS<4:0> Configuration bits in FWDT.

bit 7-6 **CLKSEL<1:0>:** Shadow Copy of Watchdog Timer Clock Selection Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RCLKSEL<1:0> Configuration bits in FWDT.

bit 5-1 **SLPDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Sleep/Idle Mode from Configuration bits
On Reset, these bits are set to the values of the SWDTPS<4:0> Configuration bits in FWDT.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
On Reset, this bit is set to the value of the WINDIS Configuration bit in FWDT.
1 = Windowed mode is enabled
0 = Windowed mode is disabled

Note 1: This bit only has control when FWDTEN (FWDT<15>) = 0.

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 20-16 **SYNC<4:0>:** CCPx Synchronization Source Select bits
11111 = Timer is in the Free-Running mode and rolls over at FFFFh (Timer Period register is ignored)
11110 = Reserved
. . .
11100 = Reserved
11011 = Time base is synchronized to the start of ADC conversion
11010 = Reserved
11001 = Time base is synchronized to Comparator 2
11000 = Time base is synchronized to Comparator 1
10111 = Reserved
. . .
10010 = Reserved
10001 = Time base is synchronized to CLC2
10001 = Time base is synchronized to CLC1
01111 = Reserved
01110 = Reserved
01101 = Time base is synchronized to the INT4 pin (remappable)
01100 = Time base is synchronized to the INT3 pin
01011 = Time base is synchronized to the INT2 pin
01010 = Time base is synchronized to the INT1 pin
01001 = Time base is synchronized to the INT0 pin
01000 = Reserved
. . .
00101 = Reserved
00100 = Time base is synchronized to SCCP3
00011 = Time base is synchronized to SCCP2
00010 = Time base is synchronized to MCCP1
00001 = Time base is synchronized to this MCCP/SCCP
00000 = No external synchronization; timer rolls over at FFFFh or matches with the Timer Period register

bit 15 **ON:** CCPx Module Enable bit(1)
1 = Module is enabled with the operating mode specified by the MOD<3:0> bits
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** CCPx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **CCPSLP:** CCPx Sleep Mode Enable bit
1 = Module continues to operate in Sleep modes
0 = Module does not operate in Sleep modes

bit 11 **TMRSYNC:** Time Base Clock Synchronization bit
1 = Module time base clock is synchronized to internal system clocks; timing restrictions apply
0 = Module time base clock is not synchronized to internal system clocks

bit 10-8 **CLKSEL<2:0>:** CCPx Time Base Clock Select bits
111 = TCKIA pin (remappable)
110 = TCKIB pin (remappable)
101 = Reserved
100 = Reserved
011 = CLC1 output for MCCP1 and SCCP2/CLC2 output for SCCP3
010 = Secondary Oscillator (SOSC) clock
001 = REFCLKO output clock
000 = System clock (FSYS)

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

13.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

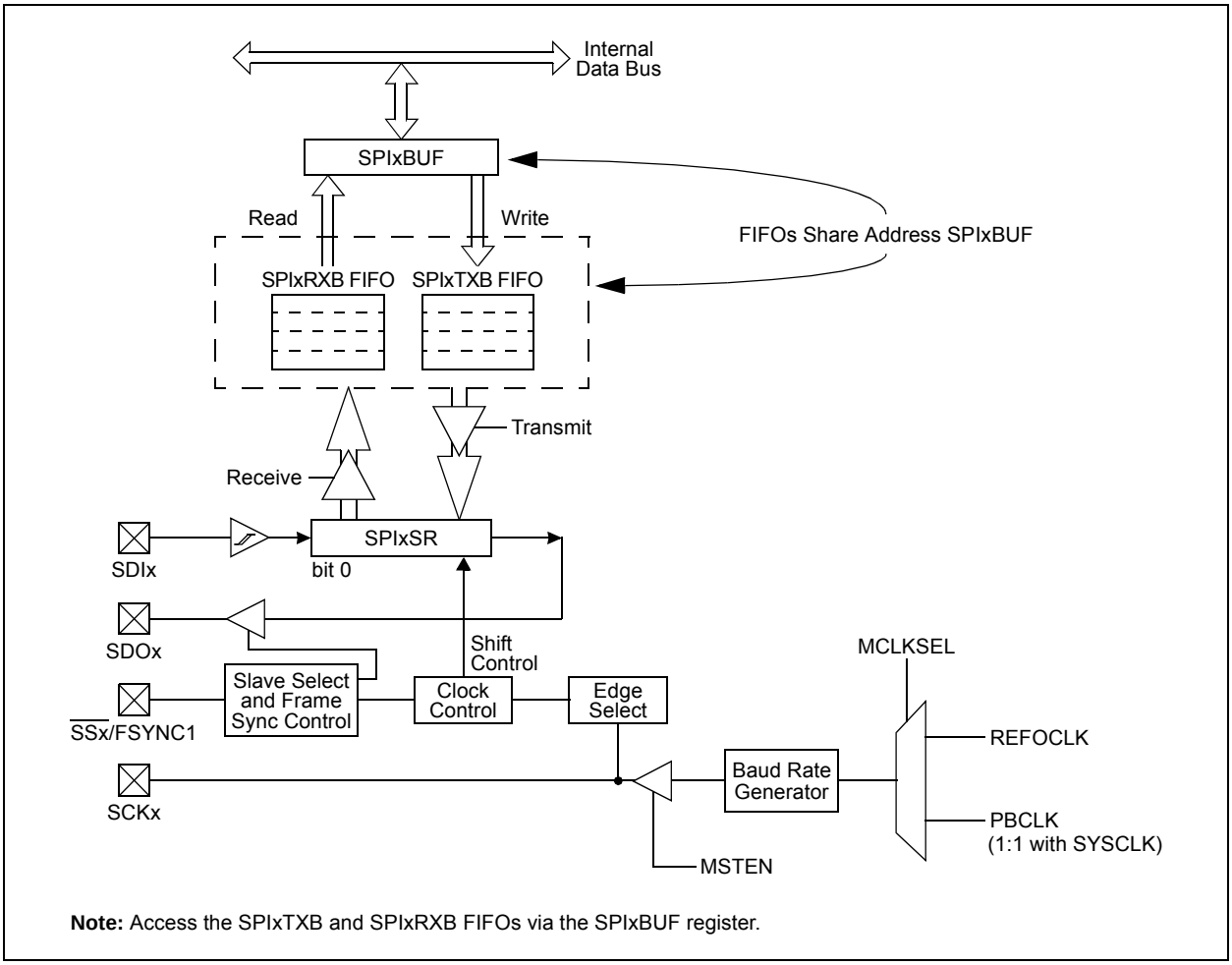
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes Support
- Four Different Clock Formats
- Enhanced Framed SPI Protocol Support
- User-Configurable 8-Bit, 16-Bit and 32-Bit Data Width
- Separate SPI FIFO Buffers for Receive and Transmit:
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable Interrupt Event on Every 8-Bit, 16-Bit and 32-Bit Data Transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol

FIGURE 13-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access the SPIxTXB and SPIxRXB FIFOs via the SPIxBUF register.

REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPIx Frame Error status bit
1 = Frame error is detected
0 = No frame error is detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPIx Activity Status bit
1 = SPIx peripheral is currently busy with some transactions
0 = SPIx peripheral is currently Idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** SPIx Transmit Underrun (TUR) bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When the SPIx Shift register is empty
0 = When the SPIx Shift register is not empty

bit 6 **SPIROV:** SPIx Receive Overflow (ROV) Flag bit
1 = New data is completely received and discarded; the user software has not read the previous data in the SPIxBUF register
0 = No overflow has occurred
This bit is set in hardware; it can only be cleared (= 0) in software.

bit 5 **SPIRBE:** SPIx RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CPU Read Pointer (CRPTR) = SPI Write Pointer (SWPTR))
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

REGISTER 15-3: RTCSTAT: RTCC STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0, HS, HC	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
- 1 = An alarm event has occurred
- 0 = An alarm event has not occurred

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Synchronization Status bit
- 1 = Time registers may change during software read
- 0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization status bit
- 1 = Alarm registers (ALMTIME and ALMDATE) and RTCCON1 should not be modified; the ALRMEN and ALMRPT<7:0> bits may change during software read
- 0 = Alarm registers and Alarm Control registers may be modified safely

bit 0 **HALFSEC:** Half Second Status bit
- 1 = Second half of 1-second period
- 0 = First half of 1-second period

TABLE 16-1: ADC REGISTER MAP

Virtual Address (BF80_#)	Register Name(3)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0700	ADC1BUF0	31:16	ADC1BUF0<31:0>																0000
		15:0																	0000
0710	ADC1BUF1	31:16	ADC1BUF1<31:0>																0000
		15:0																	0000
0720	ADC1BUF2	31:16	ADC1BUF2<31:0>																0000
		15:0																	0000
0730	ADC1BUF3	31:16	ADC1BUF3<31:0>																0000
		15:0																	0000
0740	ADC1BUF4	31:16	ADC1BUF4<31:0>																0000
		15:0																	0000
0750	ADC1BUF5	31:16	ADC1BUF5<31:0>																0000
		15:0																	0000
0760	ADC1BUF6	31:16	ADC1BUF6<31:0>																0000
		15:0																	0000
0770	ADC1BUF7	31:16	ADC1BUF7<31:0>																0000
		15:0																	0000
0780	ADC1BUF8	31:16	ADC1BUF8<31:0>																0000
		15:0																	0000
0790	ADC1BUF9	31:16	ADC1BUF9<31:0>																0000
		15:0																	0000
07A0	ADC1BUF10	31:16	ADC1BUF10<31:0>																0000
		15:0																	0000
07B0	ADC1BUF11	31:16	ADC1BUF11<31:0>																0000
		15:0																	0000
07C0	ADC1BUF12	31:16	ADC1BUF12<31:0>																0000
		15:0																	0000
07D0	ADC1BUF13	31:16	ADC1BUF13<31:0>																0000
		15:0																	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

2: The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 16-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	EXTSAM	—	SAMC<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source (TSRC) bit
1 = Clock derived from Fast RC (FRC) oscillator
0 = Clock derived from Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK)

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = ADC is still sampling after SAMP bit = 0
0 = ADC stops sampling when SAMP bit = 0

bit 13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
11111111 = 2 • TSRC • ADCS<7:0> = 510 • TSRC = TAD
•
•
•
00000001 = 2 • TSRC • ADCS<7:0> = 2 • TSRC = TAD
00000000 = 1 • TSRC = TAD
Where TSRC is a period of clock selected by the ADRC bit (AD1CON3<15>).

REGISTER 16-6: AD1CSS: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	—	CSS<30:28>			—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CSS<13:8>(1,2)					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-28 **CSS<30:28>:** ADC Input Pin Scan Selection bits
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

bit 27-14 **Unimplemented:** Read as '0'

bit 13-0 **CSS<13:0>:** ADC Input Pin Scan Selection bits(1,2)
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

Note 1: The CSS<13:11> bits are not implemented in 20-pin devices.
2: The CSS<13:12> bits are not implemented in 28-pin devices.

NOTES:

REGISTER 18-1: CLCxCON: CLCx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	G4POL	G3POL	G2POL	G1POL
15:8	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	ON	—	—	—	INTP(1)	INTN(1)	—	—
7:0	R/W-0	R-0, HS, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>		

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 18 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 17 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 16 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

bit 15 **ON:** CLCx Enable bit
1 = CLCx is enabled and mixing input signals
0 = CLCx is disabled and has logic zero outputs

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **INTP:** CLCx Positive Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** CLCx Negative Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **LCOE:** CLCx Port Enable bit
1 = CLCx port pin output is enabled
0 = CLCx port pin output is disabled

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **G4D4T:** Gate 4 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 4
0 = The Data Source 4 signal is disabled for Gate 4

bit 30 **G4D4N:** Gate 4 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 4
0 = The Data Source 4 inverted signal is disabled for Gate 4

bit 29 **G4D3T:** Gate 4 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 4
0 = The Data Source 3 signal is disabled for Gate 4

bit 28 **G4D3N:** Gate 4 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 4
0 = The Data Source 3 inverted signal is disabled for Gate 4

bit 27 **G4D2T:** Gate 4 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 4
0 = The Data Source 2 signal is disabled for Gate 4

bit 26 **G4D2N:** Gate 4 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 4
0 = The Data Source 2 inverted signal is disabled for Gate 4

bit 25 **G4D1T:** Gate 4 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 4
0 = The Data Source 1 signal is disabled for Gate 4

bit 24 **G4D1N:** Gate 4 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 4
0 = The Data Source 1 inverted signal is disabled for Gate 4

bit 23 **G3D4T:** Gate 3 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 3
0 = The Data Source 4 signal is disabled for Gate 3

bit 22 **G3D4N:** Gate 3 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 3
0 = The Data Source 4 inverted signal is disabled for Gate 3

bit 21 **G3D3T:** Gate 3 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 3
0 = The Data Source 3 signal is disabled for Gate 3

20.1 CDAC Control Registers

TABLE 20-1: CDAC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0980	DAC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	DACDAT<4:0>					0000
		15:0	ON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

REGISTER 23-8: DEVID: DEVICE ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	VER<3:0>(1)				ID<27:24>(1)			
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<23:16>(1)							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<15:8>(1)							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

Note 1: Reset values are dependent on the device variant.

REGISTER 23-9: SYSKEY: SYSTEM UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SYSKEY<31:0>:** Unlock and Lock Key bits

TABLE 23-7: UNIQUE DEVICE IDENTIFIER (UDID) REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1840	UDID1	31:16	UDID Word 1<31:0>																xxxx
		15:0																	xxxx
1844	UDID2	31:16	UDID Word 2<31:0>																xxxx
		15:0																	xxxx
1848	UDID3	31:16	UDID Word 3<31:0>																xxxx
		15:0																	xxxx
184C	UDID4	31:16	UDID Word 4<31:0>																xxxx
		15:0																	xxxx
1850	UDID5	31:16	UDID Word 5<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 23-8: RESERVED REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	RESERVED1	31:16	Reserved Register 1<31:0>																0000
		15:0																	0000
0480	RESERVED2	31:16	Reserved Register 2<31:0>																0000
		15:0																	0000
2280	RESERVED3	31:16	Reserved Register 3<31:0>																0C00
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

26.2 AC Characteristics and Timing Parameters

FIGURE 26-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

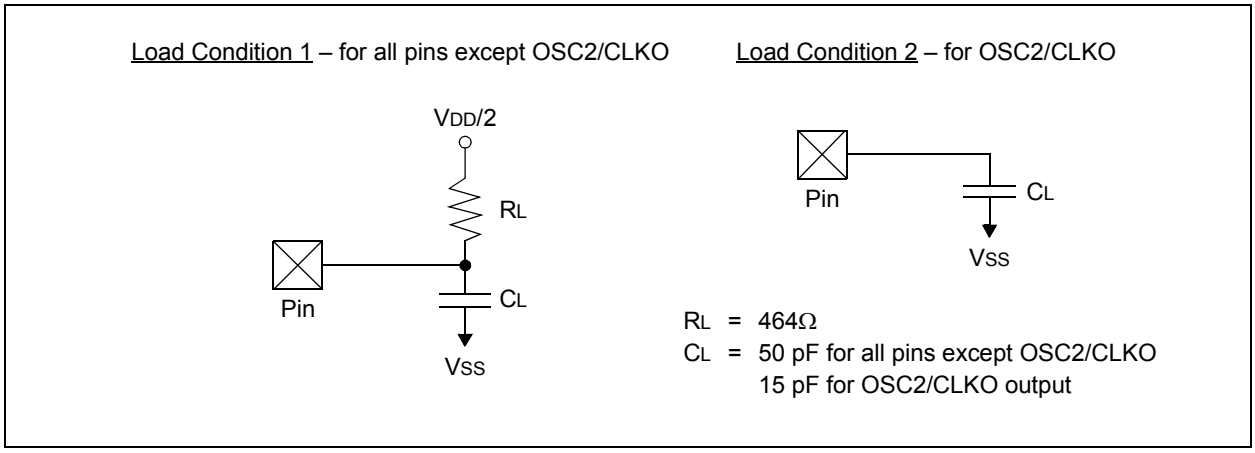
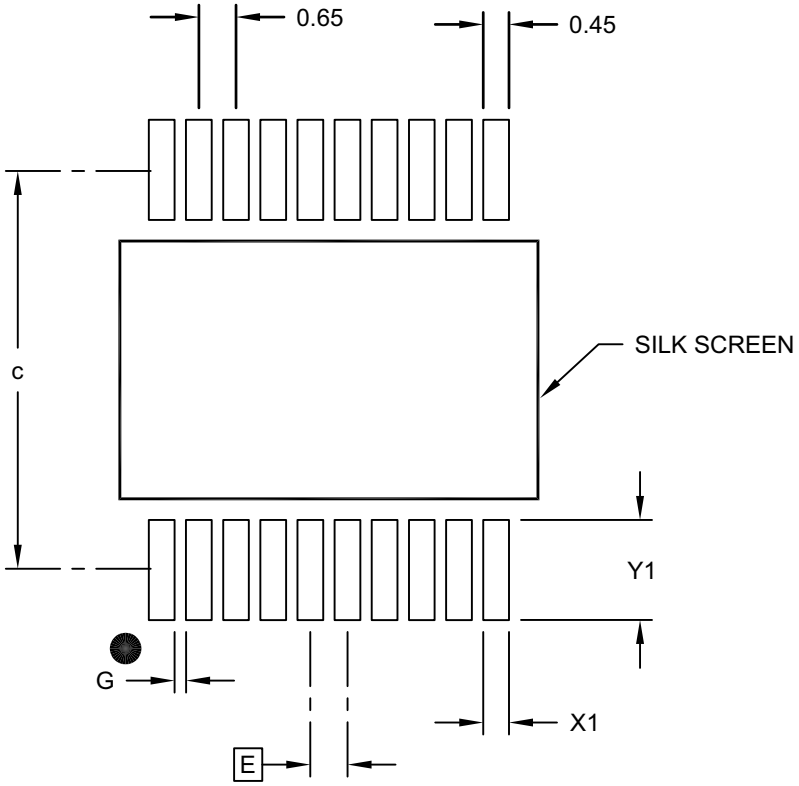


TABLE 26-16: CAPACITIVE LOADING CONDITIONS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
DO50	COSCO	OSC2/CLKO Pin	—	15	pF	In XT and HS modes when external clock is used to drive OSC1/CLKI
DO56	CIO	All I/O Pins and OSC2	—	50	pF	EC mode

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

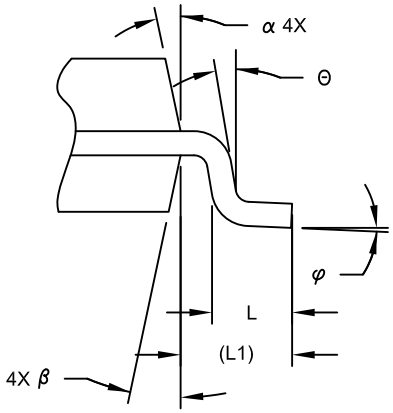
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

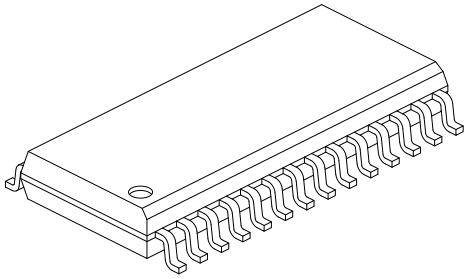
Microchip Technology Drawing No. C04-2072B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2