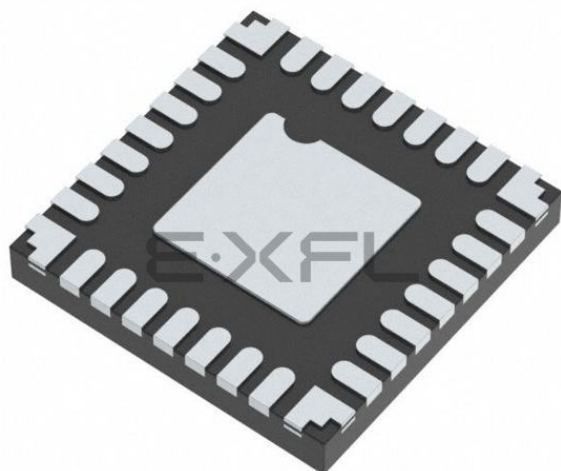




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I ² S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl028t-i-m6

PIC32MM0064GPL036 FAMILY

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
AN0	19	2	27	2	33	36	I	ANA	Analog-to-Digital Converter input channels
AN1	20	3	28	3	34	37	I	ANA	
AN2	1	4	1	4	35	38	I	ANA	
AN3	2	5	2	5	36	39	I	ANA	
AN4	3	6	3	6	1	1	I	ANA	
AN5	4	7	6	9	7	7	I	ANA	
AN6	5	8	7	10	8	8	I	ANA	
AN7	12	15	20	23	26	29	I	ANA	
AN8	13	16	21	24	27	30	I	ANA	
AN9	14	17	22	25	28	31	I	ANA	
AN10	15	18	23	26	29	32	I	ANA	
AN11	—	—	4	7	2	2	I	ANA	
AN12	—	—	—	—	3	3	I	ANA	
AN13	—	—	—	—	4	4	I	ANA	
AVDD	17	20	25	28	31	34	P	—	Analog modules power supply
AVss	16	19	24	27	30	33	P	—	Analog modules ground
C1INA	5	8	4	7	2	2	I	ANA	Comparator 1 Input A
C1INB	4	7	3	6	1	1	I	ANA	Comparator 1 Input B
C1INC	2	5	2	5	36	39	I	ANA	Comparator 1 Input C
C1IND	1	4	1	4	35	38	I	ANA	Comparator 1 Input D
C1OUT	14	17	22	25	28	31	O	DIG	Comparator 1 output
C2INA	2	5	2	5	36	39	I	ANA	Comparator 2 Input A
C2INB	1	4	1	4	35	38	I	ANA	Comparator 2 Input B
C2OUT	10	13	15	18	19	20	O	DIG	Comparator 2 output
CLKI	4	7	6	9	7	7	I	ST	External Clock input (EC mode)
CLKO	5	8	7	10	8	8	O	DIG	System clock output
CDAC1	14	17	22	25	28	31	O	ANA	Digital-to-Analog Converter output
FSYNC1	15	18	23	26	29	32	I/O	ST/DIG	SPI1 frame signal input or output
INT0	15	18	23	26	29	32	I	ST	External Interrupt 0
INT1	14	17	22	25	28	31	I	ST	External Interrupt 1
INT2	10	13	15	18	19	20	I	ST	External Interrupt 2
INT3	19	2	27	2	33	36	I	ST	External Interrupt 3
LVDIN	12	15	20	23	26	29	I	ANA	High/Low-Voltage Detect input
MCLR	18	1	26	1	32	35	I	ST	Master Clear (device Reset)
OCM1A	9	12	14	17	18	18	O	DIG	MCCP1 Output A
OCM1B	10	13	15	18	19	20	O	DIG	MCCP1 Output B
OCM1C	4	7	6	9	7	7	O	DIG	MCCP1 Output C
OCM1D	5	8	7	10	8	8	O	DIG	MCCP1 Output D
OCM1E	19	2	27	2	33	36	O	DIG	MCCP1 Output E
OCM1F	20	3	28	3	34	37	O	DIG	MCCP1 Output F
OSC1	4	7	6	9	7	7	—	—	Primary Oscillator crystal
OSC2	5	8	7	10	8	8	—	—	Primary Oscillator crystal

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. “CPU for Devices with MIPS32® microAptiv™ and M-Class Cores”** (DS60001192) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32® microAptiv™ UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32® microAptiv™ UC microprocessor core is the heart of the PIC32MM0064GPL036 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

3.1 Features

The PIC32MM0064GPL036 family processor core key features include:

- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
 - Multiply-add and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero and one detect instructions
 - WAIT instruction
 - Conditional move instructions
 - Vectored interrupts
 - Atomic interrupt enable/disable
 - One GPR shadow set to minimize latency of interrupts
 - Bit field manipulation instructions
- microMIPS™ Instruction Set:
 - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
 - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
 - Added seventeen new and thirty-five MIPS32® corresponding commonly used instructions in 16-bit opcode format.
 - Stack Pointer implicit in instruction.
 - MIPS32 assembly and ABI compatible.

- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
 - Configurable using high-performance multiplier array.
 - Maximum issue rate of one 32x16 multiply per clock.
 - Maximum issue rate of one 32x32 multiply every other clock.
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
 - No minimum frequency: 0 MHz.
 - Power-Down mode (triggered by WAIT instruction).
- EJTAG Debug/Profiling:
 - CPU control with start, stop and single stepping.
 - Software breakpoints via the SDBBP instruction.
 - Optional simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
 - PC and/or load/store address sampling for profiling.
 - Performance counters.
 - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0064GPL036 family processor core is shown in Figure 3-1.

PIC32MM0064GPL036 FAMILY

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x⁽¹⁾

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note 1: This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 10-8 **NOSC<2:0>**: New Oscillator Selection bits⁽³⁾

111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))

101 = Internal Low-Power RC (LPRC) Oscillator

100 = Secondary Oscillator (SOSC)

011 = Reserved

010 = Primary Oscillator (POSC) (XT, HS or EC)

001 = System PLL (SPLL)

000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>).

bit 7 **CLKLOCK**: Clock Selection Lock Enable bit

1 = Clock and PLL selections are locked

0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented**: Read as '0'

bit 4 **SLPEN**: Sleep Mode Enable bit

1 = Device will enter Sleep mode when a WAIT instruction is executed

0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF**: Clock Fail Detect bit

1 = FSCM has detected a clock failure

0 = No clock failure has been detected

bit 2 **Unimplemented**: Read as '0'

bit 1 **SOSCEN**: Secondary Oscillator (SOSC) Enable bit⁽⁴⁾

1 = Enables Secondary Oscillator

0 = Disables Secondary Oscillator

bit 0 **OSWEN**: Oscillator Switch Enable bit⁽²⁾

1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits

0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 “System Registers Write Protection”** for details.

2: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

3: The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.

4: The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

PIC32MM0064GPL036 FAMILY

NOTES:

PIC32MM0064GPL036 FAMILY

REGISTER 12-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	OETRIG	OSCNT<2:0>			—	OUTM<2:0> ⁽¹⁾		
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	POLACE	POLBDF ⁽¹⁾	PSSACE<1:0>		PSSBDF<1:0> ⁽¹⁾	
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DT<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **OETRIG:** PWM Dead-Time Select bit

1 = For Triggered mode (TRIGEN = 1), the module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 30-28 **OSCNT<2:0>:** One-Shot Event Count bits

Extends the duration of a one-shot trigger event by an additional n clock cycles (n+1 total cycles).

111 = 7 timer count periods (8 cycles total)

110 = 6 timer count periods (7 cycles total)

101 = 5 timer count periods (6 cycles total)

100 = 4 timer count periods (5 cycles total)

011 = 3 timer count periods (4 cycles total)

010 = 2 timer count periods (3 cycles total)

001 = 1 timer count period (2 cycles total)

000 = Does not extend the one-shot trigger event (the event takes 1 timer count period)

bit 27 **Unimplemented:** Read as '0'

bit 26-24 **OUTM<2:0>:** PWMx Output Mode Control bits⁽¹⁾

111 = Reserved

110 = Output Scan mode

101 = Brush DC Output mode, forward

100 = Brush DC Output mode, reverse

011 = Reserved

010 = Half-Bridge Output mode

001 = Push-Pull Output mode

000 = Steerable Single Output mode

bit 23-22 **Unimplemented:** Read as '0'

bit 21 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit

1 = Output pin polarity is active-low

0 = Output pin polarity is active-high

bit 20 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit⁽¹⁾

1 = Output pin polarity is active-low

0 = Output pin polarity is active-high

bit 19-18 **PSSACE<1:0>:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits

11 = Pins are driven active when a shutdown event occurs

10 = Pins are driven inactive when a shutdown event occurs

0x = Pins are in a high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in MCCP modules only.

REGISTER 12-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER (CONTINUED)

bit 17-16 **PSSBDF<1:0>**: PWMx Output Pins, OCxB, OCxD and OCxF, Shutdown State Control bits⁽¹⁾

11 = Pins are driven active when a shutdown event occurs

10 = Pins are driven inactive when a shutdown event occurs

0x = Pins are in a high-impedance state when a shutdown event occurs

bit 15-6 **Unimplemented**: Read as '0'

bit 5-0 **DT<5:0>**: PWM Dead-Time Select bits⁽¹⁾

111111 = Insert 63 dead-time delay periods between complementary output signals

111110 = Insert 62 dead-time delay periods between complementary output signals

...

000010 = Insert 2 dead-time delay periods between complementary output signals

000001 = Insert 1 dead-time delay period between complementary output signals

000000 = Dead-time logic is disabled

Note 1: These bits are implemented in MCCP modules only.

PIC32MM0064GPL036 FAMILY

NOTES:

PIC32MM0064GPL036 FAMILY

REGISTER 15-4: RTCTIME/ALMTIME: RTCC/ALARM TIME REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	HRTEN<2:0>			HRTONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SECTEN<3:0>				SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-28 **HRTEN<2:0>**: Binary Coded Decimal Value of Hours 10-Digit bits

Contains a value from 0 to 2.

bit 27-24 **HRTONE<3:0>**: Binary Coded Decimal Value of Hours 1-Digit bits

Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>**: Binary Coded Decimal Value of Minutes 10-Digit bits

Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>**: Binary Coded Decimal Value of Minutes 1-Digit bits

Contains a value from 0 to 9.

bit 15-12 **SECTEN<3:0>**: Binary Coded Decimal Value of Seconds 10-Digit bits

Contains a value from 0 to 5.

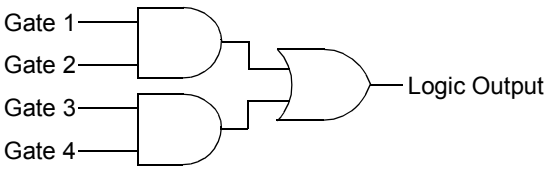
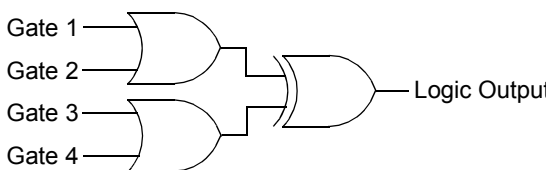
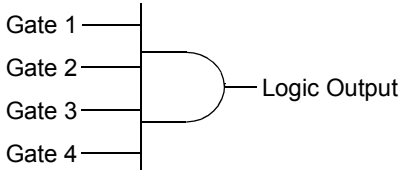
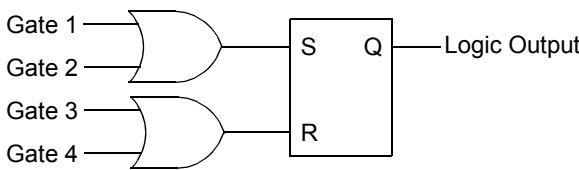
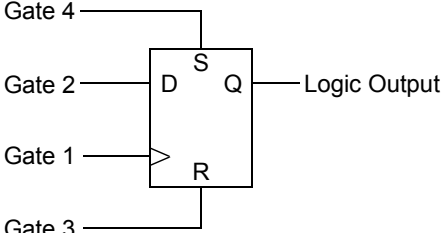
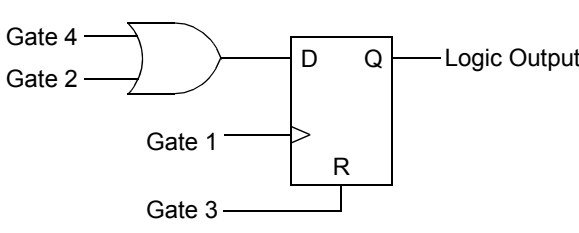
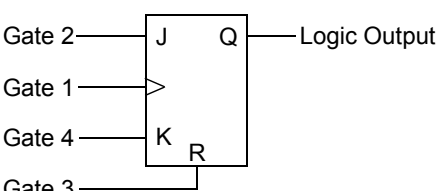
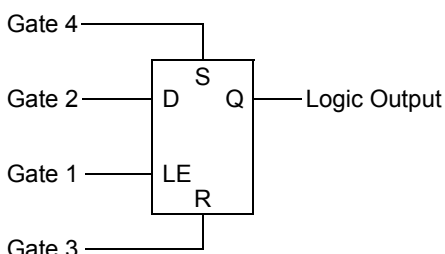
bit 11-8 **SECONE<3:0>**: Binary Coded Decimal Value of Seconds 1-Digit bits

Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

PIC32MM0064GPL036 FAMILY

FIGURE 18-2: CLCx LOGIC FUNCTION COMBINATORIAL OPTIONS

AND – OR  MODE<2:0> = 000	OR – XOR  MODE<2:0> = 001
4-Input AND  MODE<2:0> = 010	S-R Latch  MODE<2:0> = 011
1-Input D Flip-Flop with S and R  MODE<2:0> = 100	2-Input D Flip-Flop with R  MODE<2:0> = 101
J-K Flip-Flop with R  MODE<2:0> = 110	1-Input Transparent Latch with S and R  MODE<2:0> = 111

REGISTER 18-1: CLCxCON: CLCx CONTROL REGISTER (CONTINUED)

- bit 5 **LCPOL:** CLCx Output Polarity Control bit
 1 = The output of the module is inverted
 0 = The output of the module is not inverted
- bit 4-3 **Unimplemented:** Read as '0'
- bit 2-0 **MODE<2:0>:** CLCx Mode bits
 111 = Cell is a 1-input transparent latch with S and R
 110 = Cell is a JK flip-flop with R
 101 = Cell is a 2-input D flip-flop with R
 100 = Cell is a 1-input D flip-flop with S and R
 011 = Cell is an SR latch
 010 = Cell is a 4-input AND
 001 = Cell is an OR-XOR
 000 = Cell is a AND-OR

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

PIC32MM0064GPL036 FAMILY

NOTES:

PIC32MM0064GPL036 FAMILY

REGISTER 23-1: FDEVOPT/AFDEVOPT: DEVICE OPTIONS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	r-1	r-1	r-1
	—	—	—	—	SOSCHP	—	—	—

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **USERID<15:0>**: User ID bits (2 bytes which can be programmed to any value)

bit 15-4 **Reserved**: Program as '1'

bit 3 **SOSCHP**: Secondary Oscillator (SOSC) High-Power Enable bit
 1 = SOSC operates in Normal Power mode
 0 = SOSC operates in High-Power mode

bit 2-0 **Reserved**: Program as '1'

PIC32MM0064GPL036 FAMILY

REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	SOSCSEL	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	IESO	SOSCEN	—	PLLSRC	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 31-16 **Reserved:** Program as '1'
- bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled
- bit 13 **Reserved:** Program as '1'
- bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
 1 = Crystal is used (RA4 and RB4 pins are controlled by SOSC)
 0 = External clock is connected to the SOSCO pin (RA4 and RB4 pins are controlled by I/O PORTx registers)
- bit 11 **Reserved:** Program as '1'
- bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
 1 = OSC2/CLKO pin operates as normal I/O
 0 = System clock is connected to the OSC2/CLKO pin
- bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
 11 = Primary Oscillator is disabled
 10 = HS Oscillator mode is selected
 01 = XT Oscillator mode is selected
 00 = External Clock (EC) mode is selected
- bit 7 **IESO:** Two-Speed Start-up Enable bit
 1 = Two-Speed Start-up is enabled
 0 = Two-Speed Start-up is disabled
- bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
 1 = Secondary Oscillator is enabled
 0 = Secondary Oscillator is disabled
- bit 5 **Reserved:** Program as '1'
- bit 4 **PLLSRC:** System PLL Input Clock Selection bit
 1 = FRC oscillator is selected as the PLL reference input on a device Reset
 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset
- bit 3 **Reserved:** Program as '1'

PIC32MM0064GPL036 FAMILY

REGISTER 23-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	r-0	U-0	r-0	r-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EXECADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-y	U-0	r-1	r-1
	—	—	—	—	JTAGEN	—	—	—

Legend:	r = Reserved bit	y = Value set from Configuration bits on Reset
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **Reserved:** Must be written as '0'

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **Reserved:** Must be written as '0'

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits

11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)

•
•
•

00000010 = RAM program space starts at the 2-Kbyte boundary (from 0xA0000800)

00000001 = RAM program space starts at the 1-Kbyte boundary (from 0xA0000400)

00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit

1 = JTAG port is enabled

0 = JTAG port is disabled

The Reset value of this bit is the value of the JTAGEN (FICD<2>) Configuration bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Must be written as '1'

TABLE 23-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

PIC32MM0064GPL036 FAMILY

REGISTER 23-10: ANCFG: BAND GAP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS, HC	R/W-0, HS, HC	U-0
	—	—	—	—	—	VBGADC	VBGCMP	—

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **VBGADC:** ADC Band Gap Enable bit

1 = ADC band gap is enabled

0 = ADC band gap is disabled

bit 1 **VBGCMP:** Comparator Band Gap Enable bit

1 = Comparator band gap is enabled

0 = Comparator band gap is disabled

bit 0 **Unimplemented:** Read as '0'

PIC32MM0064GPL036 FAMILY

FIGURE 26-4: CLKO AND I/O TIMING CHARACTERISTICS

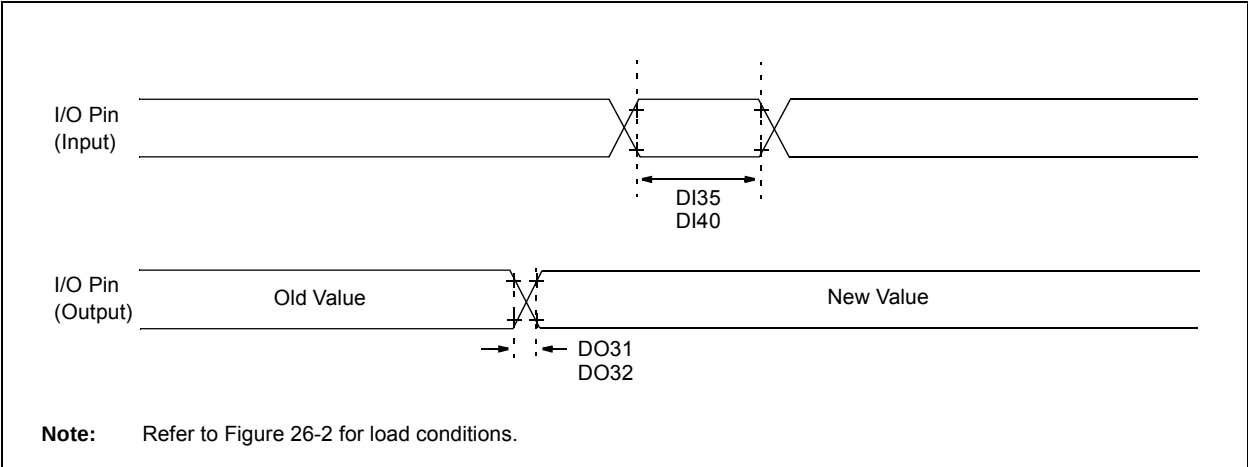


TABLE 26-21: CLKO AND I/O TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units
DO31	TioR	Port Output Rise Time	—	10	25	ns
DO32	TioF	Port Output Fall Time	—	10	25	ns
DI35	TINP	INTx Input Pin High or Low Time	10	—	—	ns
DI40	TRBP	CNx Input Pin High or Low Time	10	—	—	ns

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

PIC32MM0064GPL036 FAMILY

INDEX

A

AC Characteristics

10-Bit ADC Accuracy and Conversion Requirements	230
12-Bit ADC Accuracy and Conversion Requirements	229
ADC Inputs Specifications	229
and Timing Parameters	217
Capacitive Loading on Output Pins	217
CLKO and I/O Timing Requirements	220
EJTAG Requirements	231
External Clock Timing Requirements	218
Internal Oscillator Accuracy	219
Internal Oscillator Start-up Time	219
Load Conditions for Device Timing	217
MCCP/SCCP Input Capture x Mode Requirements	224
MCCP/SCCP Output Compare x Mode Requirements	224
MCCP/SCCP PWM Mode Requirements	225
MCCP/SCCP Timer1 External Clock Timing	222
MCCP/SCCP Timing Requirements	223
PLL Clock Timing Specifications	219
Reset, Brown-out Reset and Sleep Modes Timing Specifications	221
SPIx Master Mode Requirements	227
SPIx Module Slave Mode Timing Requirements	228

ADC Converter

Control Registers	134
Introduction	133

Assembler

MPASM Assembler	200
-----------------------	-----

B

Band Gap Voltage Reference	182
----------------------------------	-----

Block Diagrams

ADC Module	133
CDAC Module	169
CLCx Input Source Selection	153
CLCx Logic Function Combinatorial Options	152
CLCx Module	151
CPU Exceptions and Interrupt Controller	51
CRC Module	147
Dual Comparator Module	163
High/Low-Voltage Detect (HLVD)	173
MCCP/SCCP Module	96
MCLR Pin Connections	20
Microprocessor Core	24
Multiplexing Remappable Output for RP1	81
Oscillator Circuit Placement	21
Oscillator System	66
PIC32MM0064GPL036 Family	13
Recommended Minimum Connection	20
Remappable Input Example for U2RX	80
Reset System	45
RTCC Module	123
SPI/I ² S Module	109
Timer1 Module	87
Typical Shared Port Structure	77
UARTx Module	117
Watchdog Timer (WDT)	91

C

C Compilers

MPLAB XC Compilers	200
--------------------------	-----

Capture/Compare/PWM/Timer Modules

(MCCP, SCCP)	95
--------------------	----

CLC

Control Registers	154
-------------------------	-----

CLR, SET and INV Registers	78
----------------------------------	----

Code Examples

UART2 RX Input Assignment to RP9/RB14 Pin	80
---	----

UART2 TX Output Assignment to RP13/RB13 Pin	81
---	----

Code Execution from RAM	181
-------------------------------	-----

Comparator	163
------------------	-----

Configurable Logic Cell (CLC)	151
-------------------------------------	-----

Configurable Logic Cell. See CLC.

Configuration Bits	181
--------------------------	-----

Control Digital-to-Analog Converter (CDAC)	169
--	-----

Control Digital-to-Analog Converter. See CDAC.

CP0 Register 16, Select 1)	30
----------------------------------	----

CP0 Register 16, Select 3)	31
----------------------------------	----

CP0 Register 16, Select 5)	32
----------------------------------	----

CPU

Architecture Overview	25
-----------------------------	----

Coprocessor 0 Registers	27
-------------------------------	----

Core Exception Types	52
----------------------------	----

EJTAG Debug Support	28
---------------------------	----

Power Management	28
------------------------	----

CPU Module	23
------------------	----

Customer Change Notification Service	262
--	-----

Customer Notification Service	262
-------------------------------------	-----

Customer Support	262
------------------------	-----

Cyclic Redundancy Check. See CRC.

D

DC Characteristics

Comparator Specifications	216
---------------------------------	-----

High/Low-Voltage Detect	215
-------------------------------	-----

I/O Pin Input Injection Current Specifications	213
--	-----

I/O Pin Input Specifications	212
------------------------------------	-----

I/O Pin Output Specifications	214
-------------------------------------	-----

Idle Current (I _{IDLE})	209
---	-----

Incremental Peripheral Δ Current (BOR, WDT, HLVD, RTCC, ADC, FRC, PLL, DAC, LPBOR, CMP)	211
--	-----

Internal Voltage Regulator Specifications	215
---	-----

Operating Current (I _{DD})	208
--	-----

Operating Voltage Specifications	207
--	-----

Power-Down Current (I _{PD})	210
---	-----

Program Flash Memory Specifications	214
---	-----

Thermal Operating Conditions	206
------------------------------------	-----

Voltage Reference Specifications	216
--	-----

Demo/Development Boards, Evaluation and

Starter Kits	202
--------------------	-----

Development Support	199
---------------------------	-----

Third-Party Tools	202
-------------------------	-----

Device IDs	181
------------------	-----

E

Electrical Characteristics	205
----------------------------------	-----

Absolute Maximum Ratings	205
--------------------------------	-----

V/F Graph (Industrial)	206
------------------------------	-----

Errata	10
--------------	----

PIC32MM0064GPL036 FAMILY

CCPxCON3 (Capture/Compare/PWMx Control 3)	104
CCPxSTAT (Capture/Compare/PWMx Status)	106
CFGCON (Configuration Control)	193
CLCxCON (CLCx Control)	156
CLCxGLS (CLCx Gate Logic Input Select)	160
CLCxSEL (CLCx Input MUX Select)	158
CLKSTAT (Clock Status)	74
CMSTAT (Comparator Status)	165
CMxCON (Comparator x Control)	166
CNCONx (Change Notification Control for PORTx)	86
CONFIG (CP0 Register 16, Select 0)	29
CONFIG1 (Configuration Register 1)	30
CONFIG3 (Configuration Register 3)	31
CONFIG5 (Configuration Register 5)	32
CRCCON (CRC Control)	149
CRCXOR (CRC XOR)	150
DAC1CON (CDAC Control)	171
DEVID (Device ID)	194
FDEVOPT/AFDEVOPT (Device Options Configuration)	185
FICD/AFICD (ICD/Debug Configuration)	186
FOSCSEL/AFOSCSEL (Oscillator Selection Configuration)	190
FPOR/AFPOR (Power-up Settings Configuration)	187
FSEC/AFSEC (Code-Protect Configuration)	191
FWDT/AFWDT (Watchdog Timer Configuration)	188
HLVDCON (High/Low Voltage Detect Control)	175
IECx (Interrupt Enable Control x)	62
IFSx (Interrupt Flag Status x)	62
INTCON (Interrupt Control)	58
INTSTAT (Interrupt Status)	61
IPCx (Interrupt Priority Control x)	63
IPTM (Interrupt Proximity Timer)	61
NVMADDR (NVM Flash Address)	41
NVMBWP (NVM Boot Flash (Page) Write-Protect)	44
NVMCON (NVM Programming Control)	39
NVMDATAx (NVM Flash Data x)	42
NVMKEY (NVM Programming Unlock)	41
NVMPPW (NVM Program Flash Write-Protect)	43
NVMSRCADDR (NVM Source Data Address)	42
OSCCON (Oscillator Control)	68
OSCTUN (FRC Tuning)	75
PRISS (Priority Shadow Select)	59
PWRCON (Power Control)	50
RCON (Reset Control)	47
REFO1CON (Reference Oscillator Control)	71
REFO1TRIM (Reference Oscillator Trim)	73
RNMICON (Non-Maskable Interrupt (NMI) Control)	49
RSWRST (Software Reset)	48
RTCCON1 (RTCC Control 1)	125
RTCCON2 (RTCC Control 2)	127

RTCDATE (RTCC Date).....	130
RTCSTAT (RTCC Status Register)	128
RTCTIME/ALMTIME (RTCC/Alarm Time).....	129
SPIxCON (SPIx Control)	111
SPIxCON2 (SPIx Control 2)	114
SPIxSTAT (SPIx Status).....	115
SPLLCON (System PLL Control)	70
SYSKEY (System Unlock).....	194
T1CON (Timer1 (Type A) Control)	89
UxMODE (UARTx Mode)	119
UxSTA (UARTx Status and Control)	121
WDTCON (Watchdog Timer Control)	93
Resets	45
Brown-out Reset (BOR).....	45
Configuration Mismatch Reset (CMR).....	45
Master Clear Reset Pin (MCLR).....	45
Power-on Reset (POR).....	45
Software Reset (SWR)	45
Watchdog Timer Reset (WDTR).....	45
Revision History.....	257

S

Serial Peripheral Interface (SPI).....	109
Serial Peripheral Interface. <i>See</i> SPI.	
Special Features.....	181

T

Timer1 Module	87
Timing Diagrams	
CLKO and I/O Characteristics	220
EJTAG Characteristics	231
External Clock	218
MCCP/SCCP Input Capture x Mode	224
MCCP/SCCP Output Compare x Mode	224
MCCP/SCCP PWMx Mode Characteristics	225
MCCP/SCCP Timerx External Clock Timing	223
SPIx Master Mode (CKE = 0)	226
SPIx Master Mode (CKE = 1)	226
SPIx Slave Mode (CKE = 0)	227
SPIx Slave Mode (CKE = 1)	228
Timer1 External Clock Characteristics	222

U

UART	117
Unique Device Identifier (UDID)	182
Universal Asynchronous Receiver Transmitter. <i>See</i> UART.	

W

Watchdog Timer (WDT).....	91
Write Protection	
System Registers	181
WWW Address	262
WWW, On-Line Support	10