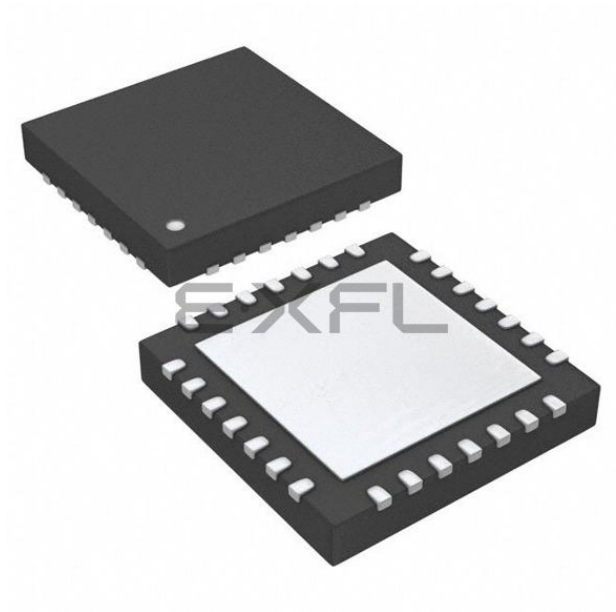
Microchip Technology - PIC32MM0032GPL028T-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl028t-i-ml

7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note:	This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupts"** (DS60001108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM

PIC32MM0064GPL036 family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The PIC32MM0064GPL036 family device interrupt module includes the following features:

- Single Vector or Multivector mode Operation
- Five External Interrupts with Edge Polarity Control
- Interrupt Proximity Timer
- Module Freeze in Debug mode
- Seven User-Selectable Priority Levels for each Vector
- Four User-Selectable Subpriority Levels within each Priority
- One Shadow Register Set that can be used for any Priority Level, Eliminating Software Context Switching and Reducing Interrupt Latency
- Software can Generate any Interrupt
- User-Configurable Interrupt Vectors' Offset and Vector Table Location

Figure 7-1 shows the block diagram for the interrupt controller and CPU exceptions.

FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM

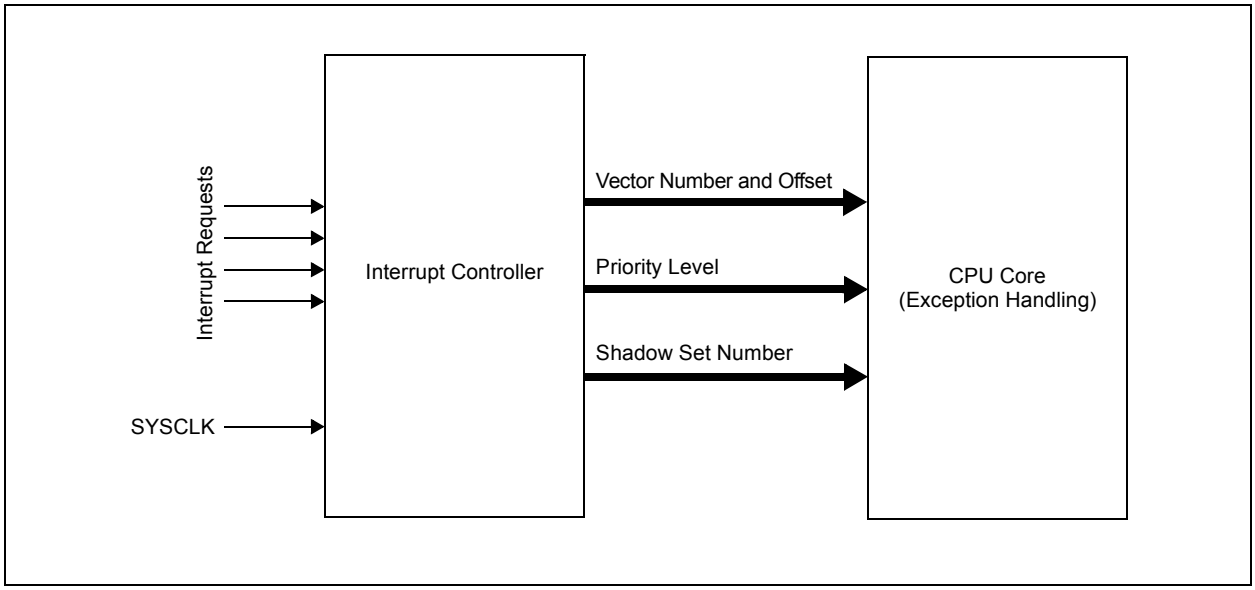


TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.	EBASE + 0x180	CU, EXL	—	CpU (0x0B)	_general_exception_handler
RI	Execution of a reserved instruction.	EBASE + 0x180	EXL	—	RI (0x0A)	_general_exception_handler
Ov	Execution of an arithmetic instruction that overflowed.	EBASE + 0x180	EXL	—	Ov (0x0C)	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE + 0x180	EXL	—	Tr (0x0D)	_general_exception_handler
DDBL	EJTAG data address break (address only) or EJTAG data value break on load (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
DDBS	EJTAG data address break (address only) or EJTAG data value break on store (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
AdES	Store address alignment error.	EBASE + 0x180	EXL	—	ADES (0x05)	_general_exception_handler
DBE	Load or store bus error.	EBASE + 0x180	EXL	—	DBE (0x07)	_general_exception_handler
CBrk	EJTAG complex breakpoint.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIBImpr, DDBLImpr and/or DDBSImpr	—	—
Lowest Priority						

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F1C0	IPC8	31:16	—	—	—	—	—	—	—	—	—	—	—	CCT3IP<2:0>			CCT3IS<1:0>		0000
		15:0	—	—	—	CCP3IP<2:0>			CCP3IS<1:0>		—	—	—	CCT2IP<2:0>			CCT2IS<1:0>		0000
F1D0	IPC9	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
		15:0	—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		—	—	—	—	—	—	—	—	0000
F1E0	IPC10	31:16	—	—	—	—	—	—	—	—	—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
		15:0	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
F1F0	IPC11	31:16	—	—	—	CPCIP<2:0>			CPCIS<1:0>		—	—	—	NVMIP<2:0>			NVMIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 20-pin devices.

9.0 I/O PORTS

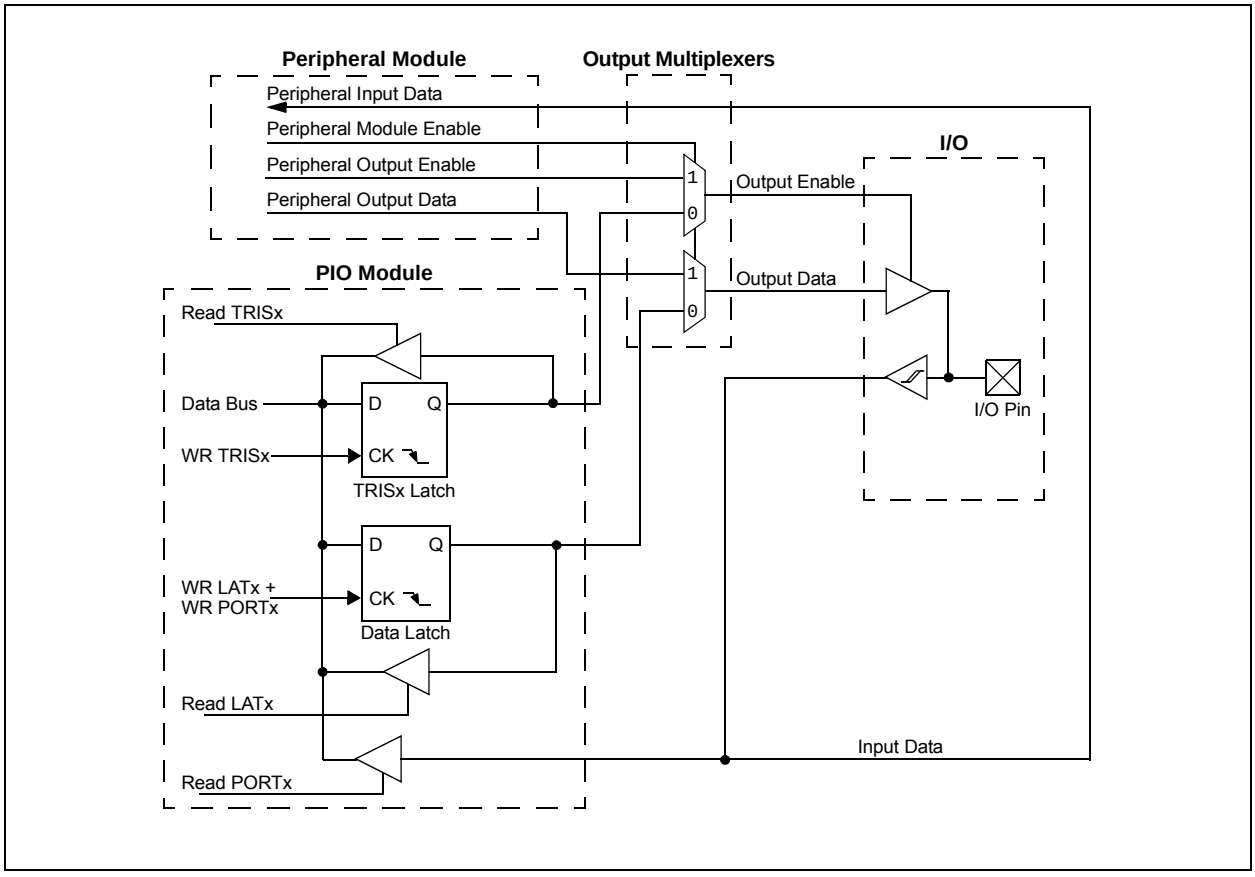
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

Many of the device pins are shared among the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. Some pins in the devices are 5V tolerant pins. Some of the key features of the I/O ports are:

- Individual Output Pin Open-Drain Enable/Disable
- Individual Input Pin Weak Pull-up and Pull-Down
- Monitor Selective Inputs and Generate Interrupt when Change-in-Pin State is Detected
- Operation during Sleep and Idle modes
- Fast Bit Manipulation using the CLR, SET and INV registers

Figure 9-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 9-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



REGISTER 9-1: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER (x = A-C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	CNSTYLE	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notification (CN) Control On bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit
1 = Edge style (detects edge transitions, CNFx bits are used for a Change Notice event)
0 = Mismatch style (detects change from last PORTx read, CNSTATx bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 7-6 **TMRPS<1:0>:** CCPx Time Base Prescale Select bits
11 = 1:64 prescaler
10 = 1:16 prescaler
01 = 1:4 prescaler
00 = 1:1 prescaler

bit 5 **T32:** 32-Bit Time Base Select bit
1 = 32-bit time base for timer, single edge output compare or input capture function
0 = 16-bit time base for timer, single edge output compare or input capture function

bit 4 **CCSEL:** Capture/Compare Mode Select bit
1 = Input Capture mode
0 = Output Compare/PWM or Timer mode (exact function is selected by the MOD<3:0> bits)

bit 3-0 **MOD<3:0>:** CCPx Mode Select bits
CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)
CCSEL = 0 (Output Compare modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode
0110 = Center-Aligned Pulse Compare mode, buffered
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode: Toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode: Drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode: Drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode: Output functions are disabled

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

13.1 SPI Control Registers

TABLE 13-1: SPI1 AND SPI2 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8080	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
8090	SPI1STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
80A0	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
80B0	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
80C0	SPI1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUDMONO	—	AUDMOD<1:0>		0000
8100	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
8110	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
8120	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
8130	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
8140	SPI2CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUDMONO	—	AUDMOD<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table, except SPIxBUF, have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

15.1 RTCC Control Registers

TABLE 15-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	RTCCON1	31:16	ALRMEN	CHIME	—	—	AMASK<3:0>				ALMRPT<7:0>								0000
		15:0	ON	—	—	—	WRLOCK	—	—	—	RTCOE	OUTSEL<2:0>			—	—	—	—	0000
0010	RTCCON2	31:16	DIV<15:0>																0000
		15:0	FDIV<4:0>					—	—	—	—	—	—	—	—	—	CLKSEL<1:0>		0000
0030	RTCSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC	0000
0040	RTCTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0050	RTCDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000
0060	ALMTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0070	ALMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 16-7: AD1CHIT: ADC COMPARE HIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CHH<13:8>(1,2)					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-0 **CHH<13:0>:** ADC Compare Hit bits(1,2)

If CM<1:0> = 11:

1 = ADC Result Buffer x has been written with data or a match has occurred

0 = ADC Result Buffer x has not been written with data

For All Other Values of CM<1:0>:

1 = A match has occurred on ADC Result Channel n

0 = No match has occurred on ADC Result Channel n

Note 1: The CHH<13:11> bits are not implemented in 20-pin devices.

2: The CHH<13:12> bits are not implemented in 28-pin devices.

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 1
0 = The Data Source 2 signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 1
0 = The Data Source 1 signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	SOSCSEL	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	IESO	SOSCEN	—	PLLSRC	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
- 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
- 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
- 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
- 1 = Crystal is used (RA4 and RB4 pins are controlled by SOSC)
- 0 = External clock is connected to the SOSCO pin (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
- 1 = OSC2/CLKO pin operates as normal I/O
- 0 = System clock is connected to the OSC2/CLKO pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit
- 1 = Two-Speed Start-up is enabled
- 0 = Two-Speed Start-up is disabled

bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Secondary Oscillator is enabled
- 0 = Secondary Oscillator is disabled

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit
- 1 = FRC oscillator is selected as the PLL reference input on a device Reset
- 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

REGISTER 23-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	r-0	U-0	r-0	r-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EXECADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-y	U-0	r-1	r-1
	—	—	—	—	JTAGEN	—	—	—

Legend:	r = Reserved bit	y = Value set from Configuration bits on Reset
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **Reserved:** Must be written as '0'

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **Reserved:** Must be written as '0'

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits

11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)
•
•
•
00000010 = RAM program space starts at the 2-Kbyte boundary (from 0xA0000800)
00000001 = RAM program space starts at the 1-Kbyte boundary (from 0xA0000400)
00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit

1 = JTAG port is enabled
0 = JTAG port is disabled
The Reset value of this bit is the value of the JTAGEN (FICD<2>) Configuration bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Must be written as '1'

24.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

24.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

24.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

24.9 PICkit 3 In-Circuit Debugger/ Programmer

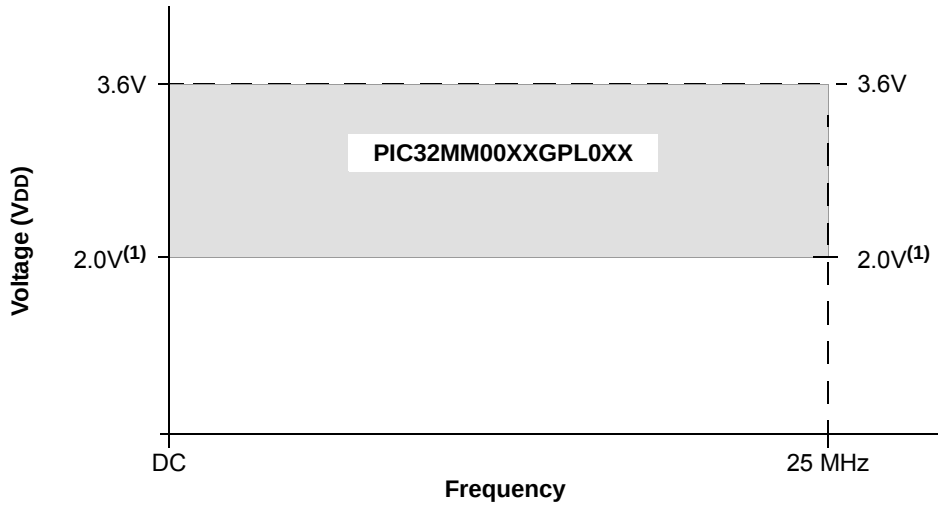
The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

24.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

26.1 DC Characteristics

FIGURE 26-1: PIC32MM0064GPL036 FAMILY VOLTAGE-FREQUENCY GRAPH



Note 1: Lower operating boundary is 2.0V or VBOR when BOR is enabled.

TABLE 26-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
PIC32MM00XXGPL0XX:					
Operating Junction Temperature Range	TJ	-40	—	+105	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: PI/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 26-2: PACKAGE THERMAL RESISTANCE(1)

Package	Symbol	Typ	Unit
20-Pin SSOP	θJA	87.3	°C/W
20-Pin QFN	θJA	43.0	°C/W
28-Pin SPDIP	θJA	60.0	°C/W
28-Pin SSOP	θJA	71.0	°C/W
28-Pin SOIC	θJA	69.7	°C/W
28-Pin UQFN	θJA	27.5	°C/W
28-Pin QFN	θJA	20.0	°C/W
36-Pin VQFN	θJA	31.1	°C/W
40-Pin UQFN	θJA	41.0	°C/W

Note 1: Junction to ambient thermal resistance; Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 26-4: OPERATING CURRENT (I_{DD})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC19	0.45	0.65	mA	2.0V	FSYS = 1 MHz
	0.45	0.65	mA	3.3V	
DC23	2.5	3.5	mA	2.0V	FSYS = 8 MHz
	2.5	3.5	mA	3.3V	
DC24	7.0	9.2	mA	2.0V	FSYS = 25 MHz
	7.0	9.2	mA	3.3V	
DC25	0.26	0.35	mA	2.0V	FSYS = 32 kHz
	0.26	0.35	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IDD current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins (except OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- NOP instructions are executed

TABLE 26-6: POWER-DOWN CURRENT (I_{PD})(2)

Parameter No.	Typical(1)	Max	Units	Operating Temperature	VDD	Conditions
DC60	134	198	µA	-40°C	2.0V	Sleep with active main voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) =0)
	136	208	µA	+25°C		
	141	217	µA	+85°C		
	139	209	µA	-40°C	3.3V	
	141	217	µA	+25°C		
	143	231	µA	+85°C		
DC61	4.3	11.7	µA	-40°C	2.0V	Sleep with main voltage regulator in Standby mode (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 0)
	5.1	15.6	µA	+25°C		
	11.4	34.3	µA	+85°C		
	6.1	16.8	µA	-40°C	3.3V	
	6.9	20.1	µA	+25°C		
	12.7	36.0	µA	+85°C		
DC62	2.3	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	2.7	—	µA	+25°C		
	5.2	—	µA	+85°C		
	2.3	—	µA	-40°C	3.3V	
	2.7	—	µA	+25°C		
	5.4	—	µA	+85°C		
DC63	0.28	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	0.44	—	µA	+25°C		
	2.52	—	µA	+85°C		
	0.29	—	µA	-40°C	3.3V	
	0.44	—	µA	+25°C		
	2.62	—	µA	+85°C		

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with:

- Oscillator is configured in FRC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 000)
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

TABLE 26-18: PLL CLOCK TIMING SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**
OS50	FPLLI	PLL Input Frequency Range(1)	2	24	MHz
OS54	FPLLO	PLL Output Frequency Range(1)	16	96	MHz
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	24	µs
OS53	DCLK	CLKO Stability (Jitter)	-0.12	0.12	%

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 26-19: INTERNAL OSCILLATOR ACCURACY(1)

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
F20	FRC Accuracy @ 8 MHz	-3	—	3	%
F21	LPRC @ 32 kHz	-20	—	20	%
F22	FRC Tune Step-Size (in OSCTUN register)	—	0.05	—	%/Bit

Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

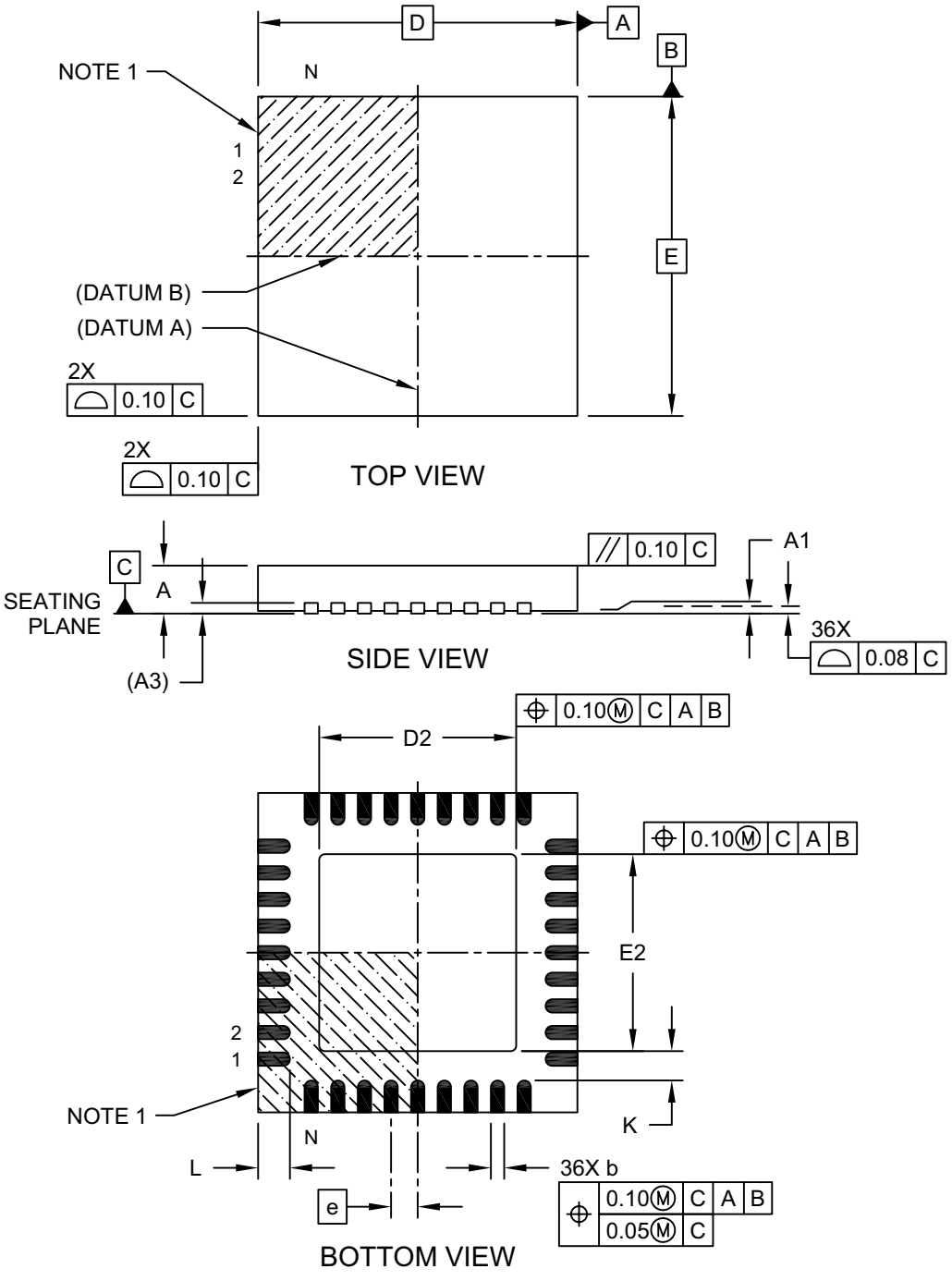
2: Data in the "Typ" column is 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-20: INTERNAL OSCILLATOR START-UP TIME

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)				
Param No.	**Symbol**	**Characteristic**	**Max**	**Units**
FR0	TFRC	FRC Oscillator Start-up Time	2	µs
FR1	TLPRC	Low-Power RC Oscillator Start-up Time	70	µs

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

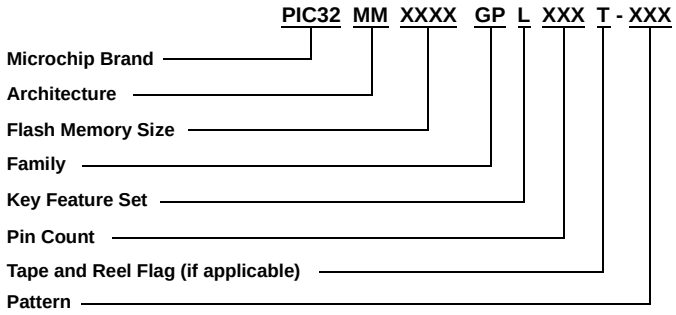
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture	MM	= MIPS32® microAptiv™ UC CPU Core
Flash Memory Size	0016 0032 0064	= 16 Kbytes = 32 Kbytes = 64 Kbytes
Family	GP	= General Purpose Family
Key Feature	L	= Up to 25 MHz operating frequency with basic peripheral set of 2 UART and 2 SPI modules
Pin Count	020 028 036	= 20-pin = 28-pin = 36/40-pin
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES	= Engineering Sample

Example:

PIC32MM0064GPL036-I/M2: PIC32 General Purpose Device with MIPS32® microAptiv™ UC Core, 64-Kbyte Program Memory, 36-Pin Package.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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