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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-SQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl036-e-m2

NOTES:

The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information is available by accessing the CP0 registers listed in Table 3-2.

REGISTER 5-2: NVMKEY: NVM PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** NVM Unlock Register bits
These bits are write-only and read as '0' on any read.

REGISTER 5-3: NVMADDR: NVM FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** NVM Flash Address bits

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<10:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<7:0> are ignored).
Double-Word Program	Address identifies the double-word (64-bit) to program (NVMADDR<1:0> bits are ignored).

6.0 RESETS

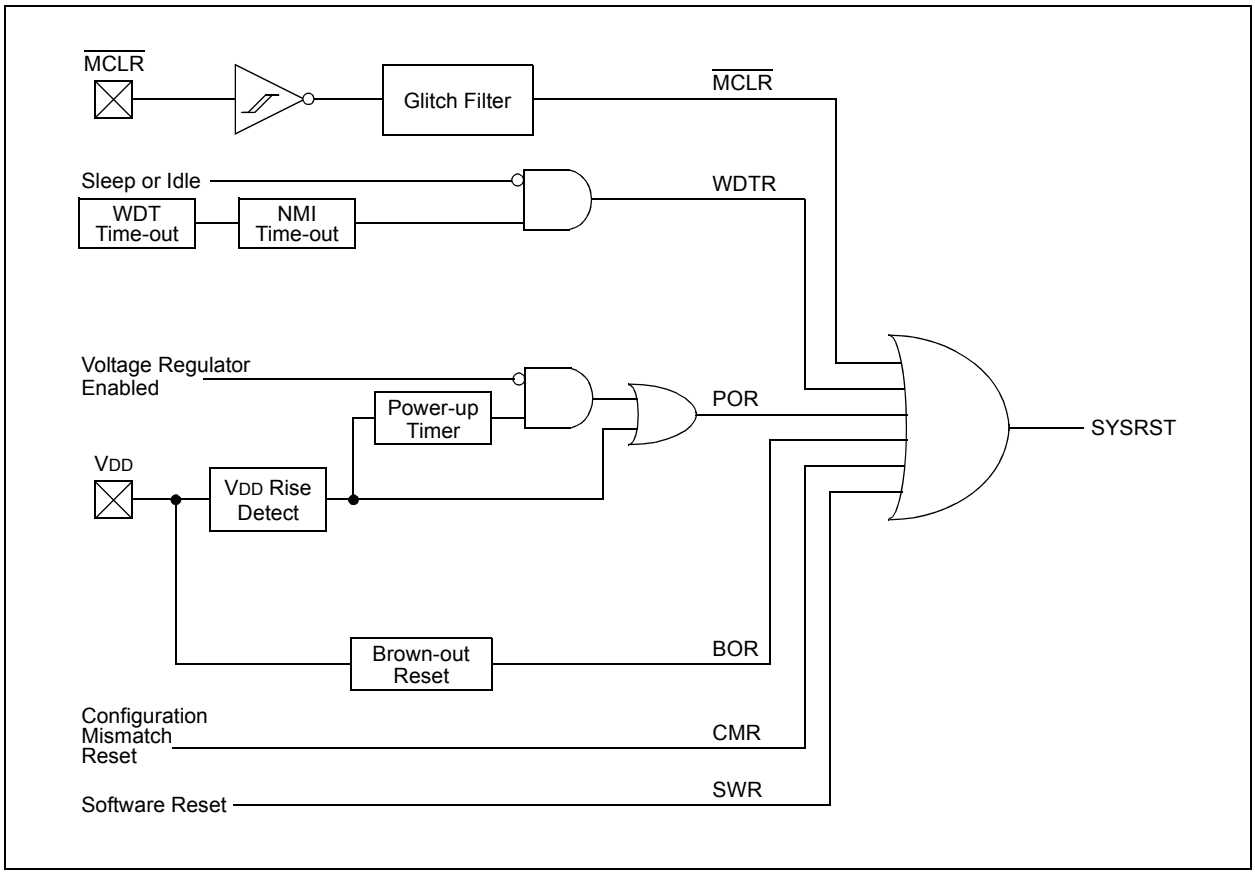
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset Pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 3 **SLEEP:** Wake from Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake from Idle Flag bit(2)
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear bits in this register to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep mode.

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enables Software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 23.4 "System Registers Write Protection"** for details.
2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

REGISTER 11-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R/W-y
	CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on Reset		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to this location using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RWDTPS<4:0> Configuration bits in FWDT.

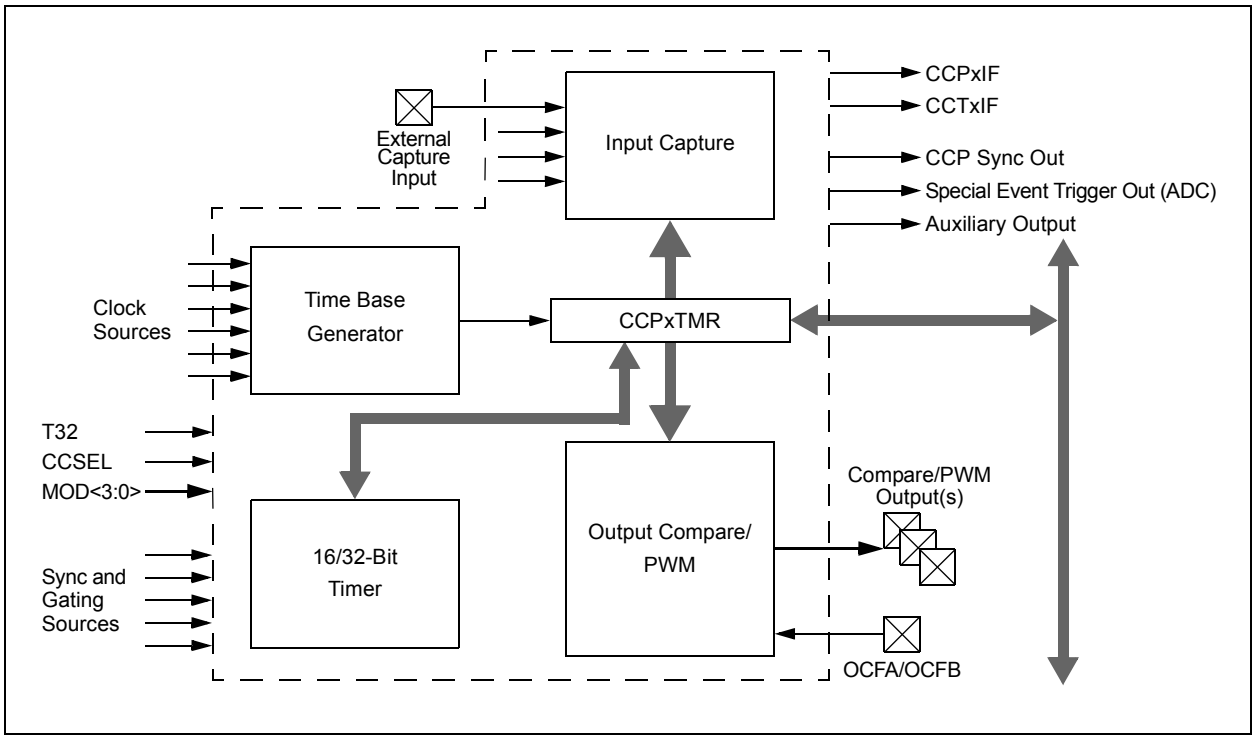
bit 7-6 **CLKSEL<1:0>:** Shadow Copy of Watchdog Timer Clock Selection Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RCLKSEL<1:0> Configuration bits in FWDT.

bit 5-1 **SLPDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Sleep/Idle Mode from Configuration bits
On Reset, these bits are set to the values of the SWDTPS<4:0> Configuration bits in FWDT.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
On Reset, this bit is set to the value of the WINDIS Configuration bit in FWDT.
1 = Windowed mode is enabled
0 = Windowed mode is disabled

Note 1: This bit only has control when FWDTEN (FWDT<15>) = 0.

FIGURE 12-1: MCCP/SCCP CONCEPTUAL BLOCK DIAGRAM



12.2 Registers

Each MCCP/SCCP module has up to seven control and status registers:

- CCPxCON1 (Register 12-1) controls many of the features common to all modes, including input clock selection, time base prescaling, timer synchronization, Trigger mode operations and postscaler selection for all modes. The module is also enabled and the operational mode is selected from this register.
- CCPxCON2 (Register 12-2) controls auto-shutdown and restart operation, primarily for PWM operations, and also configures other input capture and output compare features, and configures auxiliary output operation.
- CCPxCON3 (Register 12-3) controls multiple output PWM dead time, controls the output of the output compare and PWM modes, and configures the PWM Output mode for the MCCP modules.
- CCPxSTAT (Register 12-4) contains read-only status bits showing the state of module operations.

Each module also includes eight buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMR is the 32-Bit Timer/Counter register
- CCPxPR is the 32-Bit Timer Period register
- CCPxR is the 32-bit primary data buffer for output compare operations
- CCPxBUF(H/L) registers are the 32-Bit Buffer register pair, which are used in input capture FIFO operations

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{SSx}$ pin is used for Slave mode
0 = $\overline{SSx}$ pin is not used for Slave mode, pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit(3)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDIx bit(4)
1 = SDIx pin is not used by the SPIx module (pin is controlled by port function)
0 = SDIx pin is controlled by the SPIx module

bit 3-2 **STXISEL<1:0>:** SPIx Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPIxSR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPIx Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER (CONTINUED)

bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB, is empty
0 = Transmit buffer, SPIxTXB, is not empty
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit buffer is not full
Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.
Enhanced Buffer mode:
Set when the CPU Write Pointer (CWPTR) + 1 = SPI Read Pointer (SRPTR); cleared otherwise.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB, is full
0 = Receive buffer, SPIxRXB, is not full
Standard Buffer mode:
Automatically set in hardware when the SPIx module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise.

15.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

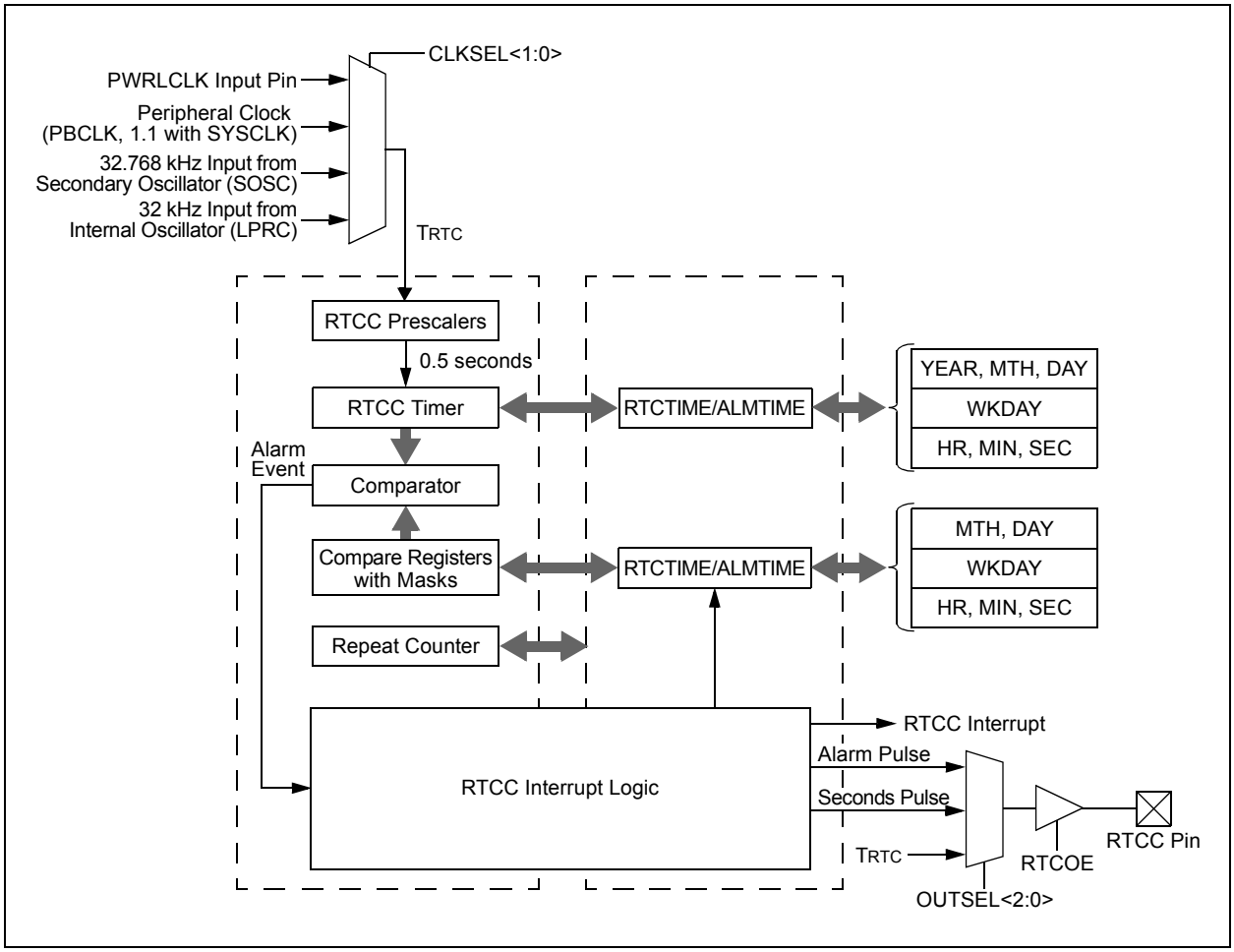
Note:	This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 28. "RTCC with Timestamp"** (DS60001362) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

Key features of the RTCC module are:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Visibility of One-Half Second Period
- Provides Calendar: Weekday, Date, Month and Year
- Alarm Intervals are Configurable for Half of a second, One Second, 10 Seconds, One Minute, 10 Minutes, One Hour, One Day, One Week, One Month and One Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat: Chime
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Smaller Firmware Overhead
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- User Calibration of the Clock Crystal Frequency with Auto-Adjust
- Uses External 32.768 kHz Crystal, 32 kHz Internal Oscillator, PWRLCLK Input Pin or Peripheral Clock
- Alarm Pulse, Seconds Clock or Internal Clock Output on RTCC Pin

FIGURE 15-1: RTCC BLOCK DIAGRAM



17.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

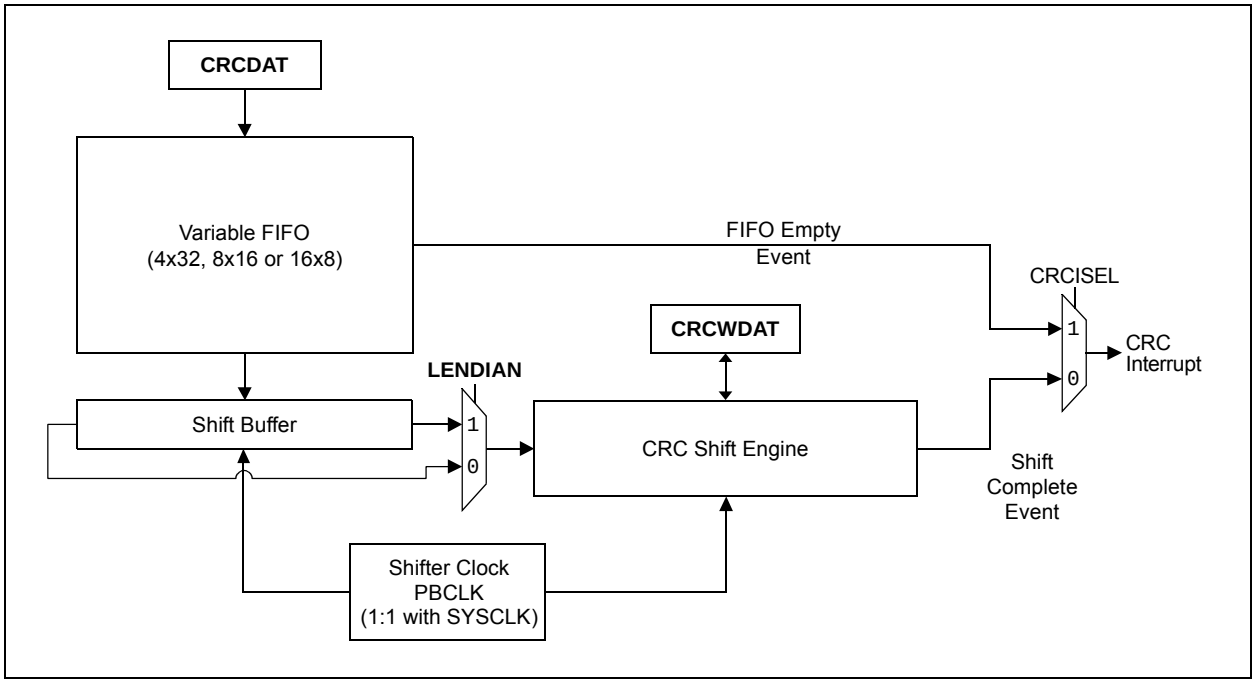
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 60. "32-Bit Programmable Cyclic Redundancy Check"** (DS60001336) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 17-1 displays a simplified block diagram of the CRC generator.

FIGURE 17-1: CRC BLOCK DIAGRAM



19.1 Comparator Control Registers

TABLE 19-1: COMPARATOR 1 AND 2 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0900	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C2EVT	C1EVT	0000
		15:0	—	—	SIDL	—	—	—	—	CVREFSEL	—	—	—	—	—	—	C2OUT	C1OUT	0000
0910	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
0930	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 19-1: CMSTAT: COMPARATOR MODULE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	—	C2EVT	C1EVT
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SIDL	—	—	—	—	CVREFSEL
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-18 **Unimplemented:** Read as '0'

bit 17 **C2EVT:** Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 16 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all enabled comparators in Idle mode

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **CVREFSEL:** Comparator Reference Voltage Select Enable bit
1 = External voltage reference from the V_{REF+} pin is selected
0 = Voltage from CDAC1 is selected

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

TABLE 22-3: PERIPHERAL MODULE DISABLE REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2C00	PMDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PMDLOCK	—	—	—	—	—	—	—	—	—	—	—	0000
2C10	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	HLVDMD	—	—	—	—	FFEF
		15:0	—	—	—	VREFMD	—	—	—	—	—	—	—	—	—	—	—	ADCMD	EFFE
2C20	PMD2	31:16	—	—	—	—	—	—	CLC2MD	CLC1MD	—	—	—	—	—	—	—	—	FCFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP2MD	CMP1MD	FFFC
2C30	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	CCP3MD	CCP2MD	CCP1MD	—	—	—	—	—	—	—	—	F8FF
2C40	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	T1MD	FFFE
2C50	PMD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	r	r	FFFC
		15:0	—	—	—	—	—	—	SPI2MD	SPI1MD	—	—	—	—	—	—	U2MD	U1MD	FCFC
2C60	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	REFOMD	—	—	—	—	—	—	—	RTCCMD	FEFE
2C70	PMD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CRCMD	—	—	—	FFF7

Legend: — = unimplemented, read as '1'; r = reserved bit, maintain as '1'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

23.9 Configuration Words and System Registers

TABLE 23-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
17D4	FOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

TABLE 26-3: OPERATING VOLTAGE SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
DC10	VDD	**Supply Voltage**	2.0	3.6	V	
DC16	VPOR(1)	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	VSS	—	V	
DC17A	SVDD(1)	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	V/ms	0-3.3V in 66 ms, 0-2.0V in 40 ms
DC17B	VBOR	**Brown-out Reset Voltage** on VDD Transition, High-to-Low	2.0	2.22	V	

Note 1: If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

TABLE 26-9: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	-5**(1,4)**	mA	This parameter applies to all pins.
DI60b	IICH	**Input High Injection Current**	0	+5**(2,3,4)**	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins and SOSCI. Maximum IICH current for these exceptions is 0 mA.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20**(5)**	+20**(5)**	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins, (| IICL + | IICH |) ≤ ∑IICT

Note 1: VIL Source < (VSS – 0.3). Characterized but not tested.

2: VIH Source > (VDD + 0.3) for non-5V tolerant pins only.

3: Digital 5V tolerant pins do not have an internal high-side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

4: Injection currents can affect the ADC results.

5: Any number and/or combination of I/O pins, not excluded under IICL or IICH conditions, are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit.

TABLE 26-10: I/O PIN OUTPUT SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**				
DO10		I/O Ports	—	0.36	V	IOL = 6.0 mA, VDD = 3.6V
			—	0.21	V	IOL = 3.0 mA, VDD = 2V
DO16		RA3, RB8, RB9 and RB15 I/O Ports	—	0.16	V	IOL = 6.0 mA, VDD = 3.6V
			—	0.12	V	IOL = 3.0 mA, VDD = 2V
	VOH	**Output High Voltage**				
DO20		I/O Ports	3.25	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.4	—	V	IOH = -3.0 mA, VDD = 2V
DO26		RA3, RB8, RB9 and RB15 I/O Ports	3.3	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.55	—	V	IOH = -3.0 mA, VDD = 2V

TABLE 26-11: PROGRAM FLASH MEMORY SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D130	EP	Cell Endurance	10000	20000	—	E/W	
D131	VICSP	VDD for In-Circuit Serial Programming™ (ICSP™)	VBOR	—	3.6	V	
D132	VRTSP	VDD for Run-Time Self-Programming (RTSP)	2.0	—	3.6	V	
D133	TIW	Self-Timed Double-Word Write Cycle Time	19.7	21.0	22.3	µs	8 bytes, data is not all ‘1’s
		Self-Timed Row Write Cycle Time	1.3	1.4	1.5	ms	256 bytes, data is not all ‘1’s, SYSCLK > 2 MHz
D133	TIE	Self-Timed Page Erase Time	15.0	16.0	17.0	ms	2048 bytes
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D136	TCE	Self-Timed Chip Erase Time	16.0	17.0	18.0	ms	

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 26-7: MCCP AND SCCP INPUT CAPTURE x MODE TIMING CHARACTERISTICS

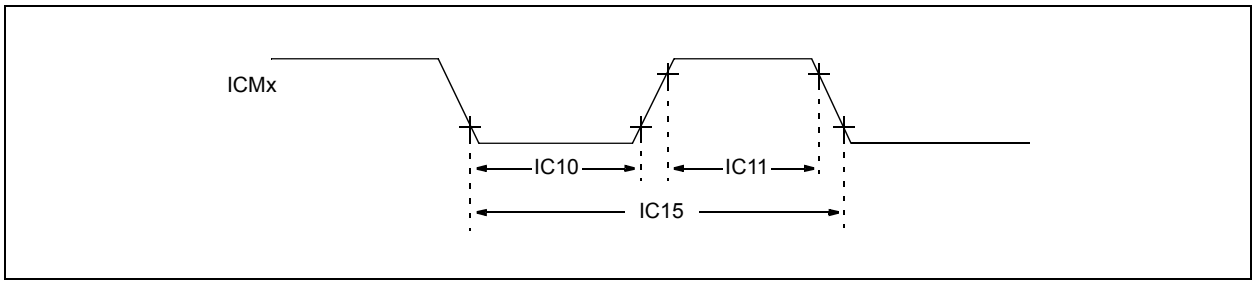
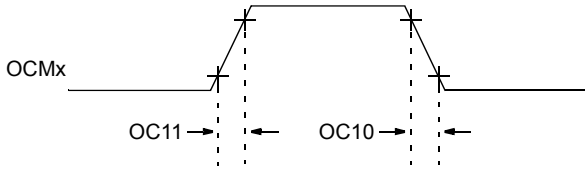


TABLE 26-25: MCCP AND SCCP INPUT CAPTURE x MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**	**Conditions**
IC10	TICL	ICMx Input Low Time	25	—	ns	Must also meet Parameter IC15
IC11	TICH	ICMx Input High Time	25	—	ns	Must also meet Parameter IC15
IC15	TICP	ICMx Input Period	50	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-8: MCCP AND SCCP OUTPUT COMPARE x MODE TIMING CHARACTERISTICS



Note: Refer to Figure 26-2 for load conditions.

TABLE 26-26: MCCP AND SCCP OUTPUT COMPARE x MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristics(1)**	**Min**	**Typ**	**Max**	**Units**
OC10	TOCF	OCMx Output Fall Time	—	10	25	ns
OC11	TOCR	OCMx Output Rise Time	—	10	25	ns

Note 1: These parameters are characterized but not tested in manufacturing.

NOTES: