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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-SQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl036-i-m2

Analog Features

- Two Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit DAC with Output Pin
- Up to 14-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit, 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit, 300K samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0064GPL036 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (Channels)	Comparators	CRC	RTCC	JTAG	Packages
							UART(1)/LIN/J2602	16-Bit Timers	MCCP(3)	SCCP(4)	CLC	SPI(2)/I2S						
PIC32MM0016GPL020	20	16	4	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0032GPL020	20	32	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0064GPL020	20	64	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0016GPL028	28	16	4	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/SOIC/ QFN/UQFN
PIC32MM0032GPL028	28	32	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/ SOIC/ QFN/UQFN
PIC32MM0064GPL028	28	64	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SPDIP/SSOP/ SOIC/QFN/ UQFN
PIC32MM0016GPL036	36/40	16	4	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0032GPL036	36/40	32	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0064GPL036	36/40	64	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN

Note 1: UART1 has assigned pins. UART2 is remappable.

2: SPI1 has assigned pins. SPI2 is remappable.

3: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0064GPL036 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0064GPL036 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0064GPL036 FAMILY BLOCK DIAGRAM

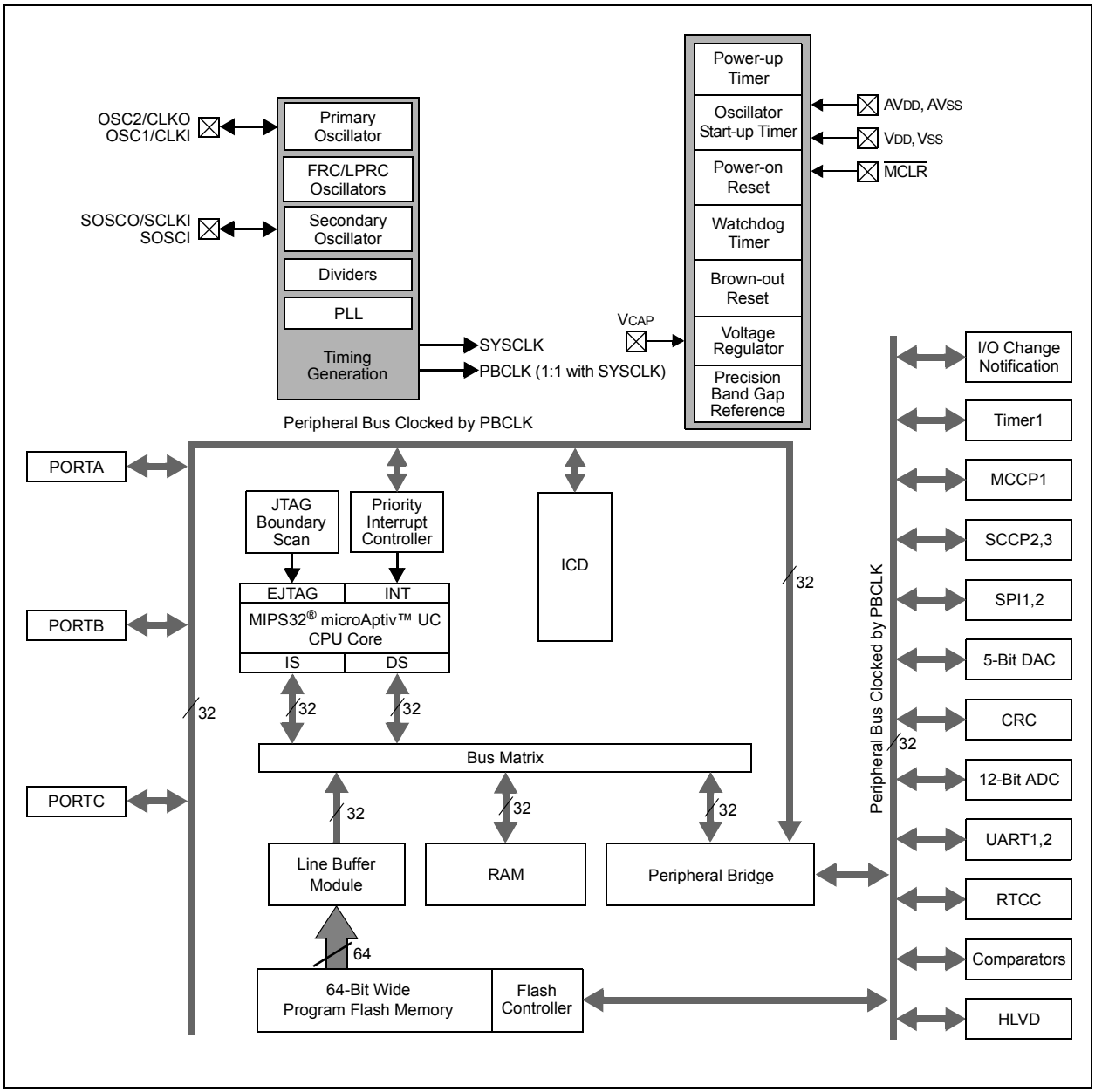


TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
PGEC1	2	5	2	5	36	39	I	ST	ICSP Port 1 programming clock input
PGEC2	19	2	19	22	25	28	I	ST	ICSP Port 2 programming clock input
PGEC3	7	10	12	15	16	16	I	ST	ICSP Port 3 programming clock input
PGED1	1	4	1	4	35	38	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	20	3	18	21	24	27	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	6	9	11	14	15	15	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	7	10	9	12	10	10	I	ST	Real-Time Clock 50/60 Hz clock input
RA0	19	2	27	2	33	36	I/O	ST/DIG	PORTA digital I/O
RA1	20	3	28	3	34	37	I/O	ST/DIG	PORTA digital I/O
RA2	4	7	6	9	7	7	I/O	ST/DIG	PORTA digital I/O
RA3	5	8	7	10	8	8	I/O	ST/DIG	PORTA digital I/O
RA4	7	10	9	12	10	10	I/O	ST/DIG	PORTA digital I/O
RA9	—	—	—	—	11	11	I/O	ST/DIG	PORTA digital I/O
RB0	1	4	1	4	35	38	I/O	ST/DIG	PORTB digital I/O
RB1	2	5	2	5	36	39	I/O	ST/DIG	PORTB digital I/O
RB2	3	6	3	6	1	1	I/O	ST/DIG	PORTB digital I/O
RB3	—	—	4	7	2	2	I/O	ST/DIG	PORTB digital I/O
RB4	6	9	8	11	9	9	I/O	ST/DIG	PORTB digital I/O
RB5	—	—	11	14	15	15	I/O	ST/DIG	PORTB digital I/O
RB6	—	—	12	15	16	16	I/O	ST/DIG	PORTB digital I/O
RB7	8	11	13	16	17	17	I/O	ST/DIG	PORTB digital I/O
RB8	9	12	14	17	18	18	I/O	ST/DIG	PORTB digital I/O
RB9	10	13	15	18	19	20	I/O	ST/DIG	PORTB digital I/O
RB10	—	—	18	21	24	27	I/O	ST/DIG	PORTB digital I/O
RB11	—	—	19	22	25	28	I/O	ST/DIG	PORTB digital I/O
RB12	12	15	20	23	26	29	I/O	ST/DIG	PORTB digital I/O
RB13	13	16	21	24	27	30	I/O	ST/DIG	PORTB digital I/O
RB14	14	17	22	25	28	31	I/O	ST/DIG	PORTB digital I/O
RB15	15	18	23	26	29	32	I/O	ST/DIG	PORTB digital I/O
RC0	—	—	—	—	3	3	I/O	ST/DIG	PORTC digital I/O
RC1	—	—	—	—	4	4	I/O	ST/DIG	PORTC digital I/O
RC2	—	—	—	—	5	5	I/O	ST/DIG	PORTC digital I/O
RC3	—	—	—	—	14	14	I/O	ST/DIG	PORTC digital I/O
RC8	—	—	—	—	20	21	I/O	ST/DIG	PORTC digital I/O
RC9	—	—	16	19	21	22	I/O	ST/DIG	PORTC digital I/O
REFCLKI	10	13	15	18	19	20	I	ST	Reference clock input
REFCLKO	15	18	23	26	29	32	O	DIG	Reference clock output

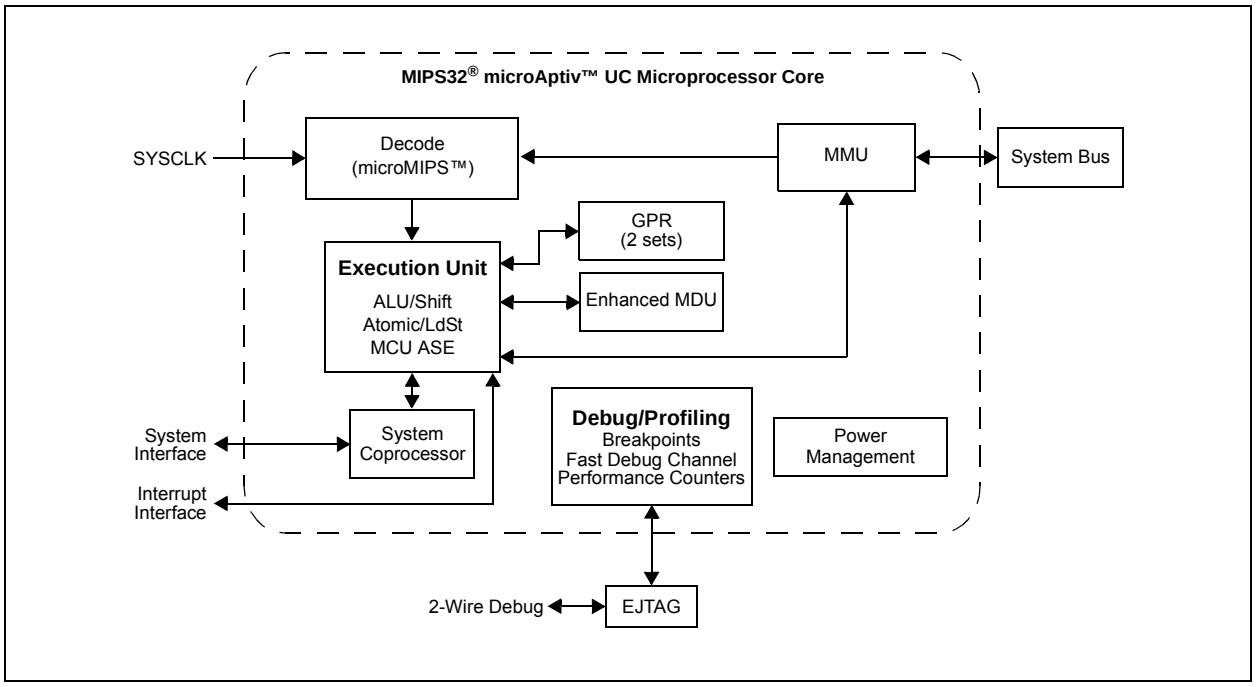
Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
RP1	19	2	27	2	33	36	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	20	3	28	3	34	37	I/O	ST/DIG	
RP3	4	7	6	9	7	7	I/O	ST/DIG	
RP4	5	8	7	10	8	8	I/O	ST/DIG	
RP5	6	9	8	11	9	9	I/O	ST/DIG	
RP6	7	10	9	12	10	10	I/O	ST/DIG	
RP7	9	12	14	17	18	18	I/O	ST/DIG	
RP8	10	13	15	18	19	20	I/O	ST/DIG	
RP9	14	17	22	25	28	31	I/O	ST/DIG	
RP10	15	18	23	26	29	32	I/O	ST/DIG	
RP11	8	11	13	16	17	17	I/O	ST/DIG	
RP12	12	15	20	23	26	29	I/O	ST/DIG	
RP13	13	16	21	24	27	30	I/O	ST/DIG	
RP14	1	4	1	4	35	38	I/O	ST/DIG	
RP15	2	5	2	5	36	39	I/O	ST/DIG	
RP16	3	6	3	6	1	1	I/O	ST/DIG	
RP17	—	—	18	21	24	27	I/O	ST/DIG	
RP18	—	—	19	22	25	28	I/O	ST/DIG	
RP19	—	—	16	19	21	22	I/O	ST/DIG	
RP20	—	—	—	—	11	11	I/O	ST/DIG	
RTCC	14	17	22	25	28	31	O	DIG	Real-Time Clock alarm/seconds output
SCK1	9	12	14	17	18	18	I/O	ST/DIG	SPI1 clock (input or output)
SCLKI	7	10	9	12	10	10	I	ST	Secondary Oscillator external clock input
SDI1	14	17	22	25	28	31	I	ST	SPI1 data input
SDO1	10	13	15	18	19	20	O	DIG	SPI1 data output
SOSCI	6	9	8	11	9	9	—	—	Secondary Oscillator crystal
SOSCO	7	10	9	12	10	10	—	—	Secondary Oscillator crystal
$\overline{SS1}$	15	18	23	26	29	32	I	ST	SPI1 slave select input
T1CK	10	13	15	18	19	20	I	ST	Timer1 external clock input
T1G	10	13	15	18	19	20	I	ST	Timer1 clock gate input
TCK	9	12	14	17	18	18	I	ST	JTAG clock input
TDI	13	16	19	22	25	28	I	ST	JTAG data input
TDO	12	15	18	21	24	27	O	DIG	JTAG data output
TMS	10	13	15	18	19	20	I	ST	JTAG mode select input
U1BCLK	10	13	15	18	19	20	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{U1CTS}$	9	12	14	17	18	18	I	ST	UART1 transmission control input
$\overline{U1RTS}$	10	13	15	18	19	20	O	DIG	UART1 reception control output
U1RX	15	18	23	26	29	32	I	ST	UART1 receive data input
U1TX	14	17	22	25	28	31	O	DIG	UART1 transmit data output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



6.0 RESETS

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset Pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM

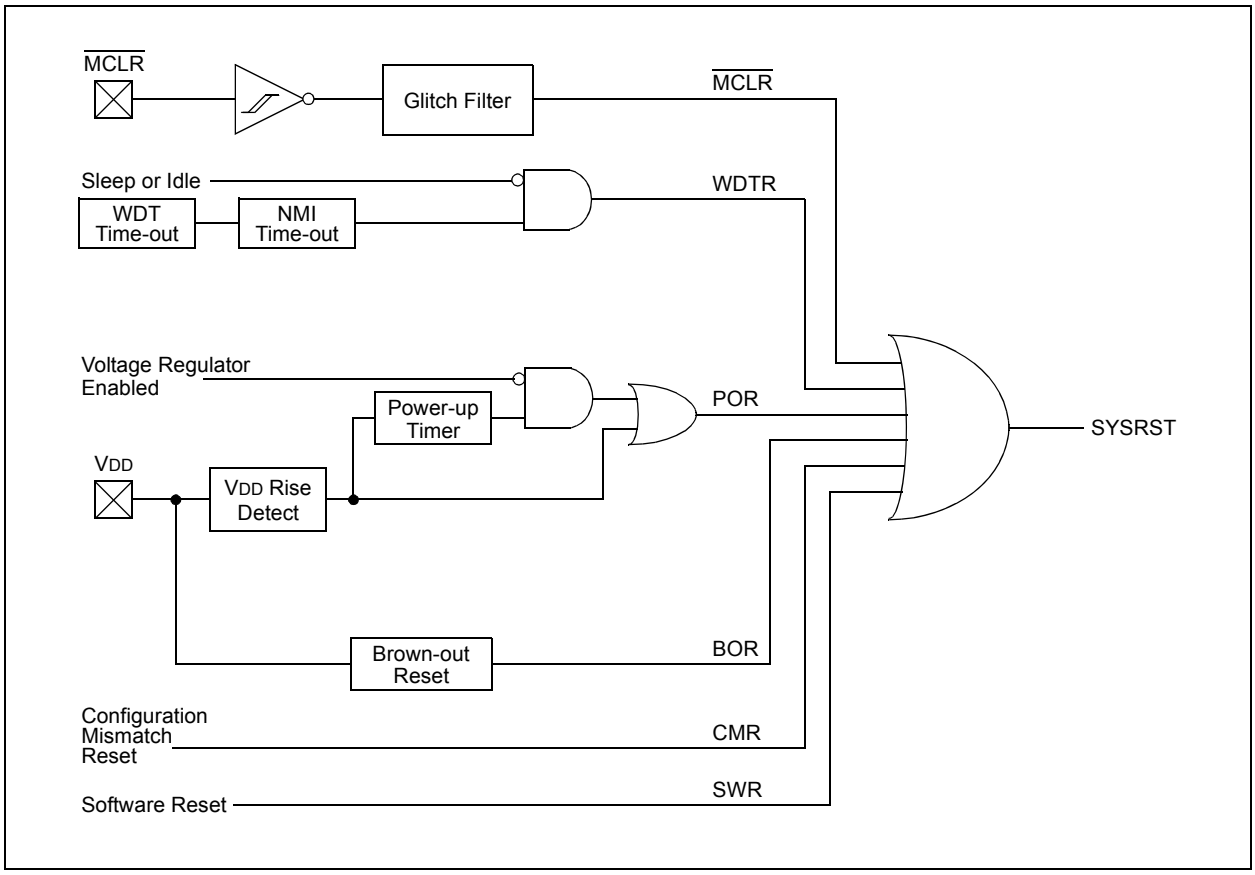


TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F1C0	IPC8	31:16	—	—	—	—	—	—	—	—	—	—	—	CCT3IP<2:0>			CCT3IS<1:0>		0000
		15:0	—	—	—	CCP3IP<2:0>			CCP3IS<1:0>		—	—	—	CCT2IP<2:0>			CCT2IS<1:0>		0000
F1D0	IPC9	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
		15:0	—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		—	—	—	—	—	—	—	—	0000
F1E0	IPC10	31:16	—	—	—	—	—	—	—	—	—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
		15:0	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
F1F0	IPC11	31:16	—	—	—	CPCIP<2:0>			CPCIS<1:0>		—	—	—	NVMIP<2:0>			NVMIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 20-pin devices.

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER (CONTINUED)

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>(1)				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
11111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

9.7 Pin Pull-up and Pull-Down

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source, or sink source, connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

9.8 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features, while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

9.8.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation, “RPn”, in their full pin designation, where “RP” designates a Remappable Peripheral and “n” is the remappable port number.

9.8.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (MCCP, SCCP) and others.

In comparison, some digital only peripheral modules are never included in the PPS feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

9.8.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.0 WATCHDOG TIMER (WDT)

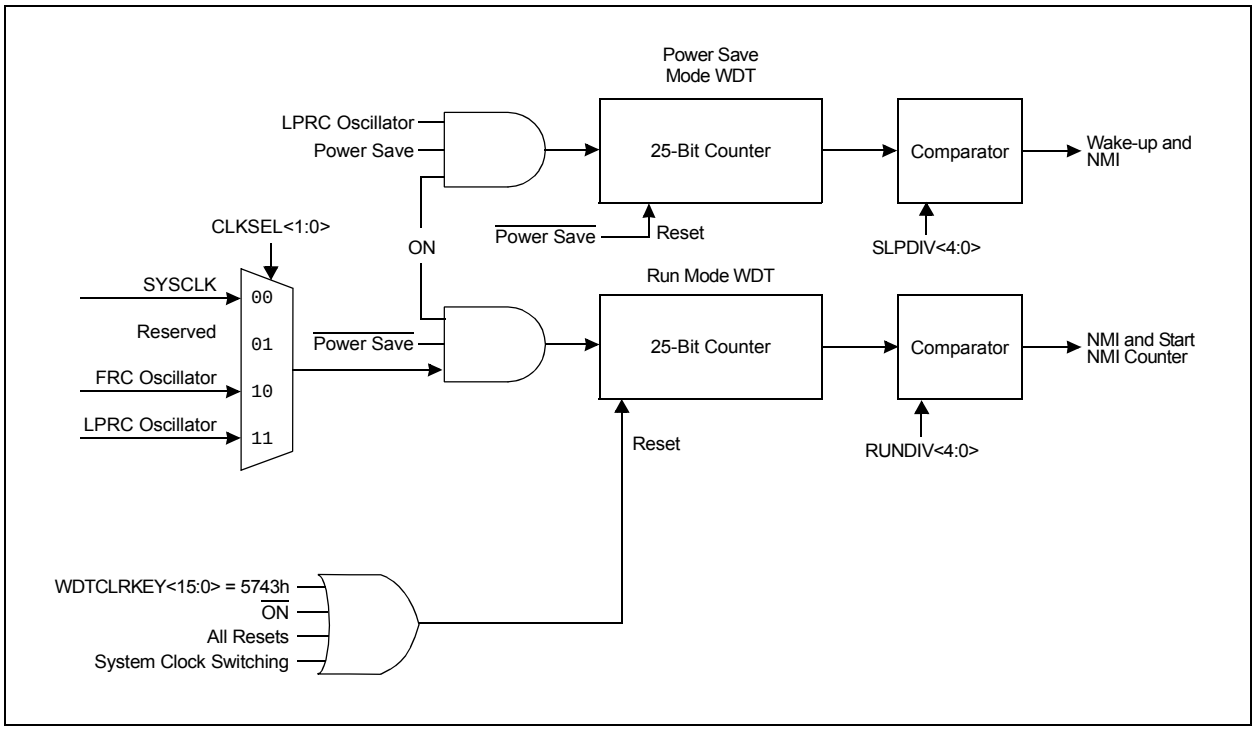
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. "Dual Watchdog Timer"** (DS60001365) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{SSx}$ pin is used for Slave mode
0 = $\overline{SSx}$ pin is not used for Slave mode, pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit(3)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDIx bit(4)
1 = SDIx pin is not used by the SPIx module (pin is controlled by port function)
0 = SDIx pin is controlled by the SPIx module

bit 3-2 **STXISEL<1:0>:** SPIx Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPIxSR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPIx Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

TABLE 16-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(3)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07E0	ADC1BUF14	31:16	ADC1BUF14<31:0>																0000
		15:0																	0000
07F0	ADC1BUF15	31:16	ADC1BUF15<31:0>																0000
		15:0																	0000
0800	AD1CON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON		SIDL	—	—	FORM<2:0>			SSRC<3:0>				MODE12	ASAM	SAMP	DONE	0000
0810	AD1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	—	0000
0820	AD1CON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	EXTSAM	—	SAMC<4:0>					ADCS<7:0>								0000
0840	AD1CHS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CH0NA<2:0>			CH0SA<4:0>					0000
0850	AD1CSS	31:16	—	CSS<30:28>			—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CSS<13:0>(1,2)														0000
0870	AD1CON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ASEN	LPEN	—	BGREQ	—	—	ASINT<1:0>		—	—	—	—	WM<1:0>		CM<1:0>		0000
0880	AD1CHIT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CHH<13:0>(1,2)														0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

2: The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 17-1: CRCCON: CRC CONTROL REGISTER (CONTINUED)

bit 2 **MOD:** CRC Calculation Mode bit
1 = Alternate mode
0 = Legacy mode

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 17-2: CRCXOR:CRC XOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	X<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **X<31:1>:** XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented:** Read as '0'

REGISTER 18-1: CLCxCON: CLCx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	G4POL	G3POL	G2POL	G1POL
15:8	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	ON	—	—	—	INTP(1)	INTN(1)	—	—
7:0	R/W-0	R-0, HS, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>		

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 18 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 17 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 16 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

bit 15 **ON:** CLCx Enable bit
1 = CLCx is enabled and mixing input signals
0 = CLCx is disabled and has logic zero outputs

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **INTP:** CLCx Positive Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** CLCx Negative Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **LCOE:** CLCx Port Enable bit
1 = CLCx port pin output is enabled
0 = CLCx port pin output is disabled

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

19.1 Comparator Control Registers

TABLE 19-1: COMPARATOR 1 AND 2 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0900	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C2EVT	C1EVT	0000
		15:0	—	—	SIDL	—	—	—	—	CVREFSEL	—	—	—	—	—	—	C2OUT	C1OUT	0000
0910	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
0930	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER (CONTINUED)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
110 and 111 = Reserved (selects Fast RC (FRC) Oscillator with Divide-by-N)
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Reserved
010 = Primary Oscillator (XT, HS, EC)
001 = Primary or FRC Oscillator with PLL
000 = Fast RC (FRC) Oscillator with Divide-by-N

REGISTER 23-6: FSEC/AFSEC: CODE-PROTECT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	CP	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **CP:** Code Protection Enable bit
1 = Code protection is disabled
0 = Code protection is enabled

bit 30-0 **Reserved:** Program as ‘1’

TABLE 26-4: OPERATING CURRENT (I_{DD})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC19	0.45	0.65	mA	2.0V	FSYS = 1 MHz
	0.45	0.65	mA	3.3V	
DC23	2.5	3.5	mA	2.0V	FSYS = 8 MHz
	2.5	3.5	mA	3.3V	
DC24	7.0	9.2	mA	2.0V	FSYS = 25 MHz
	7.0	9.2	mA	3.3V	
DC25	0.26	0.35	mA	2.0V	FSYS = 32 kHz
	0.26	0.35	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IDD current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins (except OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- NOP instructions are executed

TABLE 26-6: POWER-DOWN CURRENT (I_{PD})(2)

Parameter No.	Typical(1)	Max	Units	Operating Temperature	VDD	Conditions
DC60	134	198	µA	-40°C	2.0V	Sleep with active main voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) =0)
	136	208	µA	+25°C		
	141	217	µA	+85°C		
	139	209	µA	-40°C	3.3V	
	141	217	µA	+25°C		
	143	231	µA	+85°C		
DC61	4.3	11.7	µA	-40°C	2.0V	Sleep with main voltage regulator in Standby mode (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 0)
	5.1	15.6	µA	+25°C		
	11.4	34.3	µA	+85°C		
	6.1	16.8	µA	-40°C	3.3V	
	6.9	20.1	µA	+25°C		
	12.7	36.0	µA	+85°C		
DC62	2.3	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	2.7	—	µA	+25°C		
	5.2	—	µA	+85°C		
	2.3	—	µA	-40°C	3.3V	
	2.7	—	µA	+25°C		
	5.4	—	µA	+85°C		
DC63	0.28	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	0.44	—	µA	+25°C		
	2.52	—	µA	+85°C		
	0.29	—	µA	-40°C	3.3V	
	0.44	—	µA	+25°C		
	2.62	—	µA	+85°C		

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with:

- Oscillator is configured in FRC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 000)
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

FIGURE 26-9: MCCP AND SCCP PWMx MODE TIMING CHARACTERISTICS

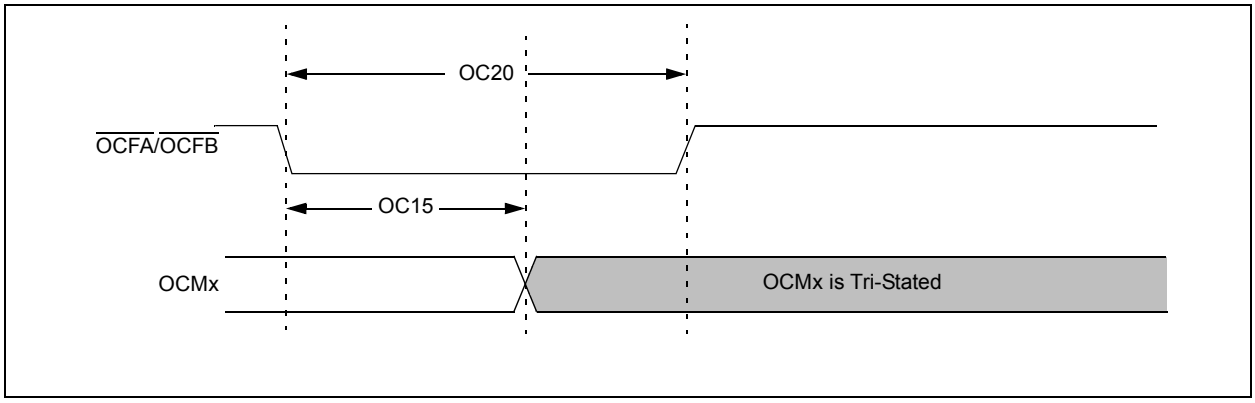


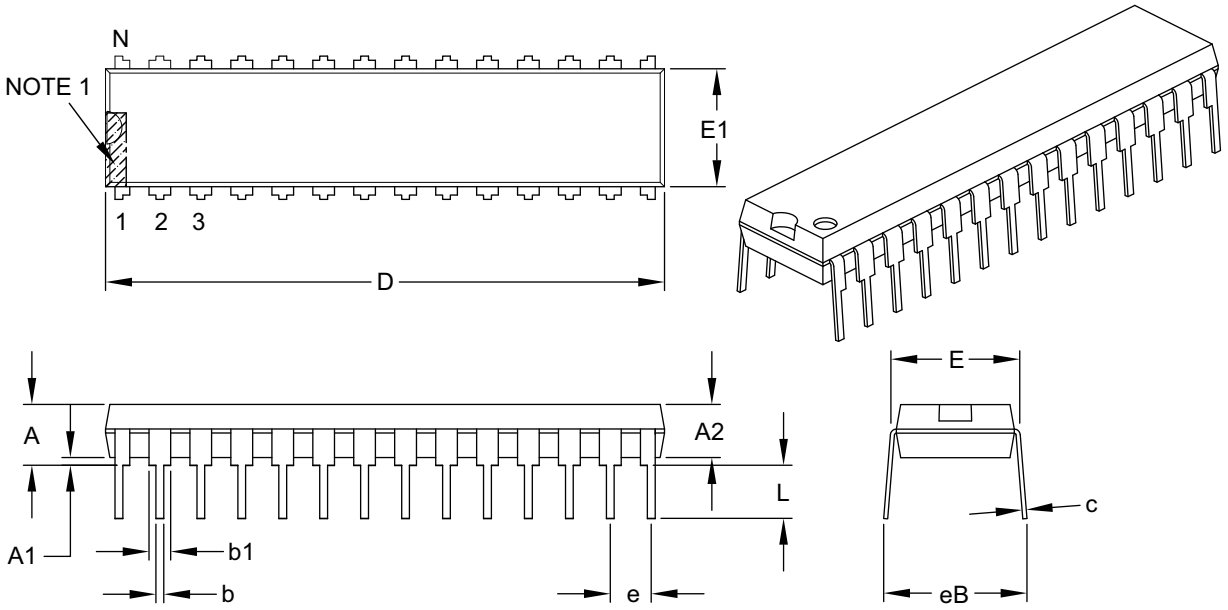
TABLE 26-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
OC15	TFD	Fault Input to PWM I/O Change	—	30	ns
OC20	TFLT	Fault Input Pulse Width	10	—	ns

Note 1: These parameters are characterized but not tested in manufacturing.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B