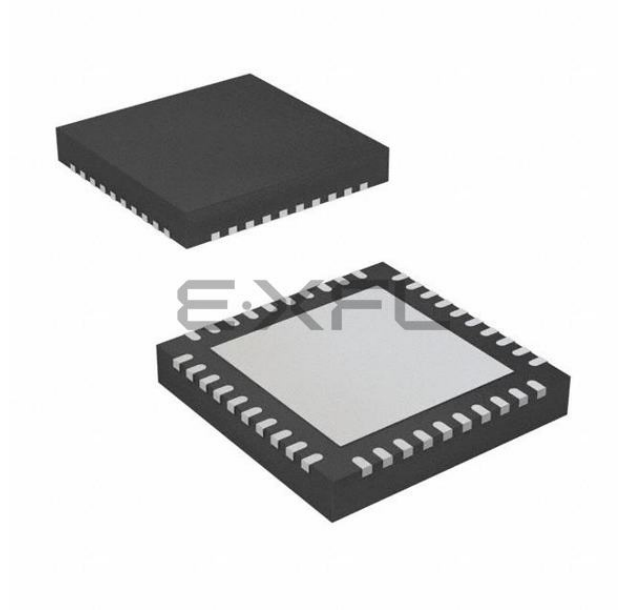
Microchip Technology - PIC32MM0032GPL036-I/MV Datasheet



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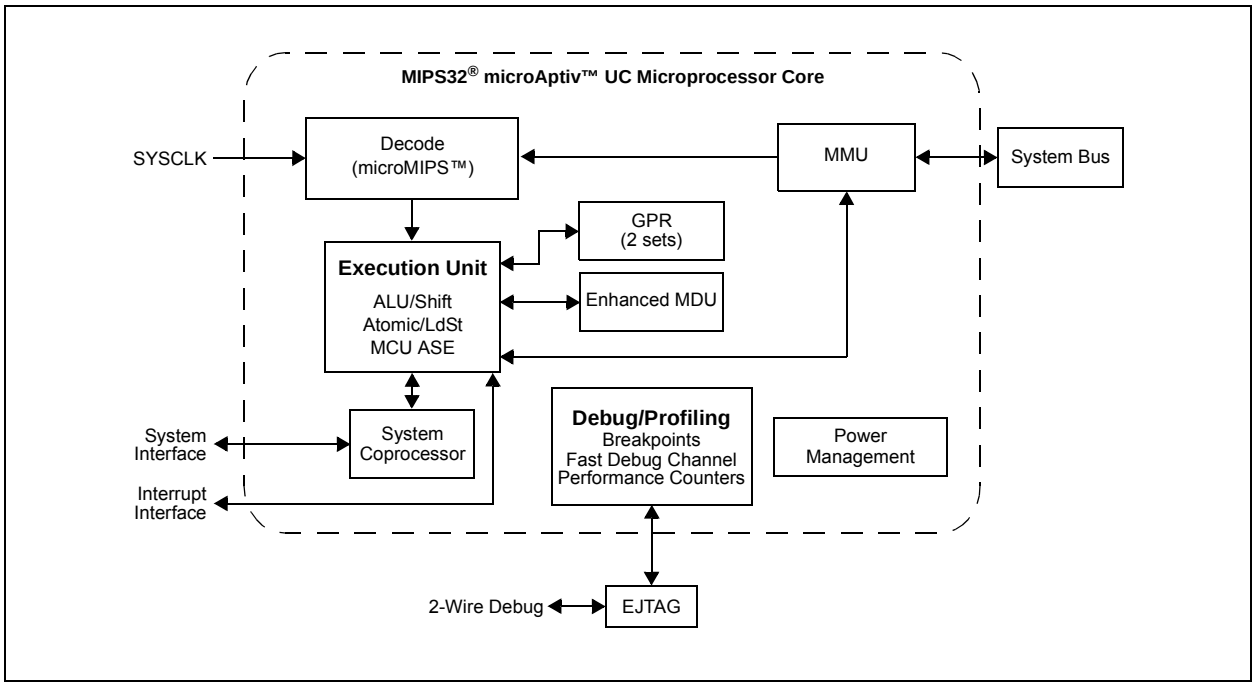
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl036-i-mv

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x(1) (CONTINUED)

bit 12-10 **IP1<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 9-8 **IS1<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP0<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS0<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

Note 1: This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. "Oscillators with DCO"** (DS60001329) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0064GPL036 family oscillator system has the following modules and features:

- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- Primary High-Frequency Crystal Oscillator
- Secondary Low-Frequency and Low-Power Crystal Oscillator
- On-Chip Fast RC (FRC) Oscillator with User-Selectable Output Divider
- Software-Controllable Switching between Various Clock Sources
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output (REFO)

A block diagram of the oscillator system is provided in Figure 8-1.

8.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0064GPL036 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 20-16 **SYNC<4:0>:** CCPx Synchronization Source Select bits
11111 = Timer is in the Free-Running mode and rolls over at FFFFh (Timer Period register is ignored)
11110 = Reserved
. . .
11100 = Reserved
11011 = Time base is synchronized to the start of ADC conversion
11010 = Reserved
11001 = Time base is synchronized to Comparator 2
11000 = Time base is synchronized to Comparator 1
10111 = Reserved
. . .
10010 = Reserved
10001 = Time base is synchronized to CLC2
10001 = Time base is synchronized to CLC1
01111 = Reserved
01110 = Reserved
01101 = Time base is synchronized to the INT4 pin (remappable)
01100 = Time base is synchronized to the INT3 pin
01011 = Time base is synchronized to the INT2 pin
01010 = Time base is synchronized to the INT1 pin
01001 = Time base is synchronized to the INT0 pin
01000 = Reserved
. . .
00101 = Reserved
00100 = Time base is synchronized to SCCP3
00011 = Time base is synchronized to SCCP2
00010 = Time base is synchronized to MCCP1
00001 = Time base is synchronized to this MCCP/SCCP
00000 = No external synchronization; timer rolls over at FFFFh or matches with the Timer Period register

bit 15 **ON:** CCPx Module Enable bit(1)
1 = Module is enabled with the operating mode specified by the MOD<3:0> bits
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** CCPx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **CCPSLP:** CCPx Sleep Mode Enable bit
1 = Module continues to operate in Sleep modes
0 = Module does not operate in Sleep modes

bit 11 **TMRSYNC:** Time Base Clock Synchronization bit
1 = Module time base clock is synchronized to internal system clocks; timing restrictions apply
0 = Module time base clock is not synchronized to internal system clocks

bit 10-8 **CLKSEL<2:0>:** CCPx Time Base Clock Select bits
111 = TCKIA pin (remappable)
110 = TCKIB pin (remappable)
101 = Reserved
100 = Reserved
011 = CLC1 output for MCCP1 and SCCP2/CLC2 output for SCCP3
010 = Secondary Oscillator (SOSC) clock
001 = REFCLKO output clock
000 = System clock (FSYS)

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 23 **MCLKSEL:** Master Clock Enable bit(1)
1 = REFCLKO is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator (1:1 with SYSCLK)

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** SPIx Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPIx Module On bit
1 = SPIx module is enabled
0 = SPIx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues operation when CPU enters Idle mode
0 = Continues operation in Idle mode

bit 12 **DISSDO:** Disable SDOx Pin bit(4)
1 = SDOx pin is not used by the module; the pin is controlled by the associated PORTx register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16/8-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
1	0	32-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
0	1	16-bit data, 16-bit FIFO, 32-bit channel/64-bit frame
0	0	16-bit data, 16-bit FIFO, 16-bit channel/32-bit frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPIx is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPIx Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 16-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 7-4 **SSRC<3:0>:** Conversion Trigger Source Select bits
1111-1101 = Reserved
1100 = CLC2 module event ends sampling and starts conversion
1011 = CLC1 module event ends sampling and starts conversion
1010 = SCCP3 module event ends sampling and starts conversion
1001 = SCCP2 module event ends sampling and starts conversion
1000 = MCCP1 module event ends sampling and starts conversion
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = Timer1 period match ends sampling and starts conversion (can trigger during Sleep mode)
0101 = Timer1 period match ends sampling and starts conversion (will not trigger during Sleep mode)
0100-0010 = Reserved
0001 = Active transition on INT0 pin ends sampling and starts conversion
0000 = Clearing the SAMP bit ends sampling and starts conversion

bit 3 **MODE12:** 12-Bit Operation Mode bit
1 = 12-bit ADC operation
0 = 10-bit ADC operation

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(1)
1 = The ADC Sample-and-Hold Amplifier (SHA) is sampling
0 = The ADC Sample-and-Hold Amplifier is holding

bit 0 **DONE:** ADC Conversion Status bit(2)
1 = Analog-to-Digital conversion is done
0 = Analog-to-Digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

Note 1: The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).
2: The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.

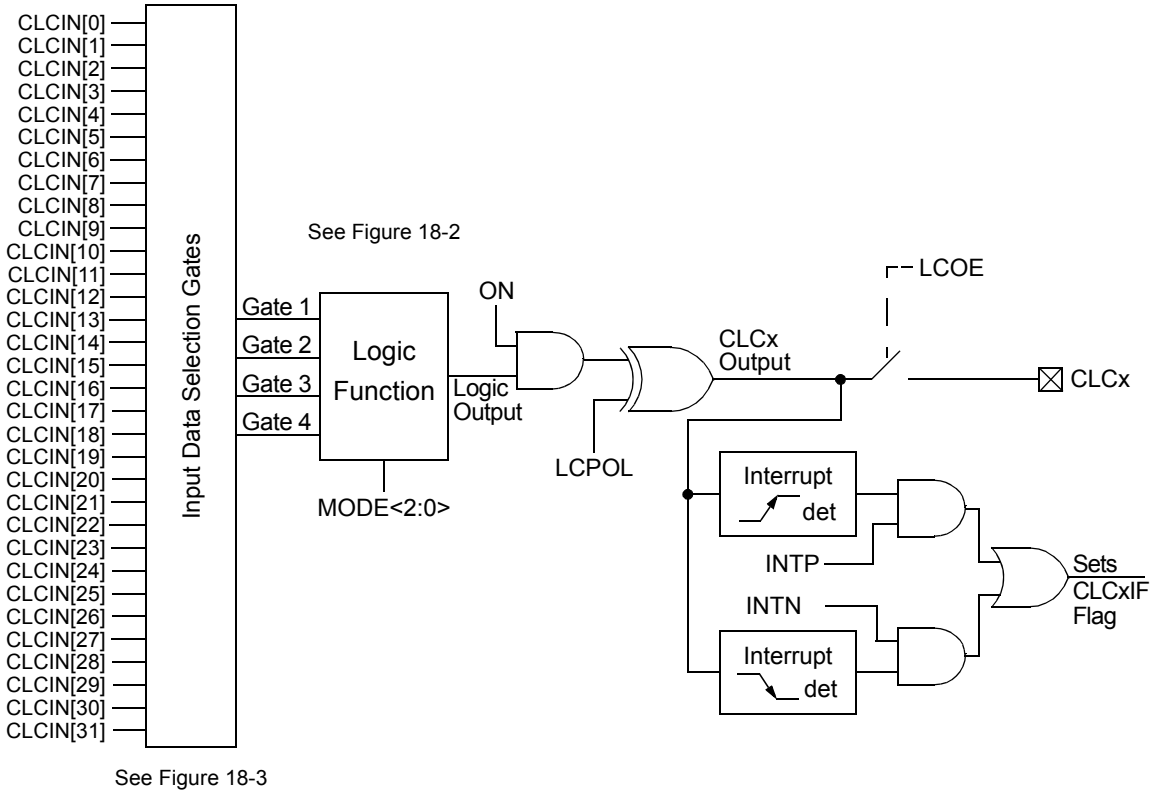
18.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 36. "Configurable Logic Cell"** (DS60001363) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 18-1 shows an overview of the module. Figure 18-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 18-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCON register.

20.1 CDAC Control Registers

TABLE 20-1: CDAC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0980	DAC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	DACDAT<4:0>					0000
		15:0	ON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

REGISTER 21-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER (CONTINUED)

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the LVDIN pin and is compared with 1.2V band gap)
1110 = VDD trip point is 2.11V(1)
1101 = VDD trip point is 2.21V(1)
1100 = VDD trip point is 2.30V(1)
1011 = VDD trip point is 2.40V(1)
1010 = VDD trip point is 2.52V(1)
1001 = VDD trip point is 2.63V(1)
1000 = VDD trip point is 2.82V(1)
0111 = VDD trip point is 2.92V(1)
0110 = VDD trip point is 3.13V(1)
0101 = VDD trip point is 3.44V(1)
0100-0000 = Reserved; do not use

Note 1: The voltage is typical. It is for design guidance only and not tested. Refer to Table 26-13 in **Section 26.0 "Electrical Characteristics"** for minimum and maximum values.

22.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Modes"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes power-saving features for the PIC32MM0064GPL036 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

22.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted, and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a `WAIT` instruction is executed.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- If WDT is enabled, the Run mode counter is not cleared upon entry to Sleep and the Sleep mode counter is reset upon entering Sleep.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC and Timer1).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The on-chip regulator enters Standby mode if the VREGS bit (PWRCON<0>) is set.
- A separate special low-power, low-voltage/ retention regulator is activated if the RETVR Configuration bit (FPOR<2>) is programmed to zero and the RETEN bit (PWRCON<1>) is set.

The processor will exit, or "wake-up", from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than, or equal to, the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

22.2 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than, or equal to, the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

23.5 Band Gap Voltage Reference

PIC32MM0064GPL036 family devices have a precision voltage reference band gap circuit used by many modules. The analog buffers are implemented between the band gap circuit and these modules. The buffers are automatically enabled by the hardware if some part of the device needs the band gap reference. The stabilization time is required when the buffer is switched on. The software can enable these buffers in advance to allow the band gap voltage to stabilize before the module uses it. The ANCFG register contains bits to enable the band gap buffers for the comparators (VBGCMP bit) and ADC (VBGADC bit). Refer to Table 23-6 and Register 23-10 for more information.

23.6 Programming and Diagnostics

PIC32MM0064GPL036 family devices provide a complete range of programming and diagnostic features:

- Simplified Field Programmability using Two-Wire In-Circuit Serial Programming™ (ICSP™) Interfaces
- Debugging using ICSP
- Programming and Debugging Capabilities using the EJTAG Extension of JTAG
- JTAG Boundary Scan Testing for Device and Board Diagnostics

23.7 Unique Device Identifier (UDID)

PIC32MM0064GPL036 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 32-bit program words. When taken together, these fields form a unique 160-bit identifier.

The UDID is stored in five read-only locations, located from 0xBFC41840 to 0xBFC41854 in the device configuration space. Table 23-7 lists the addresses of the Identifier Words.

23.8 Reserved Registers

PIC32MM0064GPL036 family devices have 3 reserved registers, located at 0xBF800400, 0xBF800480 and 0xBF802280. The application code must not modify these reserved locations. Table 23-8 lists the addresses of these reserved registers.

REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER (CONTINUED)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
110 and 111 = Reserved (selects Fast RC (FRC) Oscillator with Divide-by-N)
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Reserved
010 = Primary Oscillator (XT, HS, EC)
001 = Primary or FRC Oscillator with PLL
000 = Fast RC (FRC) Oscillator with Divide-by-N

REGISTER 23-6: FSEC/AFSEC: CODE-PROTECT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	CP	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **CP:** Code Protection Enable bit
1 = Code protection is disabled
0 = Code protection is enabled

bit 30-0 **Reserved:** Program as ‘1’

TABLE 23-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

TABLE 26-6: POWER-DOWN CURRENT (I_{PD})(2)

Parameter No.	Typical(1)	Max	Units	Operating Temperature	VDD	Conditions
DC60	134	198	µA	-40°C	2.0V	Sleep with active main voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) =0)
	136	208	µA	+25°C		
	141	217	µA	+85°C		
	139	209	µA	-40°C	3.3V	
	141	217	µA	+25°C		
	143	231	µA	+85°C		
DC61	4.3	11.7	µA	-40°C	2.0V	Sleep with main voltage regulator in Standby mode (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 0)
	5.1	15.6	µA	+25°C		
	11.4	34.3	µA	+85°C		
	6.1	16.8	µA	-40°C	3.3V	
	6.9	20.1	µA	+25°C		
	12.7	36.0	µA	+85°C		
DC62	2.3	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	2.7	—	µA	+25°C		
	5.2	—	µA	+85°C		
	2.3	—	µA	-40°C	3.3V	
	2.7	—	µA	+25°C		
	5.4	—	µA	+85°C		
DC63	0.28	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	0.44	—	µA	+25°C		
	2.52	—	µA	+85°C		
	0.29	—	µA	-40°C	3.3V	
	0.44	—	µA	+25°C		
	2.62	—	µA	+85°C		

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with:

- Oscillator is configured in FRC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 000)
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

FIGURE 26-3: EXTERNAL CLOCK TIMING

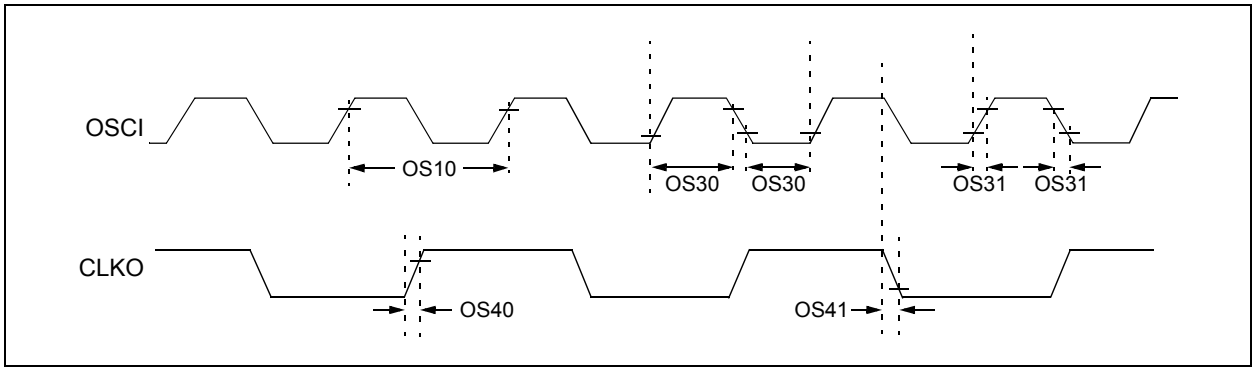


TABLE 26-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency	DC 2	— —	25 12.5	MHz MHz	EC ECPLL(2)
		Oscillator Frequency	3.5 3.5 10 10 31	— — — — —	10 10 25 25 50	MHz MHz MHz MHz kHz	XT XTPLL(2) HS HSPLL(2) SOSC
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x TOSC	—	0.55 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	15	20	ns	
OS41	TckF	CLKO Fall Time(3)	—	15	20	ns	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: PLL dividers and postscalers must be configured so that the system clock frequency does not exceed the maximum operating frequency.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

TABLE 26-32: ADC ACCURACY AND CONVERSION TIMING REQUIREMENTS FOR 10-BIT MODE(1)

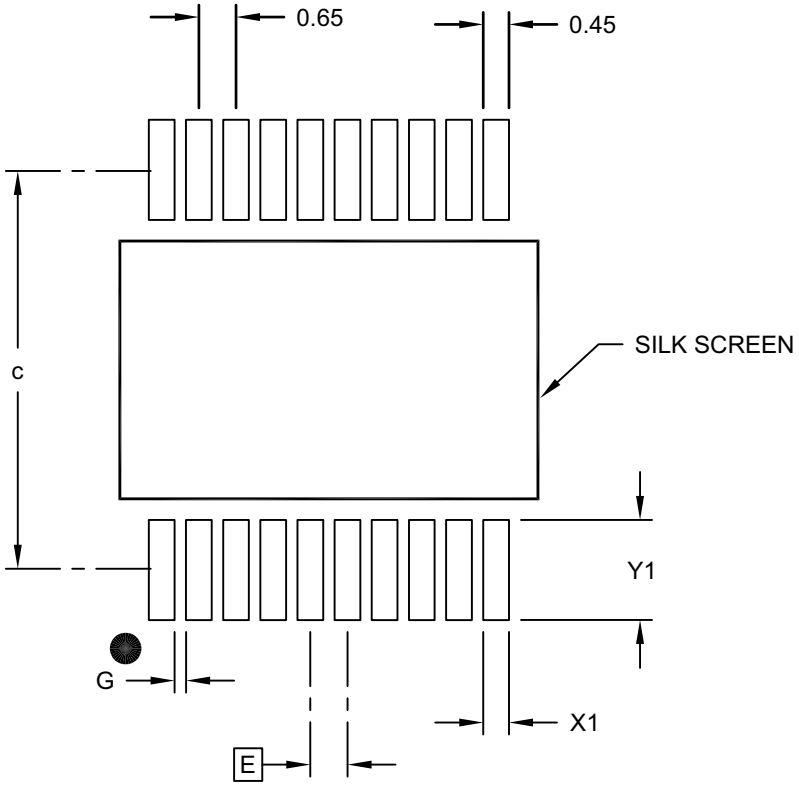
Operating Conditions: V_{DD} = 3.3V, AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3.3V, -40°C ≤ T_A ≤ +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
ADC Accuracy						
AD20A	Nr	Resolution	—	10	—	bits
AD21A	INL	Integral Nonlinearity	—	±0.5	—	LSb
AD22A	DNL	Differential Nonlinearity	—	±0.5	—	LSb
AD23A	GERR	Gain Error	—	+0.75	—	LSb
AD24A	EOFF	Offset Error	—	+0.25	—	LSb
Clock Parameters						
AD50A	TAD	ADC Clock Period	200	—	—	ns
AD61A	tPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	TAD
Conversion Rate						
AD55A	tCONV	Conversion Time	—	12	—	TAD
AD56A	FCNV	Throughput Rate	—	—	300	ksps

Note 1: Measurements are taken with the external V_{REF+} and V_{REF-} used as the ADC voltage reference.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

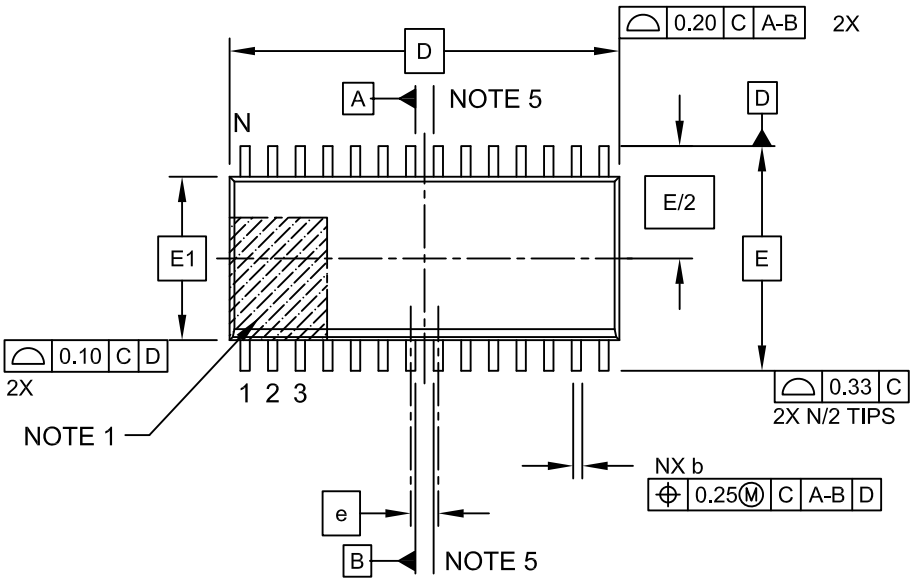
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

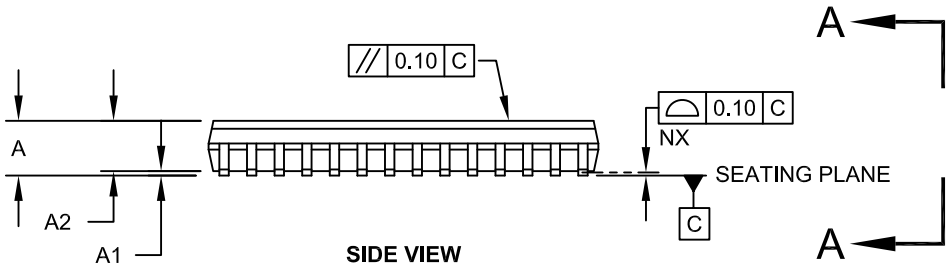
Microchip Technology Drawing No. C04-2072B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

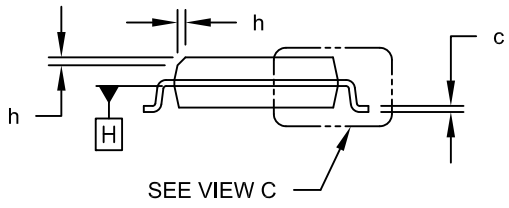
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (February 2015)

This is the initial version of the document.

Revision B (May 2016)

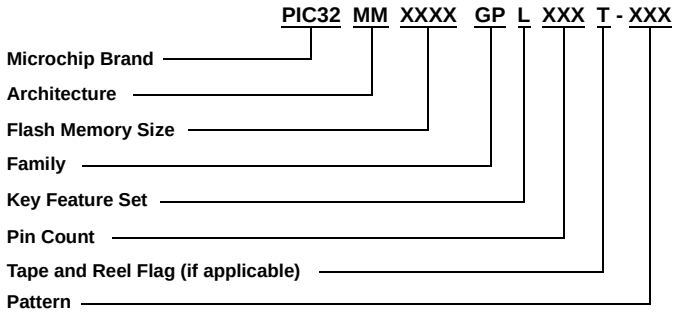
This revision incorporates the following updates:

- Registers:
  - Updates Register 5-1, Register 5-3, Register 5-6, Register 5-7, Register 6-3, Register 6-4, Register 7-2, Register 8-2, Register 8-3, Register 8-5, Register 8-6, Register 11-1, Register 13-1, Register 14-1, Register 15-1, Register 15-5, Register 15-6, Register 16-1, Register 16-2, Register 16-3, Register 16-5, Register 18-2, Register 19-1, Register 19-2 and Register 23-7
- Tables:
  - Updates Table 1-1, Table 5-1, Table 6-1,Table 7-2, Table 7-3, Table 9-3, Table 9-7, Table 15-1, Table 16-1, Table 19-1, Table 22-1, Table 23-4, Table 23-5 Table 26-2, Table 26-3, Table 26-4 and Table 26-6 through Table 26-33
  - Adds Table 23-8
- Figures:
  - Updates Figure 1-1, Figure 3-1, Figure 8-1, Figure 10-1, Figure 14-1, Figure 13-1, Figure 14-1, Figure 14-1, Figure 15-1, Figure 17-1, Figure 18-1, Figure 18-3, Figure 26-1, Figure 26-3, Figure 26-4, Figure 26-9, Figure 26-10, Figure 26-11 and Figure 26-12
- Updates pin function descriptions in **Section 1.0 “Device Overview”**
- Updates text in **Section 9.6 “Input Change Notification (ICN)”**, **Section 9.8.4 “Input Mapping”**, **Section 23.7 “Unique Device Identifier (UDID)”**, **Section 22.5 “Low-Power Brown-out Reset”** and **Section 27.0 “Packaging Information”**
- Adds **Section 5.1 “Flash Controller Registers Write Protection”**, **Section 8.0 “Oscillator Configuration”**, **Section 23.4 “System Registers Write Protection”**, reference to **Section 22.1 “Sleep Mode”**, **Section 22.2 “Idle Mode”** and **Section 23.8 “Reserved Registers”**
- Updates the Absolute Maximum Ratings in **Section 26.0 “Electrical Characteristics”**

This revision also includes minor typographical and formatting changes throughout the data sheet text.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture	MM	= MIPS32® microAptiv™ UC CPU Core
Flash Memory Size	0016 0032 0064	= 16 Kbytes = 32 Kbytes = 64 Kbytes
Family	GP	= General Purpose Family
Key Feature	L	= Up to 25 MHz operating frequency with basic peripheral set of 2 UART and 2 SPI modules
Pin Count	020 028 036	= 20-pin = 28-pin = 36/40-pin
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES	= Engineering Sample

Example:

PIC32MM0064GPL036-I/M2: PIC32 General Purpose Device with MIPS32® microAptiv™ UC Core, 64-Kbyte Program Memory, 36-Pin Package.