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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I ² S, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0032gpl036t-i-mv

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Input Voltage High (V_{IH}) and Input Voltage Low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™ In-Circuit Emulator.

For more information on MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available from the Microchip web site.

- “Using MPLAB® ICD 3 In-Circuit Debugger” (poster) (DS51765)
- “Development Tools Design Advisory” (DS51764)
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” (DS51616)
- “Using MPLAB® REAL ICE™ In-Circuit Emulator” (poster) (DS51749)

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector, and the JTAG pins on the device, as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

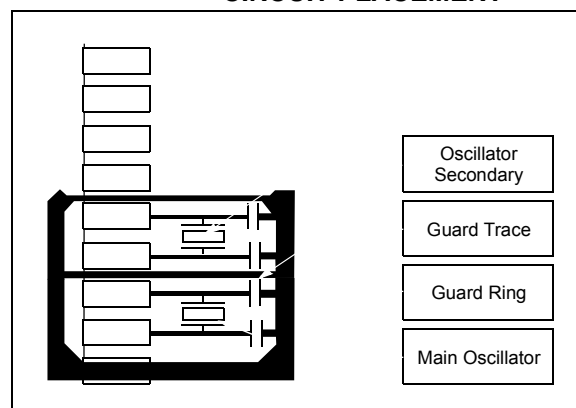
Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Input Voltage High (V_{IH}) and Input Voltage Low (V_{IL}) requirements.

2.7 External Oscillator Pins

The PIC32MM0064GPL036 family has options for two external oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 “Oscillator Configuration”** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

To minimize power consumption, unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic low or logic high state.

Alternatively, inputs can be reserved by ensuring the pin is always configured as an input and externally connecting the pin to V_{SS} or V_{DD}. A current-limiting resistor may be used to create this connection if there is any risk of inadvertently configuring the pin as an output with the logic output state opposite of the chosen power rail.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 10-8 **NOSC<2:0>**: New Oscillator Selection bits⁽³⁾

111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))

101 = Internal Low-Power RC (LPRC) Oscillator

100 = Secondary Oscillator (SOSC)

011 = Reserved

010 = Primary Oscillator (POSC) (XT, HS or EC)

001 = System PLL (SPLL)

000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>).

bit 7 **CLKLOCK**: Clock Selection Lock Enable bit

1 = Clock and PLL selections are locked

0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented**: Read as '0'

bit 4 **SLPEN**: Sleep Mode Enable bit

1 = Device will enter Sleep mode when a WAIT instruction is executed

0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF**: Clock Fail Detect bit

1 = FSCM has detected a clock failure

0 = No clock failure has been detected

bit 2 **Unimplemented**: Read as '0'

bit 1 **SOSCEN**: Secondary Oscillator (SOSC) Enable bit⁽⁴⁾

1 = Enables Secondary Oscillator

0 = Disables Secondary Oscillator

bit 0 **OSWEN**: Oscillator Switch Enable bit⁽²⁾

1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits

0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 “System Registers Write Protection”** for details.

2: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

3: The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.

4: The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

11.1 Watchdog Timer Control Registers

TABLE 11-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
3E80	WDTCON ⁽¹⁾	31:16	WDTCLRKEY<15:0>															0000
		15:0	ON	—	—	RUNDIV<4:0>				CLKSEL<1:0>			SLPDIV<4:0>				WDTWINEN	xxxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

12.0 CAPTURE/COMPARE/PWM/TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 30. “Capture/Compare/PWM/Timer (MCCP and SCCP)”** (DS60001381) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

12.1 Introduction

PIC32MM0064GPL036 family devices include three Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 32-bit microcontrollers. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all earlier PIC32 devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single Capture/Compare/PWM/Timer (SCCPs) output modules provide only one PWM output. Multiple Capture/Compare/PWM/Timer (MCCPs) output modules can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features:

- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for module Interrupt Events or Triggers
- Synchronization Output Signal for Coordinating other MCCP/SCCP modules with User-Configurable Alternate and Auxiliary Source Options

- Fully Asynchronous Operation in all modes and in Low-Power Operation
- Special Output Trigger for ADC Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture modes:
 - Backward compatible with previous input capture peripherals of the PIC32 family
 - 16-bit or 32-bit capture of time base on external event
 - Up to four-level deep FIFO capture buffer
 - Capture source input multiplexer
 - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
 - Backward compatible with previous output compare peripherals of the PIC32 family
 - Single Edge and Dual Edge Compare modes
 - Center-Aligned Compare mode
 - Variable Frequency Pulse mode
 - External Input mode

MCCP modules also include these extended PWM features:

- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can be operated in only one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in Figure 12-1. All three modes use the time base generator and the common Timer register pair (CCPxTMR). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

13.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I²S)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. “Serial Peripheral Interface (SPI)”** (DS61106) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The SPI/I²S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well

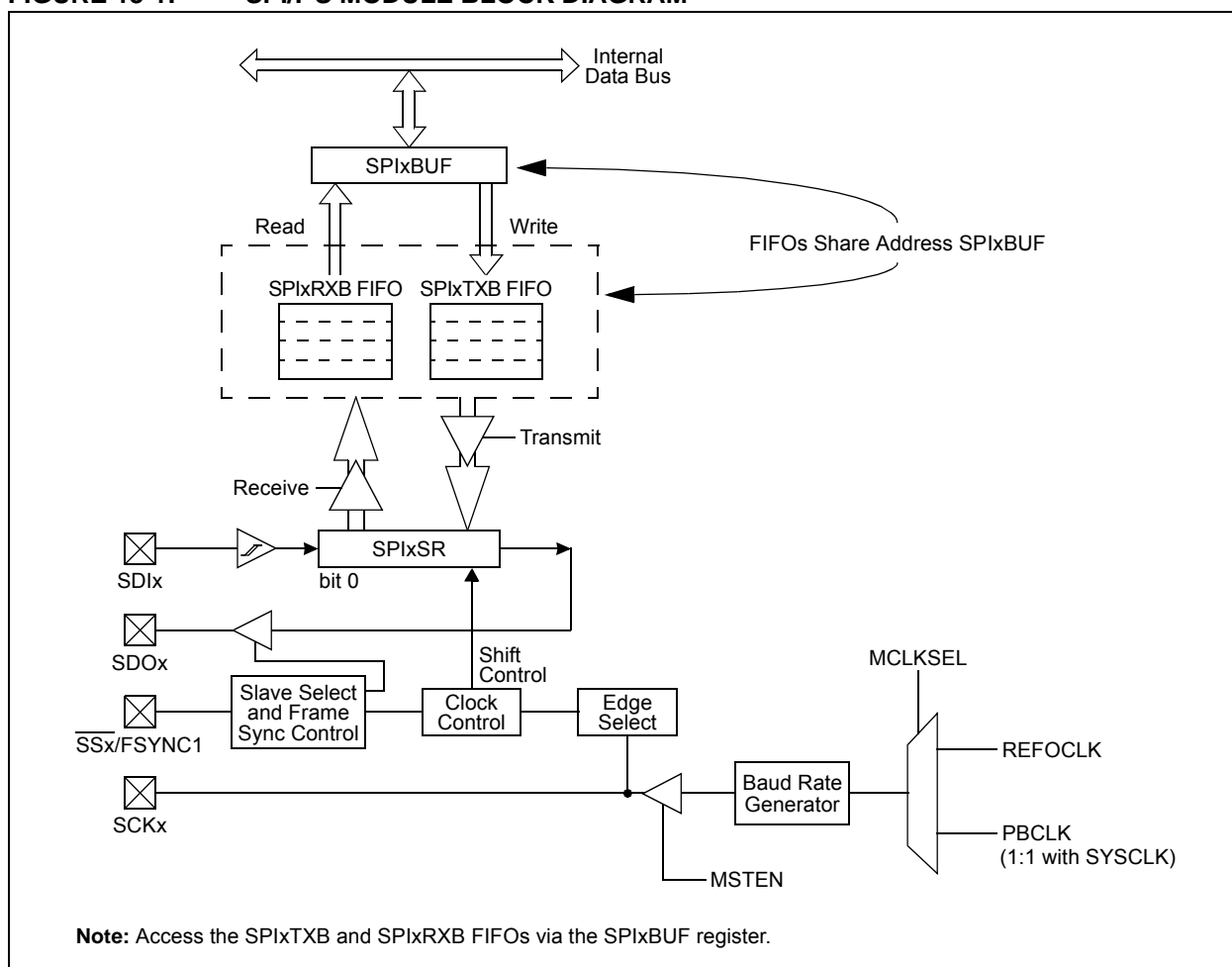
as digital audio devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I²S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes Support
- Four Different Clock Formats
- Enhanced Framed SPI Protocol Support
- User-Configurable 8-Bit, 16-Bit and 32-Bit Data Width
- Separate SPI FIFO Buffers for Receive and Transmit:
 - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable Interrupt Event on Every 8-Bit, 16-Bit and 32-Bit Data Transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
 - I²S protocol

FIGURE 13-1: SPI/I²S MODULE BLOCK DIAGRAM



REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

- bit 7 **SSEN**: Slave Select Enable (Slave mode) bit
1 = \overline{SSx} pin is used for Slave mode
0 = \overline{SSx} pin is not used for Slave mode, pin is controlled by port function
- bit 6 **CKP**: Clock Polarity Select bit⁽³⁾
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN**: Master Mode Enable bit
1 = Master mode
0 = Slave mode
- bit 4 **DISSDI**: Disable SDIx bit⁽⁴⁾
1 = SDIx pin is not used by the SPIx module (pin is controlled by port function)
0 = SDIx pin is controlled by the SPIx module
- bit 3-2 **STXISEL<1:0>**: SPIx Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPIxSR and transmit operations are complete
- bit 1-0 **SRXISEL<1:0>**: SPIx Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

- Note 1:** These bits can only be written when the ON bit = 0. Refer to **Section 26.0 “Electrical Characteristics”** for maximum clock frequency requirements.
- 2:** This bit is not used in the Framed SPI mode. The user should program this bit to ‘0’ for the Framed SPI mode (FRMEN = 1).
- 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to ‘1’, regardless of the actual value of the CKP bit.
- 4:** These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 “Peripheral Pin Select (PPS)”** for more information).

TABLE 16-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name ⁽³⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07E0	ADC1BUF14	31:16	ADC1BUF14<31:0>																0000
		15:0																	0000
07F0	ADC1BUF15	31:16	ADC1BUF15<31:0>																0000
		15:0																	0000
0800	AD1CON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON		SIDL	—	—	FORM<2:0>			SSRC<3:0>			MODE12		ASAM	SAMP	DONE	0000
0810	AD1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—	BUFS	—	SMPI<3:0>			BUFM		—	0000
0820	AD1CON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	EXTSAM	—	SAMC<4:0>					ADCS<7:0>								0000
0840	AD1CHS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CH0NA<2:0>			CH0SA<4:0>					0000
0850	AD1CSS	31:16	—	CSS<30:28>			—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CSS<13:0> ^(1,2)														0000
0870	AD1CON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ASEN	LPEN	—	BGREQ	—	—	ASINT<1:0>		—	—	—	—	WM<1:0>		CM<1:0>		0000
0880	AD1CHIT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CHH<13:0> ^(1,2)														0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

2: The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 16-4: AD1CON5: ADC CONTROL REGISTER 5 (CONTINUED)

bit 1-0 **CM<1:0>**: Compare Mode bits

- 11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
- 10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
- 01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
- 00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

Note 1: When auto-scan is enabled (ASEN (AD1CON5<15>) = 1), the CSCNA (AD1CON2<10>) and SMPI<3:0> (AD1CON2<5:2>) bits are ignored.

2: The ASINT<1:0> bits setting only takes effect when ASEN (AD1CON5<15>) = 1. Interrupt generation is governed by the SMPI<3:0> bits field.

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REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

- bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
 1 = The Data Source 3 inverted signal is enabled for Gate 1
 0 = The Data Source 3 inverted signal is disabled for Gate 1
- bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
 1 = The Data Source 2 signal is enabled for Gate 1
 0 = The Data Source 2 signal is disabled for Gate 1
- bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
 1 = The Data Source 2 inverted signal is enabled for Gate 1
 0 = The Data Source 2 inverted signal is disabled for Gate 1
- bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
 1 = The Data Source 1 signal is enabled for Gate 1
 0 = The Data Source 1 signal is disabled for Gate 1
- bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
 1 = The Data Source 1 inverted signal is enabled for Gate 1
 0 = The Data Source 1 inverted signal is disabled for Gate 1

19.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides two dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals ‘1’, the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 19-1. Each comparator has its own control register, CMxCON (Register 19-2), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (Register 19-1).

FIGURE 19-1: DUAL COMPARATOR MODULE BLOCK DIAGRAM

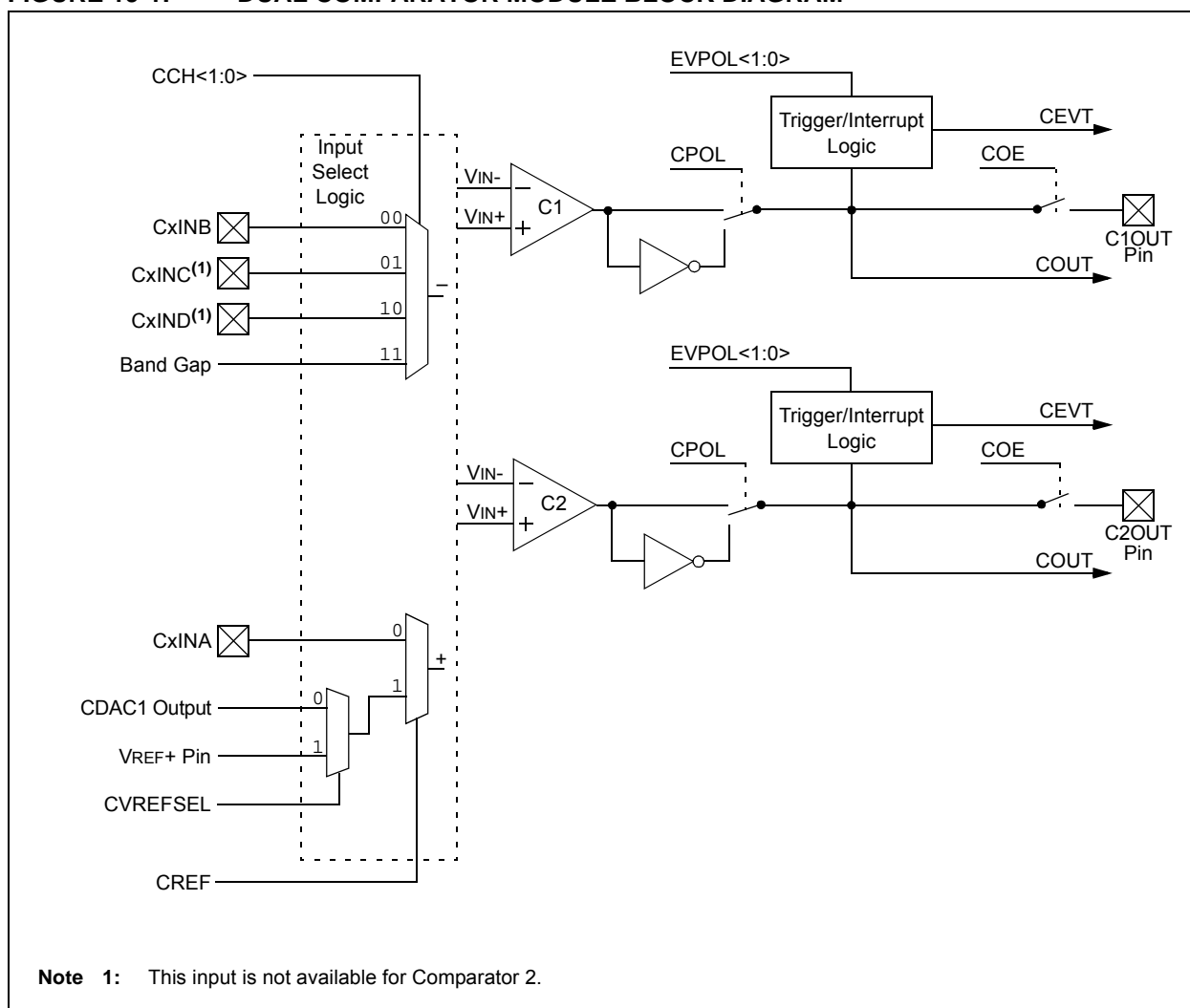


TABLE 22-3: PERIPHERAL MODULE DISABLE REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2C00	PMDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PMDLOCK	—	—	—	—	—	—	—	—	—	—	—	0000
2C10	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	HLVDMD	—	—	—	—	FFEF
		15:0	—	—	—	VREFMD	—	—	—	—	—	—	—	—	—	—	—	ADCMD	EFEE
2C20	PMD2	31:16	—	—	—	—	—	—	CLC2MD	CLC1MD	—	—	—	—	—	—	—	—	FCFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP2MD	CMP1MD	FFFC
2C30	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	CCP3MD	CCP2MD	CCP1MD	—	—	—	—	—	—	—	F8FF
2C40	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	T1MD	FFFE
2C50	PMD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	r	r	FFFC
		15:0	—	—	—	—	—	—	SPI2MD	SPI1MD	—	—	—	—	—	—	U2MD	U1MD	FCFC
2C60	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	REFOMD	—	—	—	—	—	—	—	RTCCMD	FEFE
2C70	PMD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CRCMD	—	—	—	FFF7

Legend: — = unimplemented, read as '1'; r = reserved bit, maintain as '1'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

TABLE 23-4: ALTERNATE CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
1740	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1744	AFDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
1748	AFICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
174C	AFPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
1750	AFWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>				WINDIS		FWDTWINSZ<1:0>		SWDTPS<4:0>				
1754	AFOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
1758	AFSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
175C	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1760	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1764	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

24.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

24.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

25.0 INSTRUCTION SET

The PIC32MM0064GPL036 family instruction set complies with the MIPS® Release 3 instruction set architecture. Only microMIPS32™ instructions are supported. The PIC32MM0064GPL036 family does not have the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

<p>Note: Refer to the “MIPS® Architecture for Programmers Volume II-B: The microMIPS32™ Instruction Set” at www.imgtec.com for more information.</p>

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TABLE 26-4: OPERATING CURRENT (I_{DD})⁽²⁾

Operating Conditions: -40°C < T _A < +85°C (unless otherwise stated)					
Parameter No.	Typical ⁽¹⁾	Max	Units	V _{DD}	Conditions
DC19	0.45	0.65	mA	2.0V	F _{SYS} = 1 MHz
	0.45	0.65	mA	3.3V	
DC23	2.5	3.5	mA	2.0V	F _{SYS} = 8 MHz
	2.5	3.5	mA	3.3V	
DC24	7.0	9.2	mA	2.0V	F _{SYS} = 25 MHz
	7.0	9.2	mA	3.3V	
DC25	0.26	0.35	mA	2.0V	F _{SYS} = 32 kHz
	0.26	0.35	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{DD} current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
- OSC1 pin is driven with external square wave with levels from 0.3V to V_{DD} – 0.3V
- OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDTC<15>) = 0)
- All I/O pins (except OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- NOP instructions are executed

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TABLE 26-9: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ (unless otherwise stated)						
Param. No.	Symbol	Characteristics	Min.	Max.	Units	Conditions
DI60a	I _{ICL}	Input Low Injection Current	0	-5 ^(1,4)	mA	This parameter applies to all pins.
DI60b	I _{ICH}	Input High Injection Current	0	+5 ^(2,3,4)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins and SOSCI. Maximum I _{ICH} current for these exceptions is 0 mA.
DI60c	ΣI_{ICT}	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁵⁾	+20 ⁽⁵⁾	mA	Absolute instantaneous sum of all \pm input injection currents from all I/O pins, ($ I_{ICL} + I_{ICH} $) $\leq \Sigma I_{ICT}$

- Note 1:** V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.
- 2:** V_{IH} Source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 3:** Digital 5V tolerant pins do not have an internal high-side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 4:** Injection currents can affect the ADC results.
- 5:** Any number and/or combination of I/O pins, not excluded under I_{ICL} or I_{ICH} conditions, are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit.

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TABLE 26-10: I/O PIN OUTPUT SPECIFICATIONS

Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ (unless otherwise stated)						
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
DO10	VOL	Output Low Voltage I/O Ports	—	0.36	V	$I_{OL} = 6.0 \text{ mA}$, $V_{DD} = 3.6V$
			—	0.21	V	$I_{OL} = 3.0 \text{ mA}$, $V_{DD} = 2V$
DO16		RA3, RB8, RB9 and RB15 I/O Ports	—	0.16	V	$I_{OL} = 6.0 \text{ mA}$, $V_{DD} = 3.6V$
			—	0.12	V	$I_{OL} = 3.0 \text{ mA}$, $V_{DD} = 2V$
DO20	VOH	Output High Voltage I/O Ports	3.25	—	V	$I_{OH} = -6.0 \text{ mA}$, $V_{DD} = 3.6V$
			1.4	—	V	$I_{OH} = -3.0 \text{ mA}$, $V_{DD} = 2V$
DO26		RA3, RB8, RB9 and RB15 I/O Ports	3.3	—	V	$I_{OH} = -6.0 \text{ mA}$, $V_{DD} = 3.6V$
			1.55	—	V	$I_{OH} = -3.0 \text{ mA}$, $V_{DD} = 2V$

TABLE 26-11: PROGRAM FLASH MEMORY SPECIFICATIONS

Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ (unless otherwise stated)							
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
D130	EP	Cell Endurance	10000	20000	—	E/W	8 bytes, data is not all '1's 256 bytes, data is not all '1's, $SYSCLK > 2 \text{ MHz}$ 2048 bytes If no other specifications are violated
D131	VICSP	V_{DD} for In-Circuit Serial Programming™ (ICSP™)	V_{BOR}	—	3.6	V	
D132	VRTSP	V_{DD} for Run-Time Self-Programming (RTSP)	2.0	—	3.6	V	
D133	TIW	Self-Timed Double-Word Write Cycle Time	19.7	21.0	22.3	μs	
		Self-Timed Row Write Cycle Time	1.3	1.4	1.5	ms	
D133	TIE	Self-Timed Page Erase Time	15.0	16.0	17.0	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	
D136	TCE	Self-Timed Chip Erase Time	16.0	17.0	18.0	ms	

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

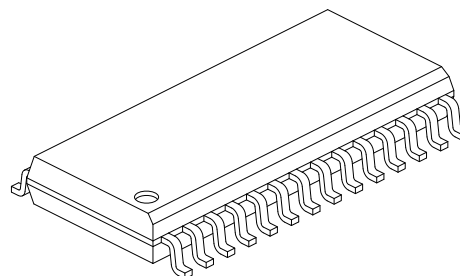
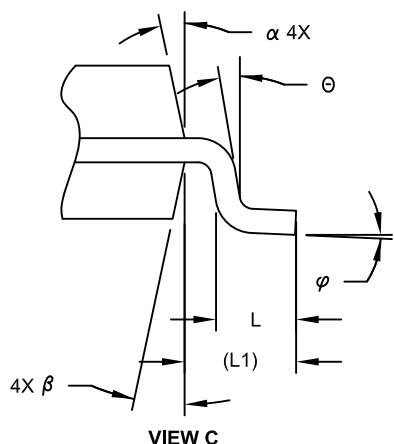
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NOTES:

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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

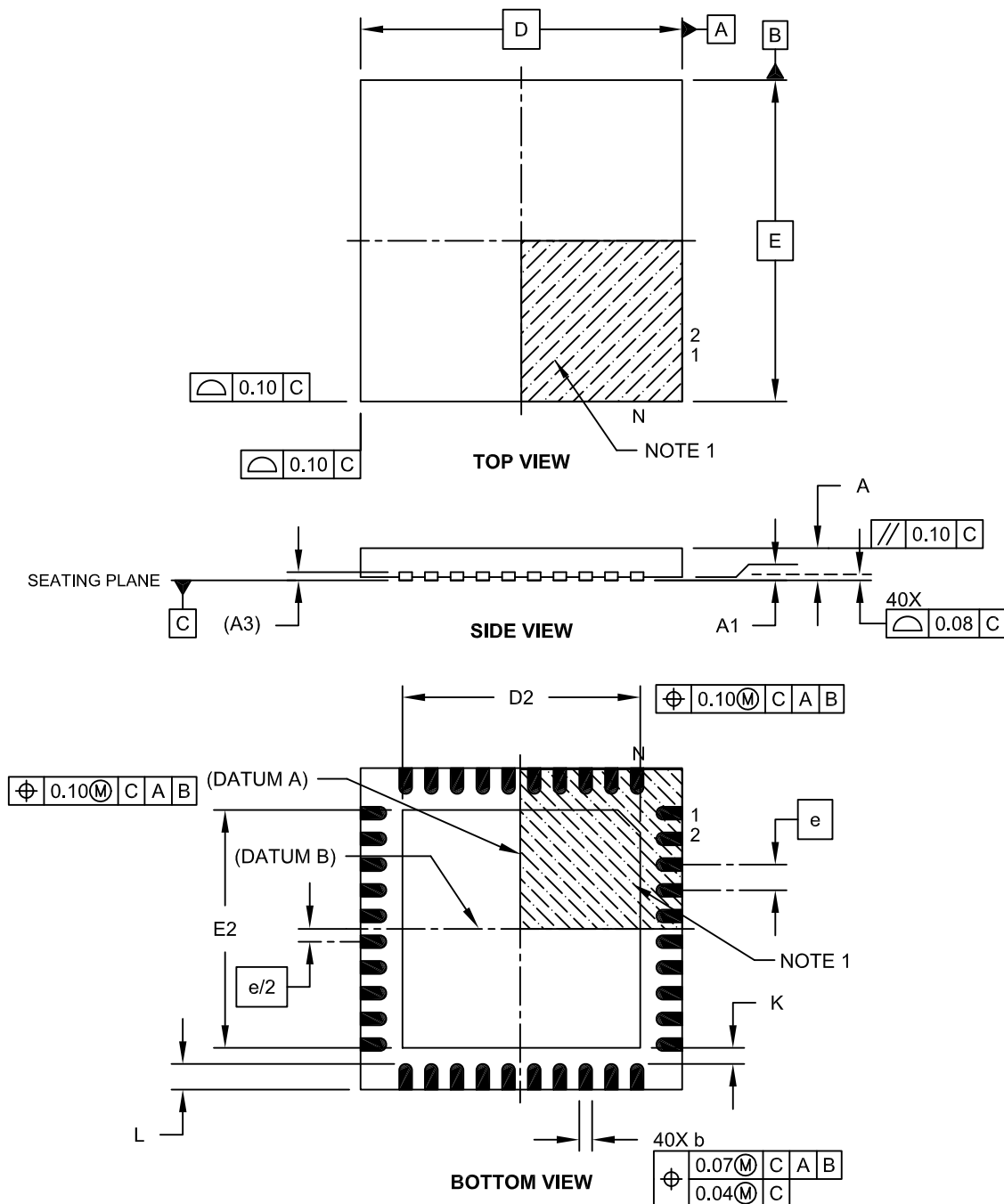
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

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40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-156A Sheet 1 of 2