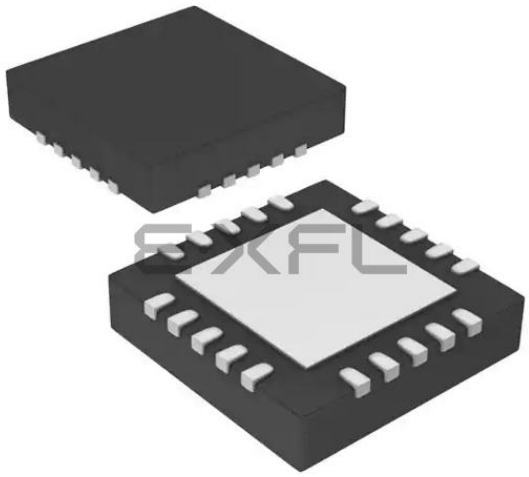

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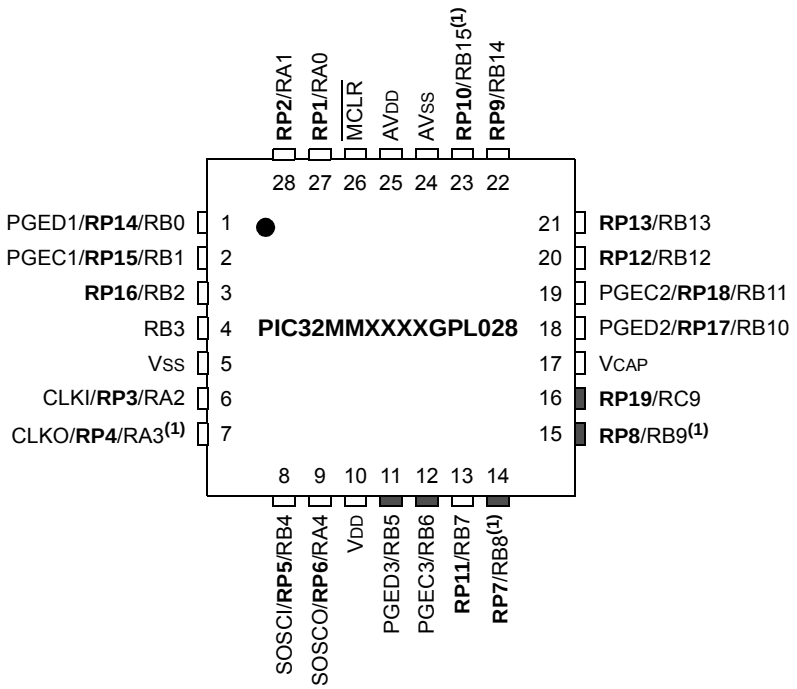
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl020-e-ml

Pin Diagrams (Continued)

28-Pin QFN/UQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

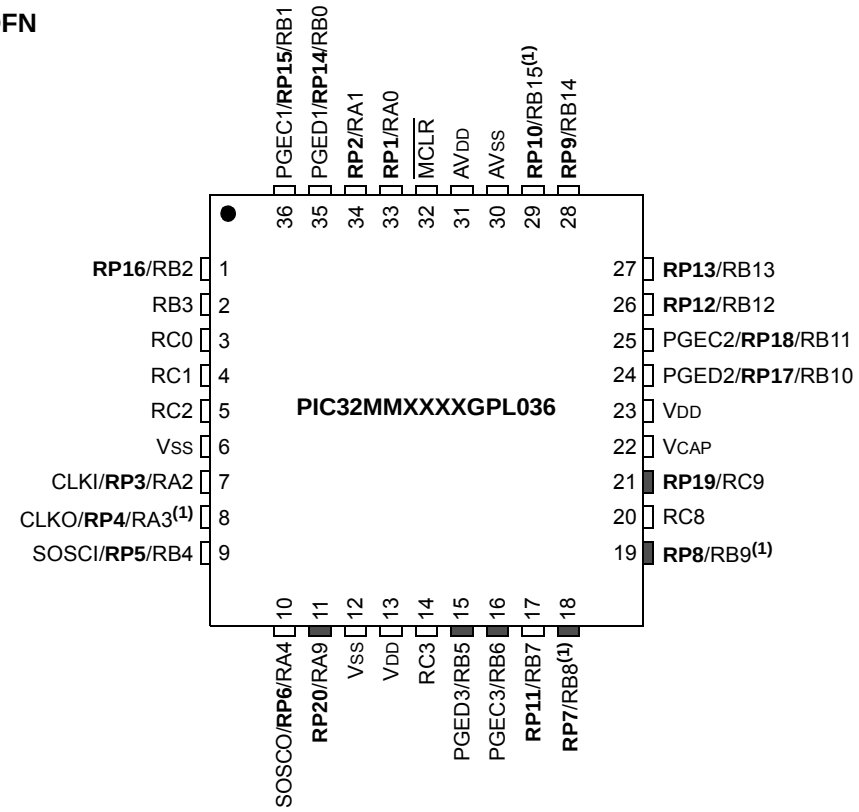
TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	15	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	16	**RP19**/RC9
3	AN4/C1INB/**RP16**/RB2	17	VCAP
4	AN11/C1INA/RB3	18	PGED2/TDO/**RP17**/RB10
5	VSS	19	PGEC2/TDI/**RP18**/RB11
6	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	20	AN7/LVDIN/**RP12**/RB12
7	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	21	AN8/**RP13**/RB13
8	SOSCI/**RP5**/RB4	22	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
9	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	23	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
10	VDD	24	AVSS
11	PGED3/RB5	25	AVDD
12	PGEC3/RB6	26	MCLR
13	**RP11**/RB7	27	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
14	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)	28	VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

36-Pin VQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN VQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP16**/RB2	19	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	AN11/C1INA/RB3	20	RC8
3	AN12/RC0	21	**RP19**/RC9
4	AN13/RC1	22	VCAP
5	RC2	23	VDD
6	VSS	24	PGED2/TDO/**RP17**/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	PGEC2/TDI/**RP18**/RB11
8	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	26	AN7/LVDIN/**RP12**/RB12
9	SOSCI/**RP5**/RB4	27	AN8/**RP13**/RB13
10	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	28	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
11	**RP20**/RA9	29	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
12	VSS	30	AVSS
13	VDD	31	AVDD
14	RC3	32	MCLR
15	PGED3/RB5	33	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	PGEC3/RB6	34	VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP11**/RB7	35	PGED1/AN2/C1IND/C2INB/**RP14**/RB0
18	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1

Note 1: Pin has an increased current drive strength.

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
PGEC1	2	5	2	5	36	39	I	ST	ICSP Port 1 programming clock input
PGEC2	19	2	19	22	25	28	I	ST	ICSP Port 2 programming clock input
PGEC3	7	10	12	15	16	16	I	ST	ICSP Port 3 programming clock input
PGED1	1	4	1	4	35	38	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	20	3	18	21	24	27	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	6	9	11	14	15	15	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	7	10	9	12	10	10	I	ST	Real-Time Clock 50/60 Hz clock input
RA0	19	2	27	2	33	36	I/O	ST/DIG	PORTA digital I/O
RA1	20	3	28	3	34	37	I/O	ST/DIG	PORTA digital I/O
RA2	4	7	6	9	7	7	I/O	ST/DIG	PORTA digital I/O
RA3	5	8	7	10	8	8	I/O	ST/DIG	PORTA digital I/O
RA4	7	10	9	12	10	10	I/O	ST/DIG	PORTA digital I/O
RA9	—	—	—	—	11	11	I/O	ST/DIG	PORTA digital I/O
RB0	1	4	1	4	35	38	I/O	ST/DIG	PORTB digital I/O
RB1	2	5	2	5	36	39	I/O	ST/DIG	PORTB digital I/O
RB2	3	6	3	6	1	1	I/O	ST/DIG	PORTB digital I/O
RB3	—	—	4	7	2	2	I/O	ST/DIG	PORTB digital I/O
RB4	6	9	8	11	9	9	I/O	ST/DIG	PORTB digital I/O
RB5	—	—	11	14	15	15	I/O	ST/DIG	PORTB digital I/O
RB6	—	—	12	15	16	16	I/O	ST/DIG	PORTB digital I/O
RB7	8	11	13	16	17	17	I/O	ST/DIG	PORTB digital I/O
RB8	9	12	14	17	18	18	I/O	ST/DIG	PORTB digital I/O
RB9	10	13	15	18	19	20	I/O	ST/DIG	PORTB digital I/O
RB10	—	—	18	21	24	27	I/O	ST/DIG	PORTB digital I/O
RB11	—	—	19	22	25	28	I/O	ST/DIG	PORTB digital I/O
RB12	12	15	20	23	26	29	I/O	ST/DIG	PORTB digital I/O
RB13	13	16	21	24	27	30	I/O	ST/DIG	PORTB digital I/O
RB14	14	17	22	25	28	31	I/O	ST/DIG	PORTB digital I/O
RB15	15	18	23	26	29	32	I/O	ST/DIG	PORTB digital I/O
RC0	—	—	—	—	3	3	I/O	ST/DIG	PORTC digital I/O
RC1	—	—	—	—	4	4	I/O	ST/DIG	PORTC digital I/O
RC2	—	—	—	—	5	5	I/O	ST/DIG	PORTC digital I/O
RC3	—	—	—	—	14	14	I/O	ST/DIG	PORTC digital I/O
RC8	—	—	—	—	20	21	I/O	ST/DIG	PORTC digital I/O
RC9	—	—	16	19	21	22	I/O	ST/DIG	PORTC digital I/O
REFCLKI	10	13	15	18	19	20	I	ST	Reference clock input
REFCLKO	15	18	23	26	29	32	O	DIG	Reference clock output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

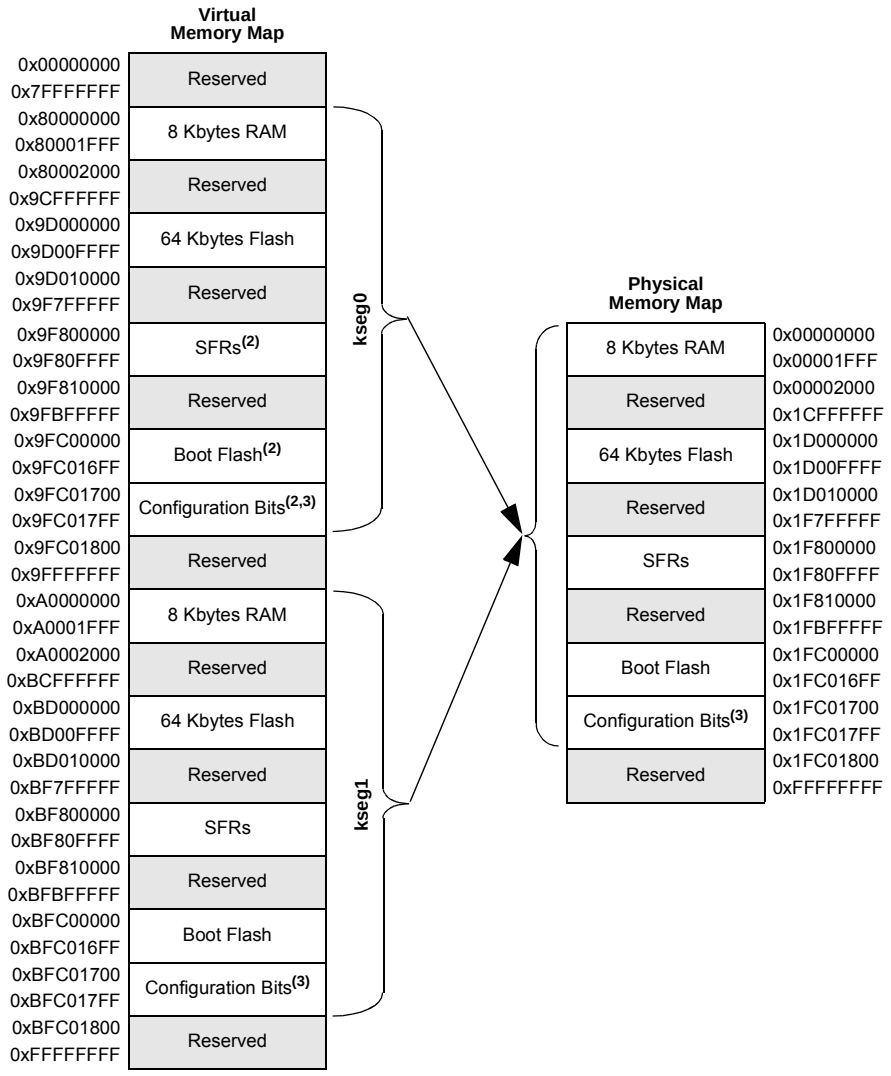
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 64 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

REGISTER 5-1: NVMCON: NVM PROGRAMMING CONTROL REGISTER (CONTINUED)

bit 3-0 **NVMOP<3:0>:** NVM Operation bits(3)

These bits are only writable when WREN = 0.

1111 = Reserved
•
•
•
1000 = Reserved
0111 = Program Erase Operation: Erases all of Program Flash Memory (all pages must be unprotected in the NVMPWP register, Boot Flash Memory is not erased)
0110 = Reserved
0101 = Reserved
0100 = Page Erase Operation: Erases page selected by NVMADDR (erases Boot or Program Flash Memory, page must be unprotected in the NVMBWP or NVMPWP register)
0011 = Row Program Operation: Programs row selected by NVMADDR (programs Boot or Program Flash Memory, page must be unprotected in the NVMBWP or NVMPWP register)
0010 = Double-Word Program Operation: Programs two words to the address selected by NVMADDR (programs Boot or Program Flash Memory, page must be unprotected in the NVMBWP or NVMPWP register)
0001 = Reserved
0000 = No operation, clears WRERR and LVDERR bits

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

2: These bits are cleared by setting NVMOP<3:0> = 0000 and initiating a Flash operation (i.e., WR).

3: NVMOP<3:0> bits are write-protected if the WREN bit is set.

4: Writes to the WR bit require an unlock sequence. Refer to **Section 5.1 "Flash Controller Registers Write Protection"** for details.

7.2 Interrupts

The PIC32MM0064GPL036 family uses fixed offset for vector spacing. For details, refer to **Section 8. "Interrupts"** (DS60001108) in the *"PIC32 Family Reference Manual"*. Table 7-2 provides the interrupt related vectors and bits information.

TABLE 7-2: INTERRUPTS

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
Core Timer	_CORE_TIMER_VECTOR	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software 0	_CORE_SOFTWARE_0_VECTOR	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software 1	_CORE_SOFTWARE_1_VECTOR	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External 0	_EXTERNAL_0_VECTOR	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
External 1	_EXTERNAL_1_VECTOR	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
External 2	_EXTERNAL_2_VECTOR	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	No
External 3	_EXTERNAL_3_VECTOR	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	No
External 4	_EXTERNAL_4_VECTOR	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
PORTA Change Notification	_CHANGE_NOTICE_A_VECTOR	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
PORTB Change Notification	_CHANGE_NOTICE_B_VECTOR	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
PORTC Change Notification	_CHANGE_NOTICE_C_VECTOR	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	No
Timer1	_TIMER_1_VECTOR	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	No
Comparator 1	_COMPARATOR_1_VECTOR	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
Comparator 2	_COMPARATOR_2_VECTOR	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Real-Time Clock Alarm	_RTCC_VECTOR	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
ADC Conversion	_ADC_VECTOR	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	No
CRC	_CRC_VECTOR	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
High/Low-Voltage Detect	_HLVD_VECTOR	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	Yes
Logic Cell 1	_CLC1_VECTOR	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Logic Cell 2	_CLC2_VECTOR	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
SPI1 Error	_SPI1_ERR_VECTOR	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
SPI1 Transmission	_SPI1_TX_VECTOR	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes
SPI1 Reception	_SPI1_RX_VECTOR	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	Yes

TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
UART1 Reception	_UART1_RX_VECTOR	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	Yes
UART1 Transmission	_UART1_TX_VECTOR	24	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	Yes
UART1 Error	_UART1_ERR_VECTOR	25	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	Yes
CCP1 Input Capture or Output Compare	_CCP1_VECTOR	29	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	No
CCP1 Timer	_CCT1_VECTOR	30	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	No
CCP2 Input Capture or Output Compare	_CCP2_VECTOR	31	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
CCP2 Timer	_CCT2_VECTOR	32	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
CCP3 Input Capture or Output Compare	_CCP3_VECTOR	33	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	No
CCP3 Timer	_CCT3_VECTOR	34	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	No
RESERVED	—	35	—	—	—	—	—
RESERVED	—	36	—	—	—	—	—
SPI2 Error	_SPI2_ERR_VECTOR	37	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
SPI2 Transmission	_SPI2_TX_VECTOR	38	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
SPI2 Reception	_SPI2_RX_VECTOR	39	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	Yes
UART2 Reception	_UART2_RX_VECTOR	40	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	Yes
UART2 Transmission	_UART2_TX_VECTOR	41	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
UART2 Error	_UART2_ERR_VECTOR	42	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
NVM Program or Erase Complete	_NVM_VECTOR	46	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
Core Performance Counter	_PERFORMANCE_COUNTER_VECTOR	47	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	No

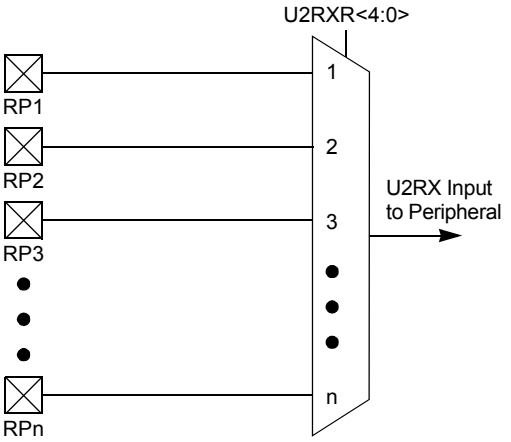
9.8.4 INPUT MAPPING

The RPINRx registers are used to assign the peripheral input to the required remappable pin, RPn (refer to the peripheral inputs and the corresponding RPINRx registers listed in Table 9-2). Each RPINRx register contains sets of 5-bit fields. Programming these bits with the remappable pin number will connect the peripheral to this RPn pin. Example 9-1 and Figure 9-2 illustrate the remappable pin selection for the U2RX input.

EXAMPLE 9-1: UART2 RX INPUT ASSIGNMENT TO RP9/RB14 PIN

```
RPINR9bits.U2RXR = 9; // connect UART2 RX
                      // input to RP9 pin
```

FIGURE 9-2: REMAPPABLE INPUT EXAMPLE FOR U2RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 9-2: INPUT PIN SELECTION

Input Name	Function Name	Register	Function Bits
External Interrupt 4	INT4	RPINR1	INT4R<4:0>
MCCP1 Input Capture	ICM1	RPINR2	ICM1R<4:0>
SCCP2 Input Capture	ICM2	RPINR2	ICM2R<4:0>
SCCP3 Input Capture	ICM3	RPINR3	ICM3R<4:0>
Output Compare Fault A	OCFA	RPINR5	OCFAR<4:0>
Output Compare Fault B	OCFB	RPINR5	OCFBR<4:0>
CCP Clock Input A	TCKIA	RPINR6	TCKIAR<4:0>
CCP Clock Input B	TCKIB	RPINR6	TCKIBR<4:0>
UART2 Receive	U2RX	RPINR9	U2RXR<4:0>
UART2 Clear-to-Send	$\overline{\text{U2CTS}}$	RPINR9	U2CTSR<4:0>
SPI2 Data Input	SDI2	RPINR11	SDI2R<4:0>
SPI2 Clock Input	SCK2IN	RPINR11	SCK2INR<4:0>
SPI2 Slave Select Input	SS2IN	RPINR11	SS2INR<4:0>
CLC Input A	CLCINA	RPINR12	CLCINAR<4:0>
CLC Input B	CLCINB	RPINR12	CLCINBR<4:0>

TABLE 9-7: PERIPHERAL PIN SELECT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2480	RPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	IOLOCK	—	—	—	—	—	—	—	—	—	—	—	0000
24A0	RPINR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0												INT4R<4:0>					0000
24B0	RPINR2	31:16	—	—	—	ICM2R<4:0>					—	—	—	ICM1R<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
24C0	RPINR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ICM3R<4:0>					0000
24E0	RPINR5	31:16	—	—	—	OCFBR<4:0>					—	—	—	OCFAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
24F0	RPINR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0				TCKIBR<4:0>					—	—	—	TCKIAR<4:0>					0000
2520	RPINR9	31:16	—	—	—	U2CTSR<4:0>					—	—	—	U2RXR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2540	RPINR11	31:16	—	—	—	—	—	—	—	—	—	—	—	SS2INR<4:0>					0000
		15:0	—	—	—	SCK2INR<4:0>					—	—	—	SDI2R<4:0>					0000
2550	RPINR12	31:16	—	—	—	CLCINBR<4:0>					—	—	—	CLCINAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2590	RPOR0	31:16					RP4R<3:0>				—	—	—	—	RP3R<3:0>				0000
		15:0	—	—	—	—	RP2R<3:0>				—	—	—	—	RP1R<3:0>				0000
25A0	RPOR1	31:16	—	—	—	—	RP8R<3:0>				—	—	—	—	RP7R<3:0>				0000
		15:0	—	—	—	—	RP6R<3:0>				—	—	—	—	RP5R<3:0>				0000
25B0	RPOR2	31:16	—	—	—	—	RP12R<3:0>				—	—	—	—	RP11R<3:0>				0000
		15:0	—	—	—	—	RP10R<3:0>				—	—	—	—	RP9R<3:0>				0000
25C0	RPOR3	31:16	—	—	—	—	RP16R<3:0>				—	—	—	—	RP15R<3:0>				0000
		15:0	—	—	—	—	RP14R<3:0>				—	—	—	—	RP13R<3:0>				0000
25D0	RPOR4	31:16	—	—	—	—	RP20R<3:0>				—	—	—	—	RP19R<3:0>				0000
		15:0	—	—	—	—	RP18R<3:0>				—	—	—	—	RP17R<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL(1)	—	—	—	—	—	SPIFE	ENHBUF(1)
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO(4)	MODE32	MODE16	SMP	CKE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP(3)	MSTEN	DISSDI(4)	STXISEL<1:0>		SRXISEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
- 1 = Framed SPI support is enabled ($\overline{SSx}$ pin is used as the FSYNC1 input/output)
- 0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ Pin bit (Framed SPI mode only)
- 1 = Frame sync pulse input (Slave mode)
- 0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
- 1 = Frame pulse is active-high
- 0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
- 1 = Slave select SPI support is enabled; the $\overline{SSx}$ pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
- 0 = Slave select SPI support is disabled

bit 27 **FRMSYPW:** Frame Sync Pulse-Width bit
- 1 = Frame sync pulse is one character wide
- 0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits

Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
- 111 = Reserved
- 110 = Reserved
- 101 = Generates a frame sync pulse on every 32 data characters
- 100 = Generates a frame sync pulse on every 16 data characters
- 011 = Generates a frame sync pulse on every 8 data characters
- 010 = Generates a frame sync pulse on every 4 data characters
- 001 = Generates a frame sync pulse on every 2 data characters
- 000 = Generates a frame sync pulse on every data character

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 15-1: RTCCON1: RTCC CONTROL 1 REGISTER (CONTINUED)

bit 11 **WRLOCK:** RTCC Registers Write Lock bit(2)
1 = Registers associated with accurate timekeeping are locked
0 = Registers associated with accurate timekeeping may be written to by user

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin
0 = RTCC clock output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Signal Output Selection bits
111 = Reserved
• • •
011 = Reserved
010 = RTCC input clock source
001 = Seconds clock
000 = Alarm event

bit 3-0 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: To clear this bit, an unlock sequence is required. Refer to **Section 23.4 "System Registers Write Protection"** for details.

NOTES:

21.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 21-1) completely controls the operation of the HLVD module. This allows the circuitry to be “turned off” by the user under software control, which minimizes the current consumption for the device.

FIGURE 21-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM

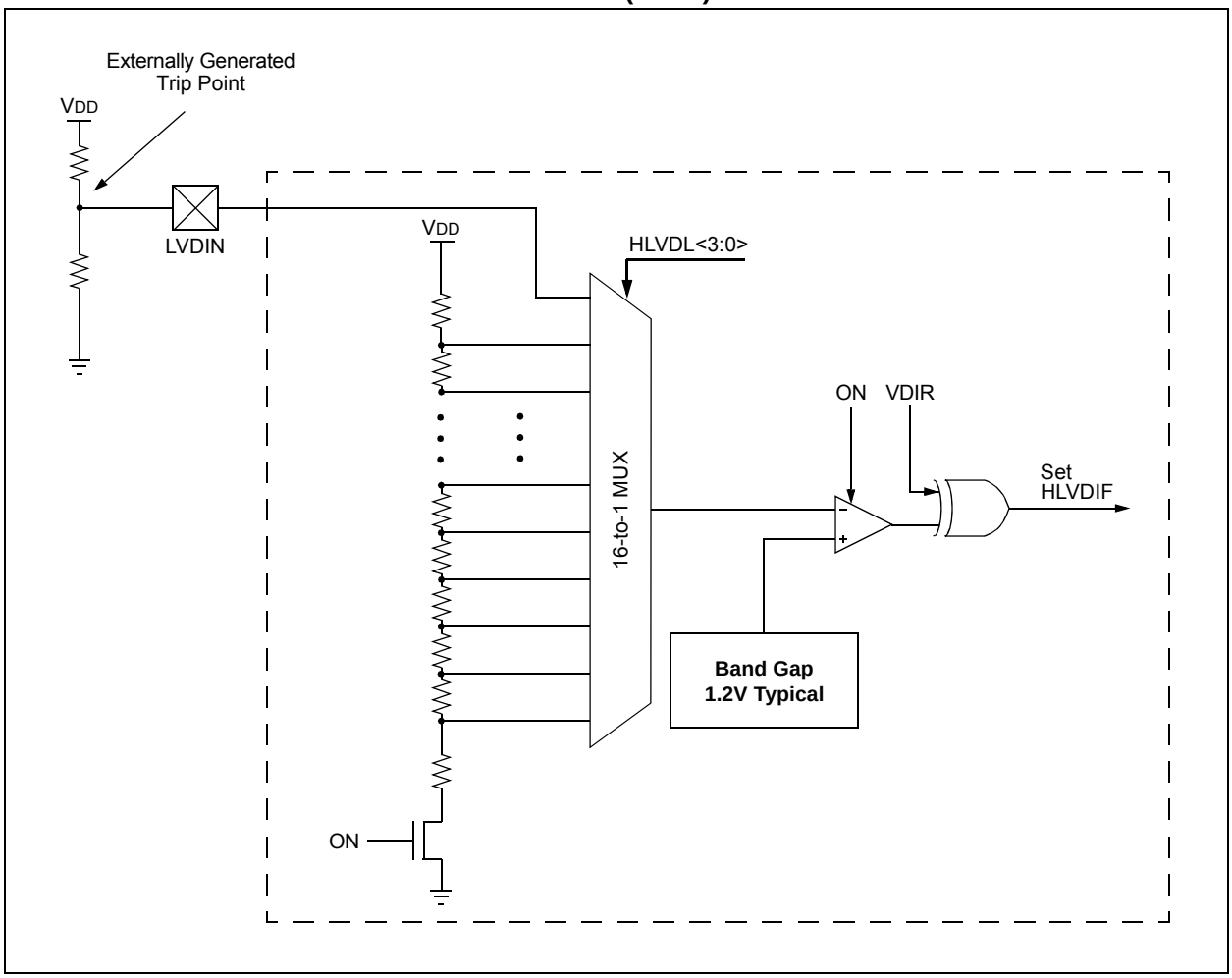


TABLE 23-4: ALTERNATE CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
1740	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1744	AFDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
1748	AFICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
174C	AFPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
1750	AFWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
1754	AFOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
1758	AFSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
175C	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1760	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1764	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

TABLE 23-5: RAM CONFIGURATION, DEVICE ID AND SYSTEM LOCK REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3B00	CFGCON	31:16	—	—	—	—	—	—	—	—	EXECADDR<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	—	—	—	000x
3B20	DEVID	31:16	VER<3:0>				ID<27:16>												xxxx
		15:0	ID<15:0>																xxxx
3B30	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0001

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

TABLE 26-8: I/O PIN INPUT SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage(2)**					
DI10		I/O Pins with ST Buffer	VSS	—	0.2 VDD	V	
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI16		OSC1/CLKI (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSC1/CLKI (HS mode)	VSS	—	0.2 VDD	V	
	VIH	**Input High Voltage(2)**					
DI20		I/O Pins with ST Buffer:					
		without 5V Tolerance	0.8 VDD	—	VDD	V	
		with 5V Tolerance	0.8 VDD	—	5.5	V	
DI25		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
DI26		OSCI/CLKI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSC1/CLKI (HS mode)	0.7 VDD	—	VDD	V	
DI30	ICNPU	**CNPUx Pull-up Current**	—	350	—	µA	VPIN = 0V, VDD = 3.3V
DI30A	ICNPD	**CNPDx Pull-Down Current**	—	300	—	µA	VPIN = 3.3V, VDD = 3.3V
	IIL	**Input Leakage Current**					
DI50		I/O Pins – 5V Tolerant	—	0.1	1.0	µA	VPIN = 3.3V, VDD = 3.3V, pin at high-impedance
DI51		I/O Pins – Not 5V Tolerant	—	0.1	1.0	µA	VPIN = 3.3V, VDD = 3.3V, pin at high-impedance
DI55		$\overline{\text{MCLR}}$	—	0.1	1.0	µA	VPIN = 3.3V, VDD = 3.3V
DI56		OSC1/CLKI	—	0.1	1.0	µA	VPIN = 3.3V, VDD = 3.3V

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Refer to Table 1-1 for I/O pin buffer types.

FIGURE 26-3: EXTERNAL CLOCK TIMING

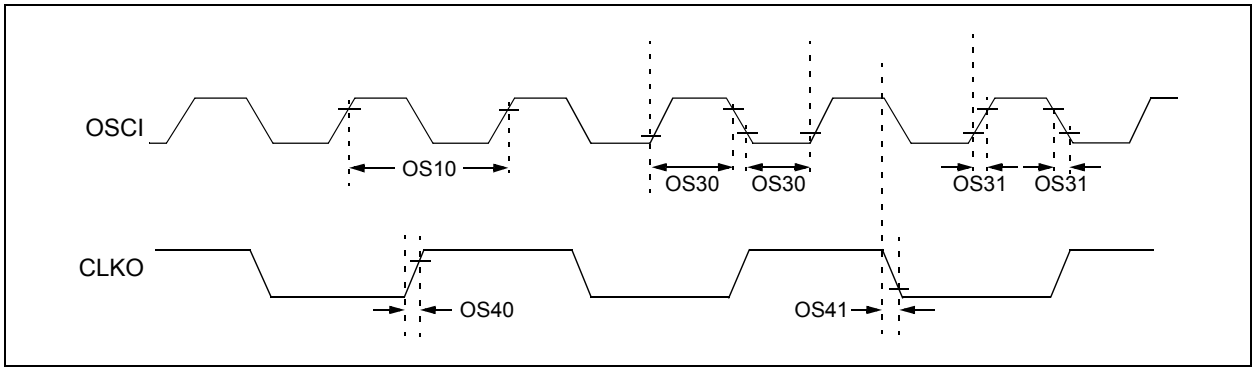


TABLE 26-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency	DC 2	— —	25 12.5	MHz MHz	EC ECPLL(2)
		Oscillator Frequency	3.5 3.5 10 10 31	— — — — —	10 10 25 25 50	MHz MHz MHz MHz kHz	XT XTPLL(2) HS HSPLL(2) SOSC
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x TOSC	—	0.55 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	15	20	ns	
OS41	TckF	CLKO Fall Time(3)	—	15	20	ns	

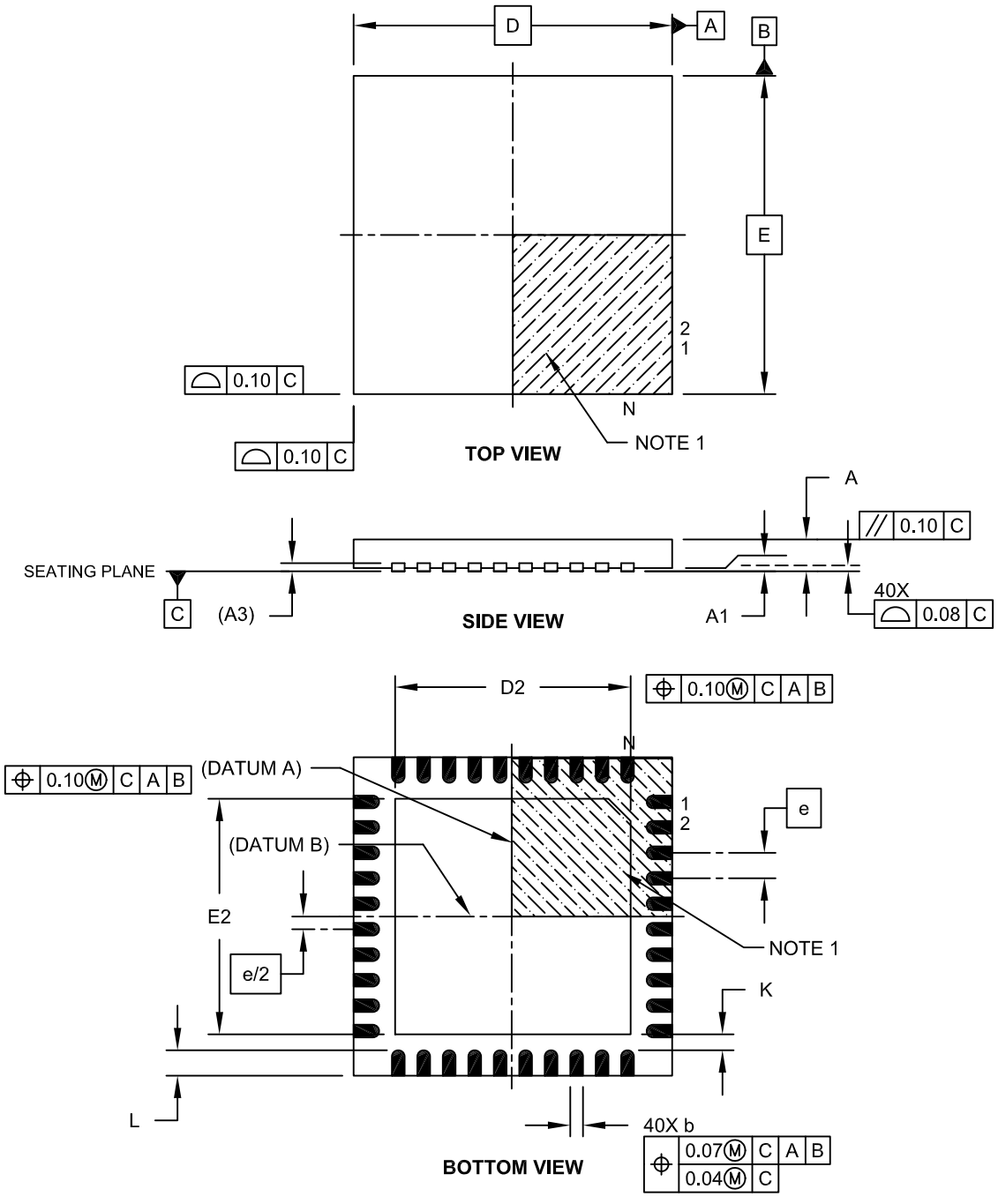
Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: PLL dividers and postscalers must be configured so that the system clock frequency does not exceed the maximum operating frequency.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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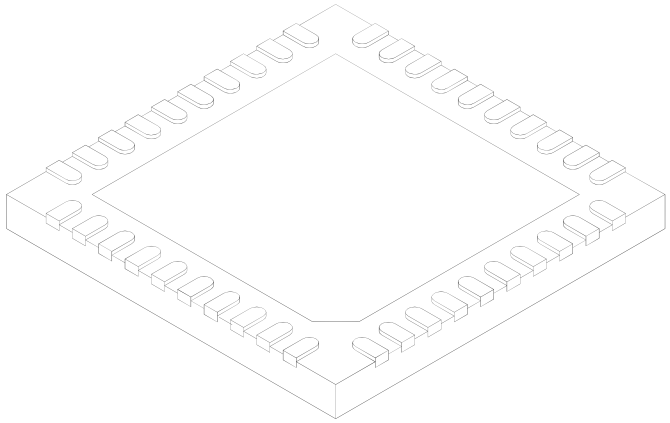
40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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