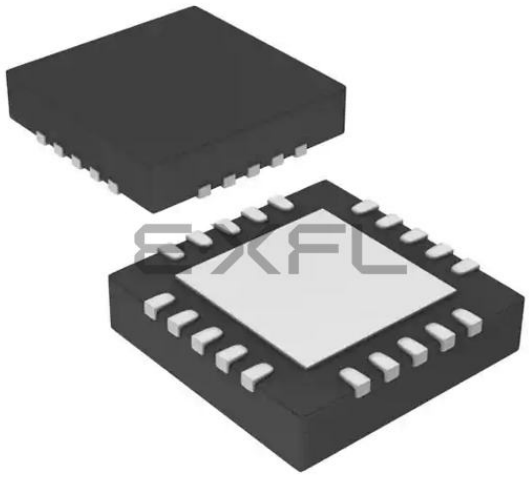
Microchip Technology - PIC32MM0064GPL020T-I/ML Datasheet



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What is "Embedded - Microcontrollers"?

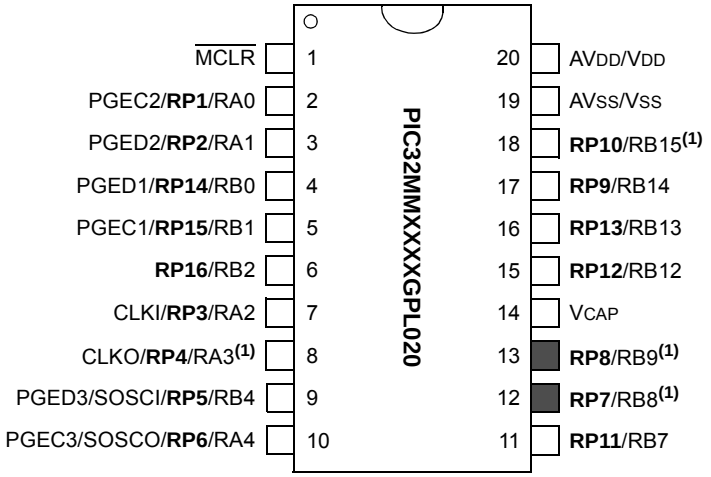
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl020t-i-ml

Pin Diagrams

20-Pin SSOP



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN SSOP DEVICES

Pin	Function	Pin	Function
1	$\overline{\text{MCLR}}$	11	**RP11**/RB7
2	PGEC2/VREF+/AN0/**RP1**/OCM1E/INT3/RA0	12	TCK/**RP7**/$\overline{\text{U1CTS}}$/SCK1/OCM1A/RB8(1)
3	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	13	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
4	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	14	VCAP
5	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	15	TDO/AN7/LVDIN/**RP12**/RB12
6	AN4/**RP16**/RB2	16	TDI/AN8/**RP13**/RB13
7	OSC1/CLKI/AN5/C1INB/**RP3**/OCM1C/RA2	17	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
8	OSC2/CLKO/AN6/C1INA/**RP4**/OCM1D/RA3(1)	18	AN10/REFCLKO/**RP10**/U1RX/$\overline{\text{SS1}}$/FSYNC1/INT0/RB15(1)
9	PGED3/SOSCI/**RP5**/RB4	19	AVSS/VSS
10	PGEC3/SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	20	AVDD/VDD

Note 1: Pin has an increased current drive strength.

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
RP1	19	2	27	2	33	36	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	20	3	28	3	34	37	I/O	ST/DIG	
RP3	4	7	6	9	7	7	I/O	ST/DIG	
RP4	5	8	7	10	8	8	I/O	ST/DIG	
RP5	6	9	8	11	9	9	I/O	ST/DIG	
RP6	7	10	9	12	10	10	I/O	ST/DIG	
RP7	9	12	14	17	18	18	I/O	ST/DIG	
RP8	10	13	15	18	19	20	I/O	ST/DIG	
RP9	14	17	22	25	28	31	I/O	ST/DIG	
RP10	15	18	23	26	29	32	I/O	ST/DIG	
RP11	8	11	13	16	17	17	I/O	ST/DIG	
RP12	12	15	20	23	26	29	I/O	ST/DIG	
RP13	13	16	21	24	27	30	I/O	ST/DIG	
RP14	1	4	1	4	35	38	I/O	ST/DIG	
RP15	2	5	2	5	36	39	I/O	ST/DIG	
RP16	3	6	3	6	1	1	I/O	ST/DIG	
RP17	—	—	18	21	24	27	I/O	ST/DIG	
RP18	—	—	19	22	25	28	I/O	ST/DIG	
RP19	—	—	16	19	21	22	I/O	ST/DIG	
RP20	—	—	—	—	11	11	I/O	ST/DIG	
RTCC	14	17	22	25	28	31	O	DIG	Real-Time Clock alarm/seconds output
SCK1	9	12	14	17	18	18	I/O	ST/DIG	SPI1 clock (input or output)
SCLKI	7	10	9	12	10	10	I	ST	Secondary Oscillator external clock input
SDI1	14	17	22	25	28	31	I	ST	SPI1 data input
SDO1	10	13	15	18	19	20	O	DIG	SPI1 data output
SOSCI	6	9	8	11	9	9	—	—	Secondary Oscillator crystal
SOSCO	7	10	9	12	10	10	—	—	Secondary Oscillator crystal
$\overline{SS1}$	15	18	23	26	29	32	I	ST	SPI1 slave select input
T1CK	10	13	15	18	19	20	I	ST	Timer1 external clock input
T1G	10	13	15	18	19	20	I	ST	Timer1 clock gate input
TCK	9	12	14	17	18	18	I	ST	JTAG clock input
TDI	13	16	19	22	25	28	I	ST	JTAG data input
TDO	12	15	18	21	24	27	O	DIG	JTAG data output
TMS	10	13	15	18	19	20	I	ST	JTAG mode select input
U1BCLK	10	13	15	18	19	20	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{U1CTS}$	9	12	14	17	18	18	I	ST	UART1 transmission control input
$\overline{U1RTS}$	10	13	15	18	19	20	O	DIG	UART1 reception control output
U1RX	15	18	23	26	29	32	I	ST	UART1 receive data input
U1TX	14	17	22	25	28	31	O	DIG	UART1 transmit data output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	WDTR
23:16	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SWNMI	—	—	—	GNMI	—	CF	WDTS
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **WDTR:** Watchdog Timer Time-out in Run Mode Flag bit
1 = A Run mode WDT time-out has occurred and caused an NMI
0 = WDT time-out has not occurred
Setting this bit will cause a WDT NMI event and NMICNT<15:0> will begin counting.

bit 23 **SWNMI:** Software NMI Trigger bit
1 = An NMI has been generated
0 = An NMI was not generated

bit 22-20 **Unimplemented:** Read as '0'

bit 19 **GNMI:** Software General NMI Trigger bit
1 = A general NMI has been generated
0 = A general NMI was not generated

bit 18 **Unimplemented:** Read as '0'

bit 17 **CF:** Clock Fail Detect bit
1 = FSCM has detected clock failure and caused an NMI
0 = FSCM has not detected clock failure
Setting this bit will cause a CF NMI event, but will not cause a clock switch to the FRC.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from Sleep
0 = WDT time-out has not occurred during Sleep mode
Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI Reset counter.
FFFFh-0001h = Number of SYSCLK cycles before a device Reset occurs(2)
0000h = No delay between NMI assertion and device Reset event

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

2: If a Watchdog Timer NMI event (when not in Sleep mode) is cleared before this counter reaches '0', no device Reset is asserted. This NMI Reset counter is only applicable to the Watchdog Timer NMI event.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F1C0	IPC8	31:16	—	—	—	—	—	—	—	—	—	—	—	CCT3IP<2:0>			CCT3IS<1:0>		0000
		15:0	—	—	—	CCP3IP<2:0>			CCP3IS<1:0>		—	—	—	CCT2IP<2:0>			CCT2IS<1:0>		0000
F1D0	IPC9	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
		15:0	—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		—	—	—	—	—	—	—	—	0000
F1E0	IPC10	31:16	—	—	—	—	—	—	—	—	—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
		15:0	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
F1F0	IPC11	31:16	—	—	—	CPCIP<2:0>			CPCIS<1:0>		—	—	—	NVMIP<2:0>			NVMIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 20-pin devices.

REGISTER 8-2: SPLLCON: SYSTEM PLL CONTROL REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-y	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PLLICLK	—	—	—	—	—	—	—

Legend:	y = Values set from Configuration bits on Reset		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits
- 111 = PLL divide-by-256
- 110 = PLL divide-by-64
- 101 = PLL divide-by-32
- 100 = PLL divide-by-16
- 011 = PLL divide-by-8
- 010 = PLL divide-by-4
- 001 = PLL divide-by-2
- 000 = PLL divide-by-1 (default setting)

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits
- 111111-0000111 = Reserved
- 0000110 = 24x
- 0000101 = 12x
- 0000100 = 8x
- 0000011 = 6x
- 0000010 = 4x
- 0000001 = 3x (default setting)
- 0000000 = 2x

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PLLICLK:** System PLL Input Clock Source bit
- 1 = FRC is selected as the input to the system PLL (not divided)
- 0 = POSC is selected as the input to the system PLL

The POR default value is specified by the PLLSRC Configuration bit in the FOSCSEL register. Refer to Register 23-9 in **Section 23.0 "Special Features"** for more information.

bit 6-0 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details. All bits in this register must be modified only if the PLL is not used.

TABLE 9-5: PORTB REGISTER MAP

Virtual Address (BF80_#)	Register Name(2)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2700	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB<15:12>				—	—	—	—	—	—	—	—	ANSB<3:0>(1)				F00F
2710	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB<15:0>(1)																FFFF
2720	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB<15:0>(1)																0000
2730	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB<15:0>(1)																0000
2740	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB<15:0>(1)																0000
2750	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB<15:0>(1)																0000
2760	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB<15:0>(1)																0000
2770	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—	0000
2780	CNEN0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB<15:0>(1)																0000
2790	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATB<15:0>(1)																0000
27A0	CNEN1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1B<15:0>(1)																0000
27B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB<15:0>(1)																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits<11:10,6:5,3> are not implemented in 20-pin devices.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 9-1: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER (x = A-C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	CNSTYLE	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notification (CN) Control On bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit
1 = Edge style (detects edge transitions, CNFx bits are used for a Change Notice event)
0 = Mismatch style (detects change from last PORTx read, CNSTATx bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 10-1: T1CON: TIMER1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer1 On bit
1 = Timer1 is enabled
0 = Timer1 is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer1 Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer mode functionality)

bit 11 **TWIP:** Asynchronous Timer1 Write in Progress bit
In Asynchronous Timer1 mode:
1 = Asynchronous write to TMR1 register is in progress
0 = Asynchronous write to TMR1 register is complete
In Synchronous Timer1 mode:
This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK Pin
00 = External clock comes from the Secondary Oscillator (SOSC)

bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

REGISTER 16-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 7-4 **SSRC<3:0>:** Conversion Trigger Source Select bits
1111-1101 = Reserved
1100 = CLC2 module event ends sampling and starts conversion
1011 = CLC1 module event ends sampling and starts conversion
1010 = SCCP3 module event ends sampling and starts conversion
1001 = SCCP2 module event ends sampling and starts conversion
1000 = MCCP1 module event ends sampling and starts conversion
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = Timer1 period match ends sampling and starts conversion (can trigger during Sleep mode)
0101 = Timer1 period match ends sampling and starts conversion (will not trigger during Sleep mode)
0100-0010 = Reserved
0001 = Active transition on INT0 pin ends sampling and starts conversion
0000 = Clearing the SAMP bit ends sampling and starts conversion

bit 3 **MODE12:** 12-Bit Operation Mode bit
1 = 12-bit ADC operation
0 = 10-bit ADC operation

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(1)
1 = The ADC Sample-and-Hold Amplifier (SHA) is sampling
0 = The ADC Sample-and-Hold Amplifier is holding

bit 0 **DONE:** ADC Conversion Status bit(2)
1 = Analog-to-Digital conversion is done
0 = Analog-to-Digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

Note 1: The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).
2: The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.

REGISTER 16-4: AD1CON5: ADC CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	ASEN(1)	LPEN	—	BGREQ	—	—	ASINT<1:0>(2)	
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WM<1:0>		CM<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ASEN:** Auto-Scan Enable bit(1)
- 1 = Auto-scan is enabled
- 0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
- 1 = Low power is enabled after scan
- 0 = Full power is enabled after scan

bit 13 **Unimplemented:** Read as '0'

bit 12 **BGREQ:** Band Gap Request bit
- 1 = Band gap is enabled when the ADC is enabled and active
- 0 = Band gap is not enabled by the ADC

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits(2)
- 11 = Interrupt after Threshold Detect sequence has completed and a valid compare has occurred
- 10 = Interrupt after valid compare has occurred
- 01 = Interrupt after Threshold Detect sequence has completed
- 00 = No interrupt

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **WM<1:0>:** Write Mode bits
- 11 = Reserved
- 10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CM<1:0> and ASINT<1:0> bits)
- 01 = Convert and save (conversion results saved to ADC1BUFx registers when a match occurs, as defined by the CM<1:0> bits)
- 00 = Threshold (Comparison) mode is disabled, legacy operation (conversion data saved to ADC1BUFx registers)

Note 1: When auto-scan is enabled (ASEN (AD1CON5<15>) = 1), the CSCNA (AD1CON2<10>) and SMPI<3:0> (AD1CON2<5:2>) bits are ignored.

2: The ASINT<1:0> bits setting only takes effect when ASEN (AD1CON5<15>) = 1. Interrupt generation is governed by the SMPI<3:0> bits field.

REGISTER 16-5: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA<2:0>			CH0SA<4:0>(1)				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-5 **CH0NA<2:0>:** Negative Input Select bits
111-001 = Reserved
000 = Negative input is AVSS

bit 4-0 **CH0SA<4:0>:** Positive Input Select bits(1)
11111 = Reserved
11110 = Positive input is AVDD
11101 = Positive input is AVSS
11100 = Positive input is Band Gap Reference (VBG)
11011-01110 = Reserved
01101 = Positive input is AN13(2,3)
01100 = Positive input is AN12(2,3)
01011 = Positive input is AN11(2)
01010 = Positive input is AN10
01001 = Positive input is AN9
01000 = Positive input is AN8
00111 = Positive input is AN7
00110 = Positive input is AN6
00101 = Positive input is AN5
00100 = Positive input is AN4
00011 = Positive input is AN3
00010 = Positive input is AN2
00001 = Positive input is AN1
00000 = Positive input is AN0

Note 1: The CH0SA<4:0> positive input selection is only used when CSCNA (AD1CON2<10>) = 0 and ASEN (AD1CON5<15>) = 0. The AD1CSS bits specify the positive inputs when CSCNA = 1 or ASEN = 1.

2: This option is not implemented in the 20-pin devices.

3: This option is not implemented in the 28-pin devices.

REGISTER 17-1: CRCCON: CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DWIDTH<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
15:8	R/W-0	U-0	R/W-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ON	—	SIDL	VWORD<4:0>				
7:0	R-0, HS, HC	R-1, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	MOD	—	—

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **DWIDTH<4:0>:** Data Word Width Configuration bits
Configures the width of the data word (Data Word Width – 1).

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **PLEN<4:0>:** Polynomial Length Configuration bits
Configures the length of the polynomial (Polynomial Length – 1).

bit 15 **ON:** CRC Enable bit
1 = Enables module
0 = Disables module

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** CRC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Counter Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 16 when DWIDTH<4:0> ≤ (data words, 8-bit wide or less). Has a maximum value of 8 when DWIDTH<4:0> ≤ 15 (data words from 9 to 16-bit wide). Has a maximum value of 4 when DWIDTH<4:0> ≤ 31 (data words from 17 to 32-bit wide).

bit 7 **CRCFUL:** CRC FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

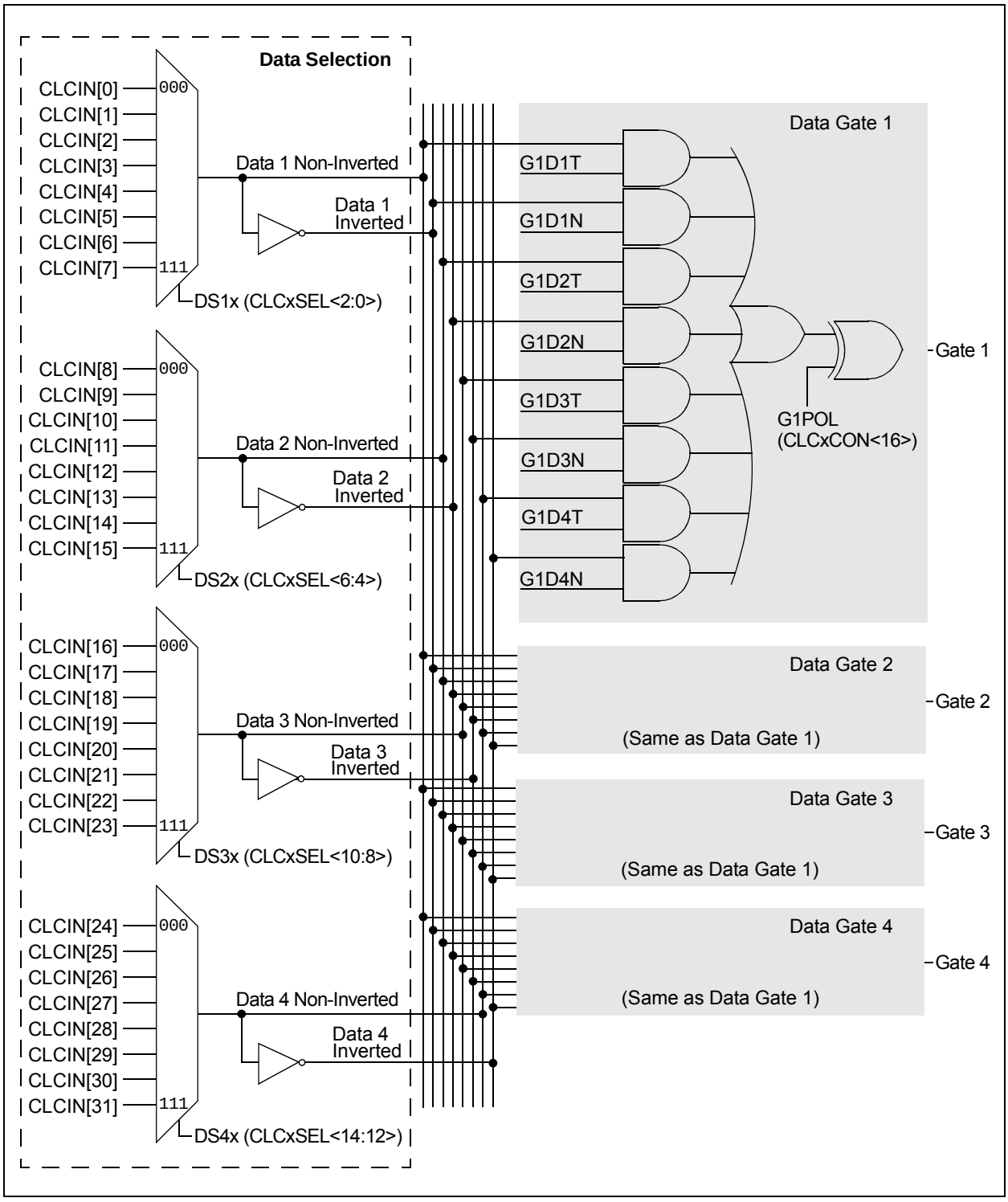
bit 6 **CRCMPT:** CRC FIFO Empty bit
1 = FIFO is empty
0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit
1 = Interrupt on FIFO is empty; final word of data is still shifted through CRC
0 = Interrupt on shift is complete (FIFO is empty and no data is shifted from the shift buffer)

bit 4 **CRCGO:** Start CRC bit
1 = Starts CRC serial shifter; clearing the bit aborts shifting
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
1 = Data word is shifted into the CRC, starting with the LSb (little-endian); reflected input data
0 = Data word is shifted into the CRC, starting with the MSb (big-endian); non-reflected input data

FIGURE 18-3: CLCx INPUT SOURCE SELECTION DIAGRAM



23.9 Configuration Words and System Registers

TABLE 23-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
17D4	FOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

REGISTER 23-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	r-0	U-0	r-0	r-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EXECADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-y	U-0	r-1	r-1
	—	—	—	—	JTAGEN	—	—	—

Legend:	r = Reserved bit	y = Value set from Configuration bits on Reset
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **Reserved:** Must be written as '0'

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **Reserved:** Must be written as '0'

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits

11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)
•
•
•
00000010 = RAM program space starts at the 2-Kbyte boundary (from 0xA0000800)
00000001 = RAM program space starts at the 1-Kbyte boundary (from 0xA0000400)
00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit

1 = JTAG port is enabled
0 = JTAG port is disabled
The Reset value of this bit is the value of the JTAGEN (FICD<2>) Configuration bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Must be written as '1'

TABLE 26-5: IDLE CURRENT (I_{IDLE})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC40	0.26	0.46	mA	2.0V	FSYS = 1 MHz
	0.26	0.46	mA	3.3V	
DC41	0.85	1.5	mA	2.0V	FSYS = 8 MHz
	0.85	1.5	mA	3.3V	
DC42	2.3	3.7	mA	2.0V	FSYS = 25 MHz
	2.3	3.7	mA	3.3V	
DC44	0.18	0.34	mA	2.0V	FSYS = 32 kHz
	0.18	0.34	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = `010` and POSCMOD<1:0> (FOSCSEL<9:8>) = `00`)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = `1`)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = `00`)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = `0` and SOSCSEL (FOSCSEL<12>) = `0`)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = `00` and LPBOREN (FPOR<3>) = `0`)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = `0`)
- All I/O pins (excepting OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

FIGURE 26-3: EXTERNAL CLOCK TIMING

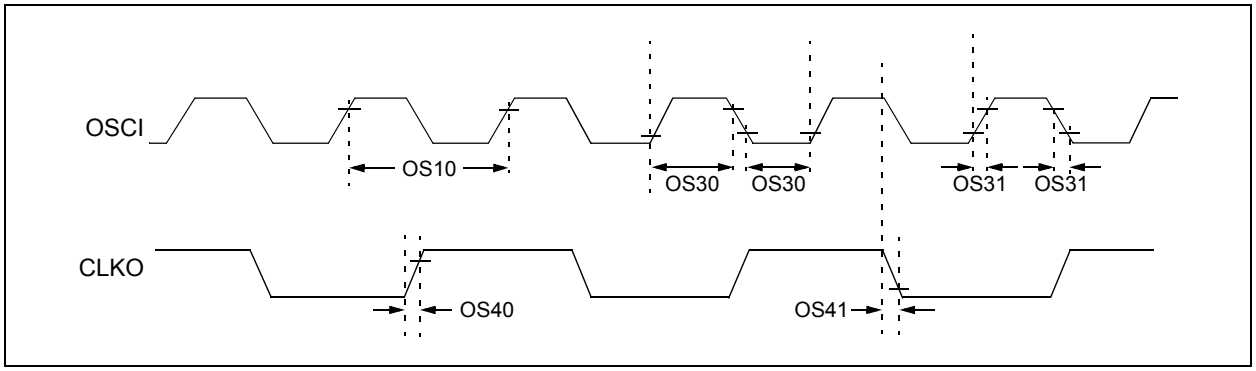


TABLE 26-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency	DC 2	— —	25 12.5	MHz MHz	EC ECPLL(2)
		Oscillator Frequency	3.5 3.5 10 10 31	— — — — —	10 10 25 25 50	MHz MHz MHz MHz kHz	XT XTPLL(2) HS HSPLL(2) SOSC
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x TOSC	—	0.55 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	15	20	ns	
OS41	TckF	CLKO Fall Time(3)	—	15	20	ns	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: PLL dividers and postscalers must be configured so that the system clock frequency does not exceed the maximum operating frequency.

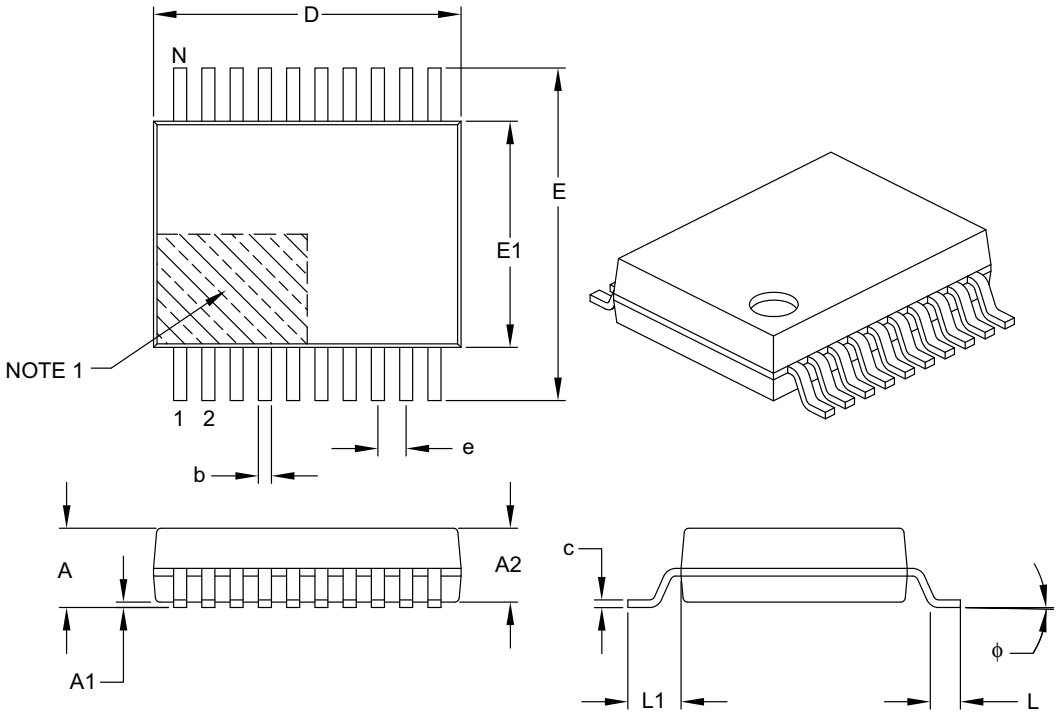
3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

27.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

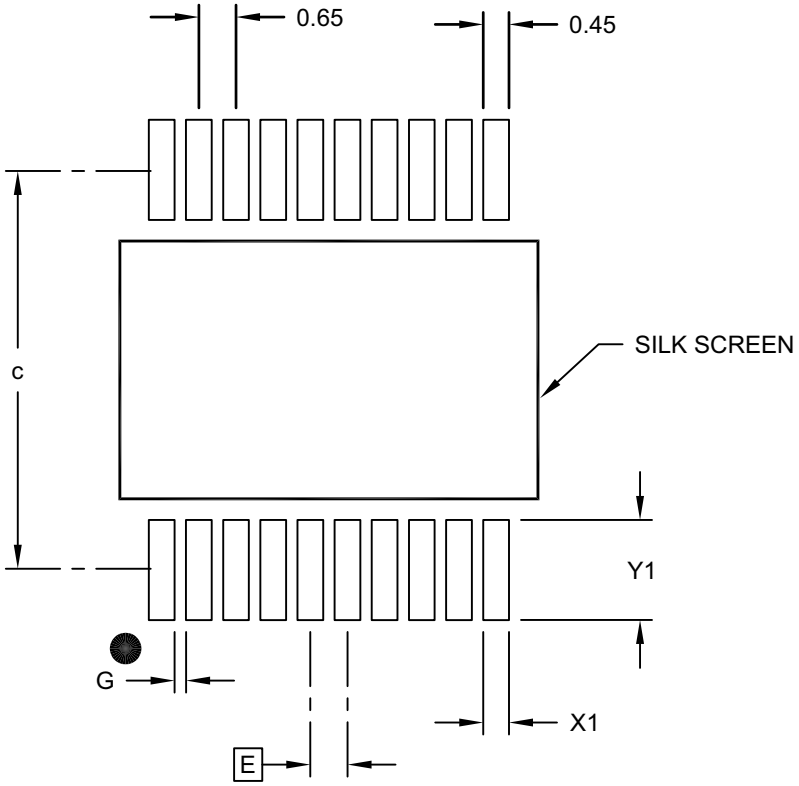
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072B

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