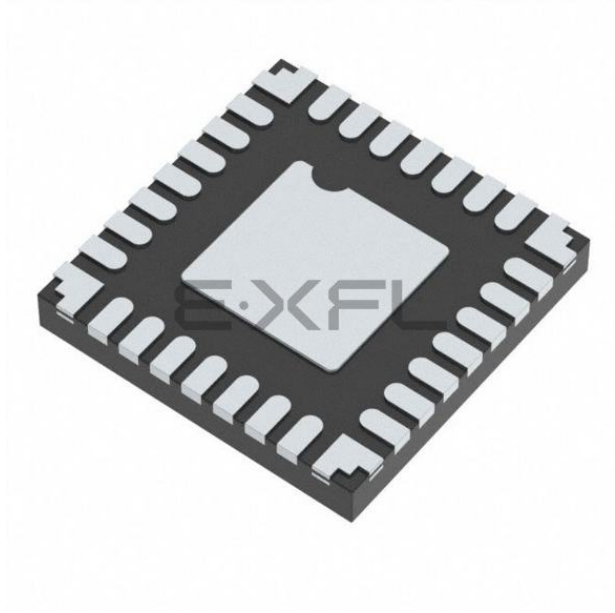

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028-e-m6

Analog Features

- Two Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit DAC with Output Pin
- Up to 14-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit, 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit, 300K samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0064GPL036 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (Channels)	Comparators	CRC	RTCC	JTAG	Packages
							UART(1)/LIN/J2602	16-Bit Timers	MCCP(3)	SCCP(4)	CLC	SPI(2)/I2S						
PIC32MM0016GPL020	20	16	4	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0032GPL020	20	32	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0064GPL020	20	64	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0016GPL028	28	16	4	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/SOIC/ QFN/UQFN
PIC32MM0032GPL028	28	32	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/ SOIC/ QFN/UQFN
PIC32MM0064GPL028	28	64	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SPDIP/SSOP/ SOIC/QFN/ UQFN
PIC32MM0016GPL036	36/40	16	4	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0032GPL036	36/40	32	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0064GPL036	36/40	64	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN

Note 1: UART1 has assigned pins. UART2 is remappable.

2: SPI1 has assigned pins. SPI2 is remappable.

3: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

3.3 Power Management

The processor core offers a number of power management features, including low-power design, active power management and Power-Down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during Idle periods.

The mechanism for invoking Power-Down mode is implemented through execution of the WAIT instruction. The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MM family makes extensive use of local gated clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The microAptiv UC core has an Enhanced JTAG (EJTAG) interface for use in the software debug. In addition to the standard mode of operation, the microAptiv UC core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the microAptiv UC core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

3.5 MIPS32® microAptiv™ UC Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the microAptiv UC core, which is included on PIC32MM0064GPL036 family devices.

6.0 RESETS

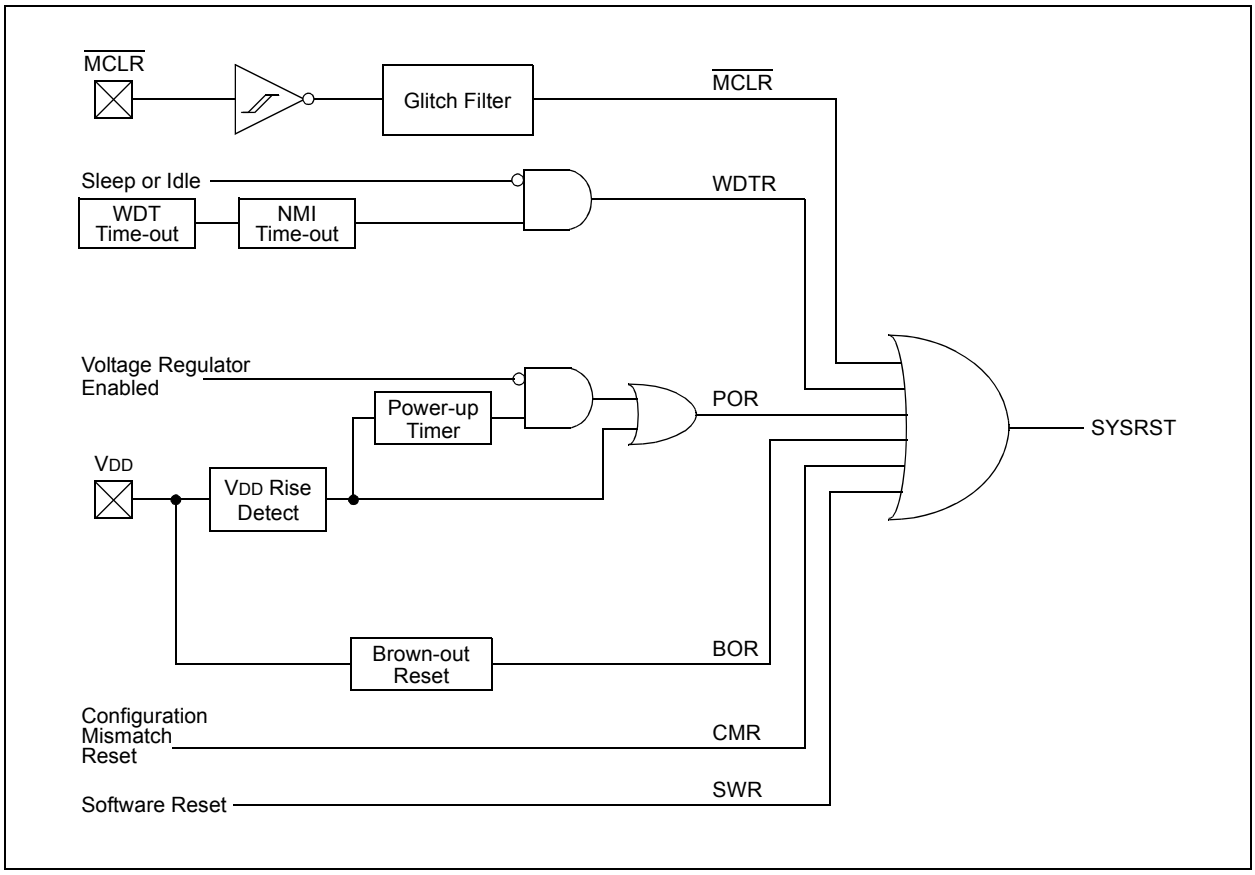
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset Pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 3 **SLEEP:** Wake from Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake from Idle Flag bit(2)
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear bits in this register to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep mode.

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enables Software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 23.4 "System Registers Write Protection"** for details.
2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FRCDIV<2:0>		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>(3)			—	NOSC<2:0>(3)		
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0, HS	U-0	R/W-y	R/W-y
	CLKLOCK	—	—	SLPEN	CF	—	SOSCEN(4)	OSWEN(2)

Legend:	HS = Hardware Settable bit	y = Value set from Configuration bits on Reset
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits
- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2
- 000 = FRC divided by 1 (default setting)

bit 23-15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits(3)
- 111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by the FRCDIV<2:0> bits (FRCDIV))
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Reserved
- 010 = Primary Oscillator (POSC) (XT, HS or EC)
- 001 = System PLL (SPLL)
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

bit 11 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

2: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

3: The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.

4: The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(3)
- 111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Reserved
- 010 = Primary Oscillator (POSC) (XT, HS or EC)
- 001 = System PLL (SPLL)
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit(4)
- 1 = Enables Secondary Oscillator
- 0 = Disables Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit(2)
- 1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits
- 0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

2: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

3: The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.

4: The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

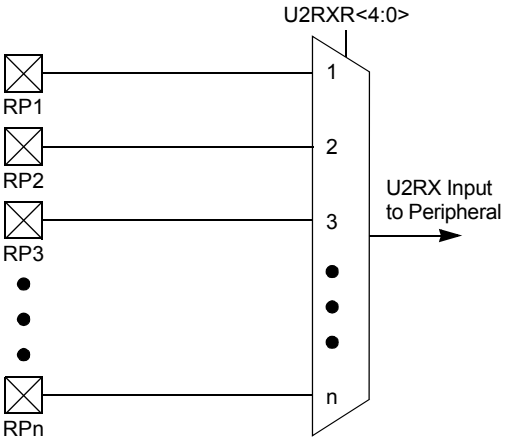
9.8.4 INPUT MAPPING

The RPINRx registers are used to assign the peripheral input to the required remappable pin, RPn (refer to the peripheral inputs and the corresponding RPINRx registers listed in Table 9-2). Each RPINRx register contains sets of 5-bit fields. Programming these bits with the remappable pin number will connect the peripheral to this RPn pin. Example 9-1 and Figure 9-2 illustrate the remappable pin selection for the U2RX input.

EXAMPLE 9-1: UART2 RX INPUT ASSIGNMENT TO RP9/RB14 PIN

```
RPINR9bits.U2RXR = 9; // connect UART2 RX
                      // input to RP9 pin
```

FIGURE 9-2: REMAPPABLE INPUT EXAMPLE FOR U2RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 9-2: INPUT PIN SELECTION

Input Name	Function Name	Register	Function Bits
External Interrupt 4	INT4	RPINR1	INT4R<4:0>
MCCP1 Input Capture	ICM1	RPINR2	ICM1R<4:0>
SCCP2 Input Capture	ICM2	RPINR2	ICM2R<4:0>
SCCP3 Input Capture	ICM3	RPINR3	ICM3R<4:0>
Output Compare Fault A	OCFA	RPINR5	OCFAR<4:0>
Output Compare Fault B	OCFB	RPINR5	OCFBR<4:0>
CCP Clock Input A	TCKIA	RPINR6	TCKIAR<4:0>
CCP Clock Input B	TCKIB	RPINR6	TCKIBR<4:0>
UART2 Receive	U2RX	RPINR9	U2RXR<4:0>
UART2 Clear-to-Send	$\overline{\text{U2CTS}}$	RPINR9	U2CTSR<4:0>
SPI2 Data Input	SDI2	RPINR11	SDI2R<4:0>
SPI2 Clock Input	SCK2IN	RPINR11	SCK2INR<4:0>
SPI2 Slave Select Input	SS2IN	RPINR11	SS2INR<4:0>
CLC Input A	CLCINA	RPINR12	CLCINAR<4:0>
CLC Input B	CLCINB	RPINR12	CLCINBR<4:0>

9.8.5 OUTPUT MAPPING

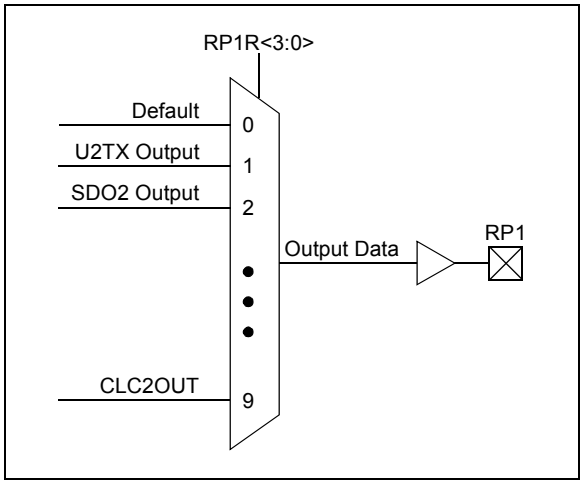
The RPORx registers are used to assign the peripheral output to the required remappable pin, RPn. Each RPORx register contains 4-bit fields corresponding to the remappable pins. A special value is defined for each peripheral output. This value should be written to the remappable pin bit field in the RPORx register to connect the peripheral output to the RPn pin. All possible (implemented) values for the peripheral's outputs are listed in Table 9-3.

Example 9-2 and Figure 9-3 illustrate the peripheral's output selection for the remappable pin.

EXAMPLE 9-2: UART2 TX OUTPUT ASSIGNMENT TO RP13/RB13 PIN

```
RPOR4bits.RP13R = 1;       // connect UART2 TX (= 1)
                           // to RP13 pin
```

FIGURE 9-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RP1



9.8.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MM0064GPL036 family devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

9.8.6.1 Control Register Lock

Under normal operation, the RPORx and RPINRx registers can be written, but they can also be locked to prevent accidental writes. This feature is controlled by the IOLOCK bit in the RPCON register. If the IOLOCK bit is set, then the contents of the RPORx and RPINRx registers cannot be changed.

To modify the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

TABLE 9-3: OUTPUT PIN SELECTION

Output Function Number	Function	Output Name
0	None (not connected)	—
1	U2TX	UART2 Transmit
2	$\overline{\text{U2RTS}}$	UART2 Request-to-Send
3	SDO2	SPI2 Data Output
4	SCK2OUT	SPI2 Clock Output
5	SS2OUT	SPI2 Slave Select Output
6	OCM2	SCCP2 Output Compare
7	OCM3	SCCP3 Output Compare
8	CLC1OUT	CLC1 Output
9	CLC2OUT	CLC2 Output

TABLE 9-5: PORTB REGISTER MAP

Virtual Address (BF80_#)	Register Name(2)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2700	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB<15:12>				—	—	—	—	—	—	—	—	ANSB<3:0>(1)				F00F
2710	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB<15:0>(1)																FFFF
2720	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB<15:0>(1)																0000
2730	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB<15:0>(1)																0000
2740	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB<15:0>(1)																0000
2750	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB<15:0>(1)																0000
2760	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB<15:0>(1)																0000
2770	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—	0000
2780	CNEN0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB<15:0>(1)																0000
2790	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATB<15:0>(1)																0000
27A0	CNEN1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1B<15:0>(1)																0000
27B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB<15:0>(1)																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits<11:10,6:5,3> are not implemented in 20-pin devices.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

NOTES:

REGISTER 15-4: RTCTIME/ALMTIME: RTCC/ALARM TIME REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	HRTEN<2:0>			HRONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SECTEN<3:0>				SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-28 **HRTEN<2:0>:** Binary Coded Decimal Value of Hours 10-Digit bits
Contains a value from 0 to 2.

bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours 1-Digit bits
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes 10-Digit bits
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes 1-Digit bits
Contains a value from 0 to 9.

bit 15-12 **SECTEN<3:0>:** Binary Coded Decimal Value of Seconds 10-Digit bits
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds 1-Digit bits
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 16-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	EXTSAM	—	SAMC<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source (TSRC) bit
1 = Clock derived from Fast RC (FRC) oscillator
0 = Clock derived from Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK)

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = ADC is still sampling after SAMP bit = 0
0 = ADC stops sampling when SAMP bit = 0

bit 13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
11111111 = 2 • TSRC • ADCS<7:0> = 510 • TSRC = TAD
•
•
•
00000001 = 2 • TSRC • ADCS<7:0> = 2 • TSRC = TAD
00000000 = 1 • TSRC = TAD
Where TSRC is a period of clock selected by the ADRC bit (AD1CON3<15>).

REGISTER 20-1: DAC1CON: CDAC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DACDAT<4:0>				
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON	—	—	—	—	—	—	DACOE
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **DACDAT<4:0>:** CDAC Voltage Reference Selection bits

11111 = (DACDAT<4:0> * VREF+/32) or (DACDAT<4:0> * AVDD/32) volts depending on the REFSEL<1:0> bits
•
•
•
00000 = 0.0 volts

bit 15 **ON:** Voltage Reference Enable bit

1 = Voltage reference is enabled
0 = Voltage reference is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** CDAC Voltage Reference Output Enable bit

1 = Voltage level is output on the CDAC1 pin
0 = Voltage level is disconnected from the CDAC1 pin

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** CDAC Voltage Reference Source Select bits

11 = Reference voltage is AVDD
10 = No reference is selected – output is AVSS
01 = Reference voltage is the VREF+ input pin voltage
00 = No reference is selected – output is AVSS

21.1 High/Low-Voltage Detect Registers

TABLE 21-1: HIGH/LOW-VOLTAGE DETECT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2310	HLVDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	VDIR	BGVST	IRVST	HLEVT	—	—	—	—	HLVDL<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

22.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Modes"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes power-saving features for the PIC32MM0064GPL036 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

22.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted, and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a `WAIT` instruction is executed.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- If WDT is enabled, the Run mode counter is not cleared upon entry to Sleep and the Sleep mode counter is reset upon entering Sleep.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC and Timer1).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The on-chip regulator enters Standby mode if the VREGS bit (PWRCON<0>) is set.
- A separate special low-power, low-voltage/ retention regulator is activated if the RETVR Configuration bit (FPOR<2>) is programmed to zero and the RETEN bit (PWRCON<1>) is set.

The processor will exit, or "wake-up", from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than, or equal to, the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

22.2 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than, or equal to, the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	SOSCSEL	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	IESO	SOSCEN	—	PLLSRC	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
- 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
- 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
- 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
- 1 = Crystal is used (RA4 and RB4 pins are controlled by SOSC)
- 0 = External clock is connected to the SOSCO pin (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
- 1 = OSC2/CLKO pin operates as normal I/O
- 0 = System clock is connected to the OSC2/CLKO pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit
- 1 = Two-Speed Start-up is enabled
- 0 = Two-Speed Start-up is disabled

bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Secondary Oscillator is enabled
- 0 = Secondary Oscillator is disabled

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit
- 1 = FRC oscillator is selected as the PLL reference input on a device Reset
- 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

FIGURE 26-5: TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS

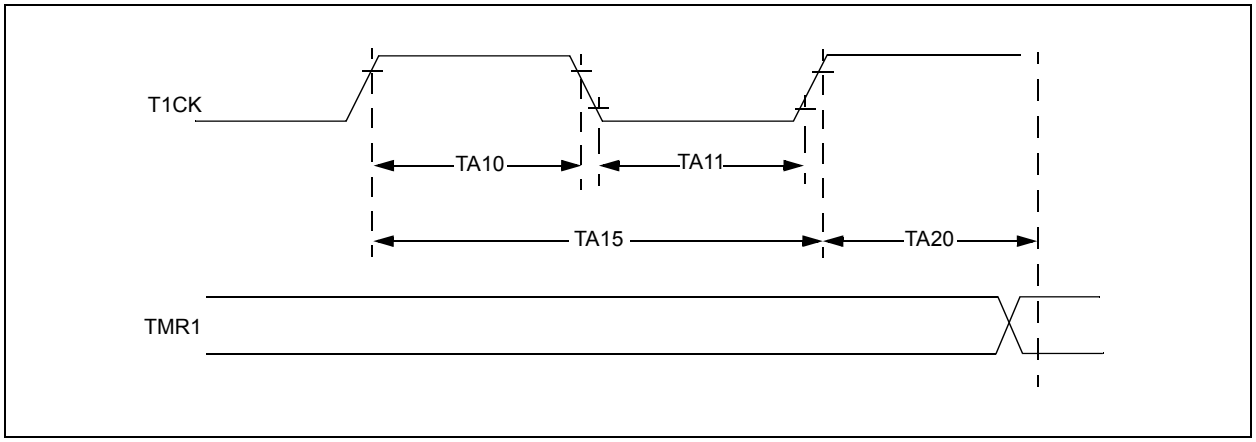


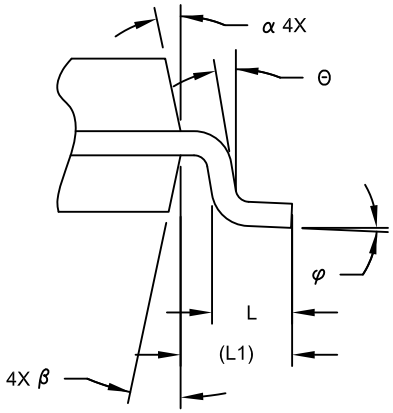
TABLE 26-23: MCCP/SCCP TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristics(1)**		**Min**	**Max**	**Units**	**Conditions**
TA10	TCKH	T1CK High Time	Synchronous	1	—	TPBCLK	Must also meet Parameter TA15
			Asynchronous	10	—	ns	
TA11	TCKL	T1CK Low Time	Synchronous	1	—	TPBCLK	Must also meet Parameter TA15
			Asynchronous	10	—	ns	
TA15	TCKP	T1CK Input Period	Synchronous	2	—	TPBCLK	
			Asynchronous	20	—	ns	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		—	3	TPBCLK	Synchronous mode

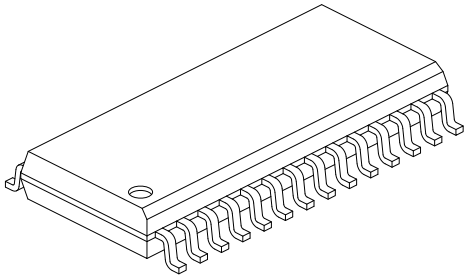
Note 1: These parameters are characterized but not tested in manufacturing.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

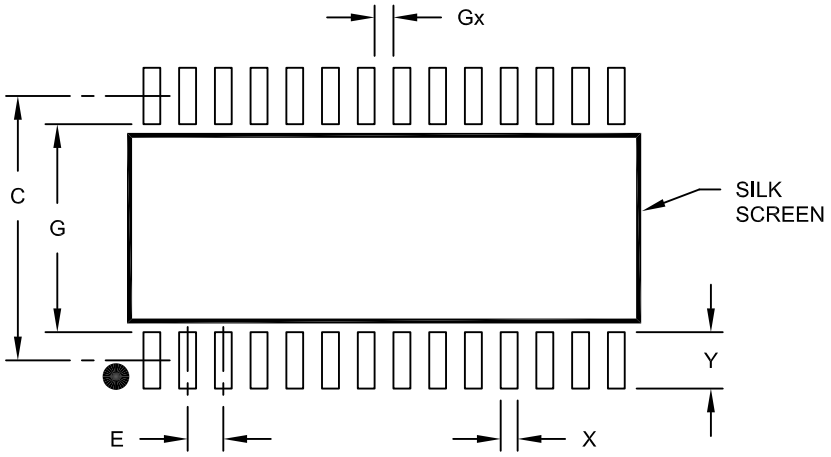
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

NOTES: