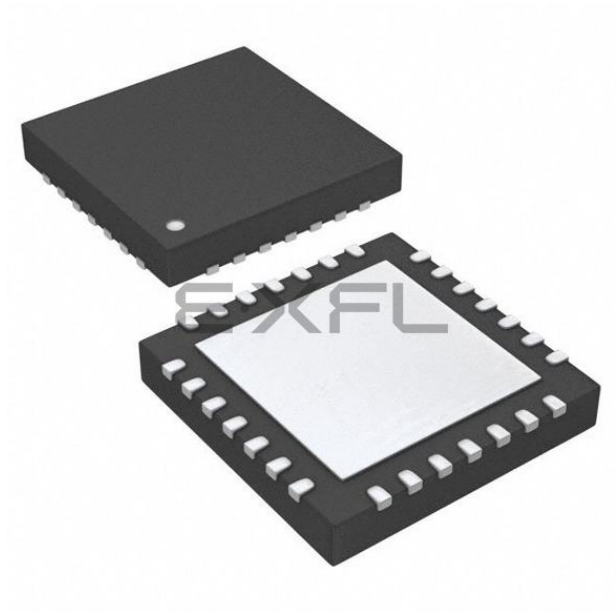

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028-e-ml

Analog Features

- Two Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit DAC with Output Pin
- Up to 14-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit, 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit, 300K samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0064GPL036 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (Channels)	Comparators	CRC	RTCC	JTAG	Packages
							UART(1)/LIN/J2602	16-Bit Timers	MCCP(3)	SCCP(4)	CLC	SPI(2)/I2S						
PIC32MM0016GPL020	20	16	4	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0032GPL020	20	32	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0064GPL020	20	64	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0016GPL028	28	16	4	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/SOIC/ QFN/UQFN
PIC32MM0032GPL028	28	32	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/ SOIC/ QFN/UQFN
PIC32MM0064GPL028	28	64	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SPDIP/SSOP/ SOIC/QFN/ UQFN
PIC32MM0016GPL036	36/40	16	4	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0032GPL036	36/40	32	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0064GPL036	36/40	64	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN

Note 1: UART1 has assigned pins. UART2 is remappable.

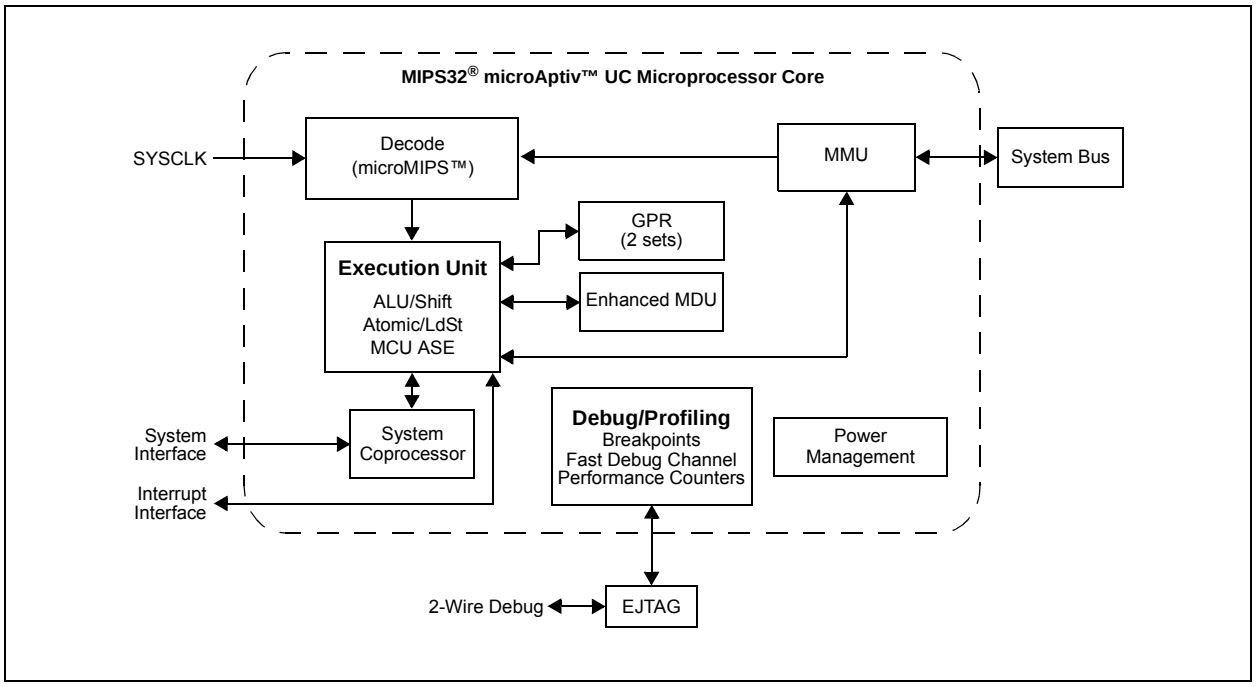
2: SPI1 has assigned pins. SPI2 is remappable.

3: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

NOTES:

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



REGISTER 5-2: NVMKEY: NVM PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** NVM Unlock Register bits
These bits are write-only and read as '0' on any read.

REGISTER 5-3: NVMADDR: NVM FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** NVM Flash Address bits

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<10:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<7:0> are ignored).
Double-Word Program	Address identifies the double-word (64-bit) to program (NVMADDR<1:0> bits are ignored).

6.0 RESETS

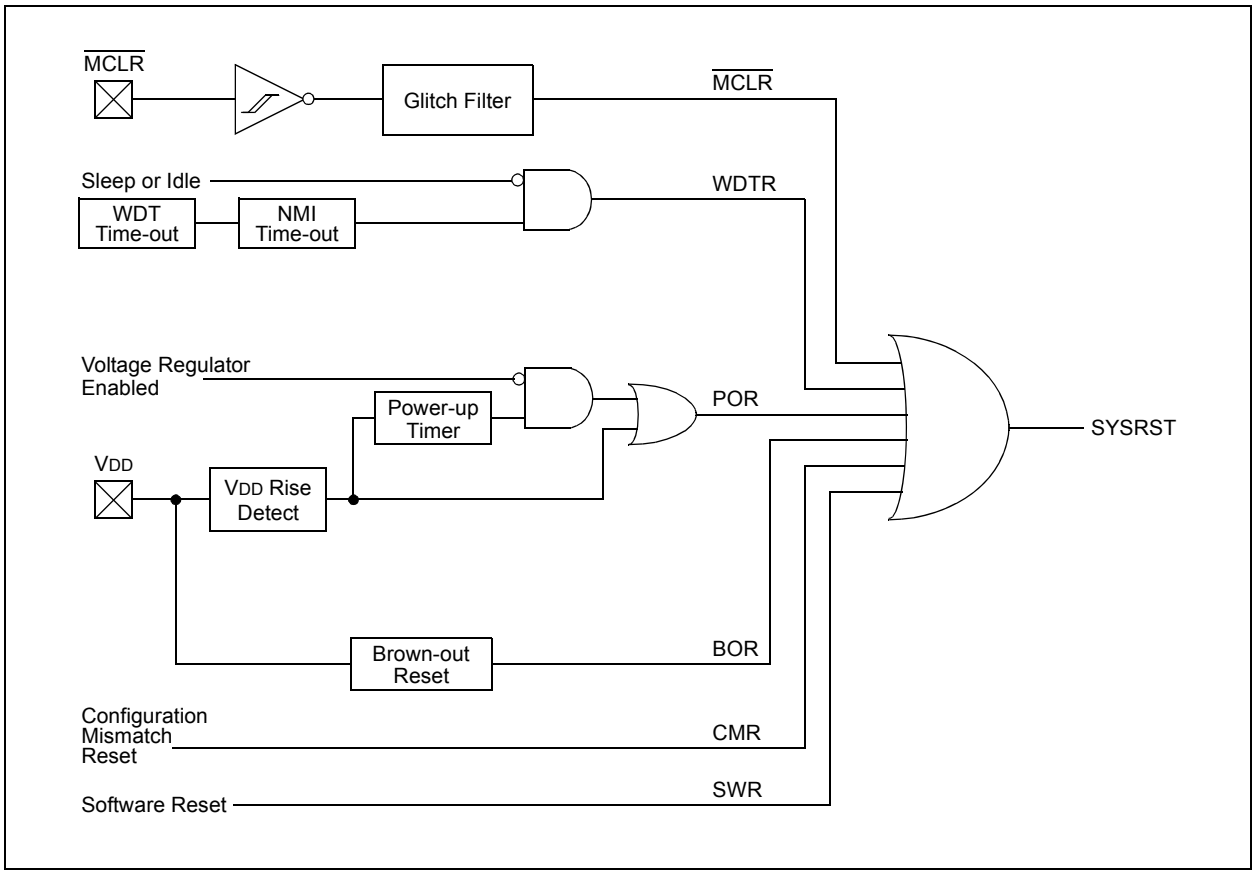
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset Pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	WDTR
23:16	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SWNMI	—	—	—	GNMI	—	CF	WDTS
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **WDTR:** Watchdog Timer Time-out in Run Mode Flag bit
1 = A Run mode WDT time-out has occurred and caused an NMI
0 = WDT time-out has not occurred
Setting this bit will cause a WDT NMI event and NMICNT<15:0> will begin counting.

bit 23 **SWNMI:** Software NMI Trigger bit
1 = An NMI has been generated
0 = An NMI was not generated

bit 22-20 **Unimplemented:** Read as '0'

bit 19 **GNMI:** Software General NMI Trigger bit
1 = A general NMI has been generated
0 = A general NMI was not generated

bit 18 **Unimplemented:** Read as '0'

bit 17 **CF:** Clock Fail Detect bit
1 = FSCM has detected clock failure and caused an NMI
0 = FSCM has not detected clock failure
Setting this bit will cause a CF NMI event, but will not cause a clock switch to the FRC.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from Sleep
0 = WDT time-out has not occurred during Sleep mode
Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI Reset counter.
FFFFh-0001h = Number of SYSCLK cycles before a device Reset occurs(2)
0000h = No delay between NMI assertion and device Reset event

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

2: If a Watchdog Timer NMI event (when not in Sleep mode) is cleared before this counter reaches '0', no device Reset is asserted. This NMI Reset counter is only applicable to the Watchdog Timer NMI event.

TABLE 7-3: INTERRUPT REGISTER MAP

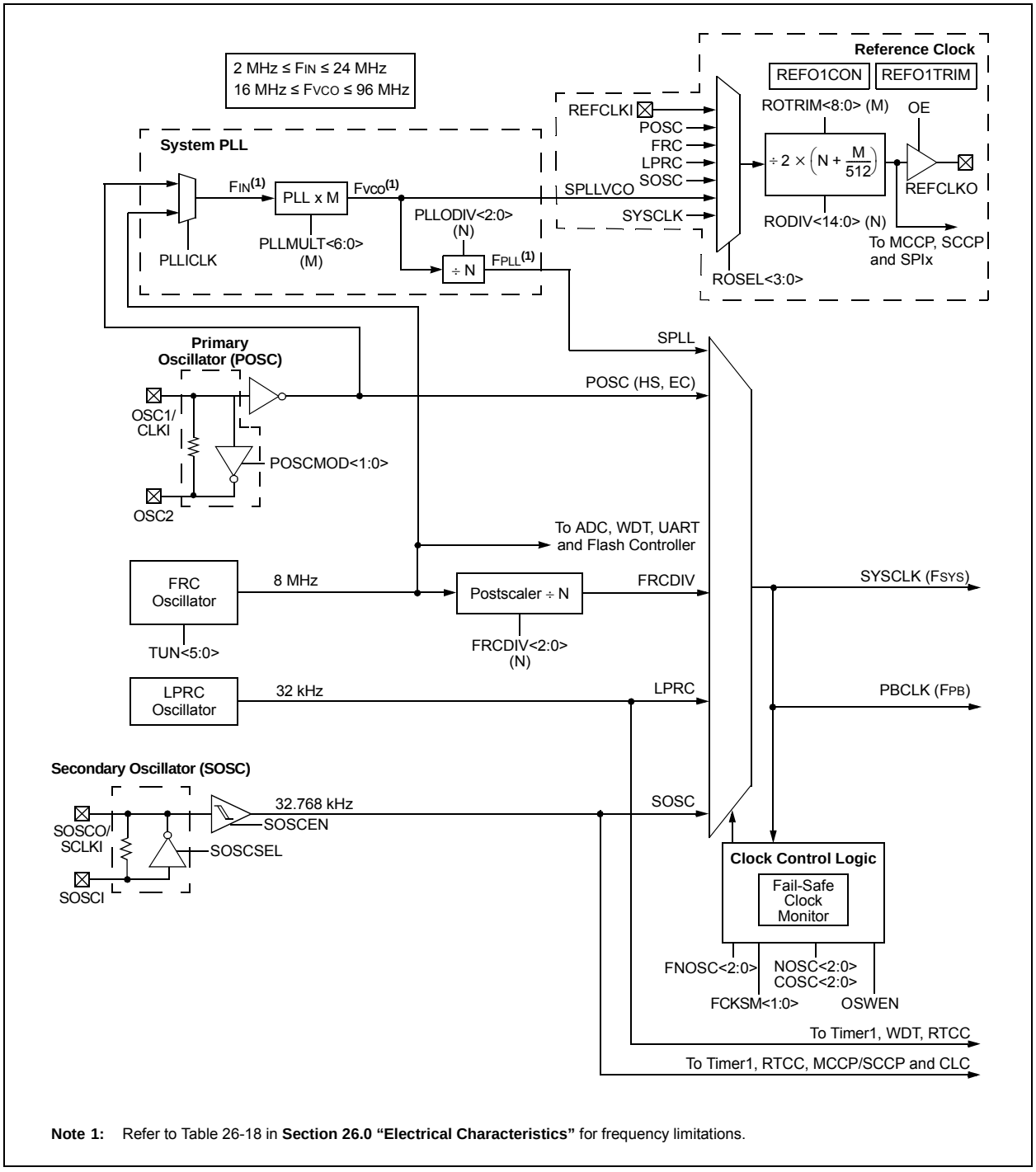
Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	INTCON	31:16	—	—	—	—	—	—	—	—	—	VS<6:0>							0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
F010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
F020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
F030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
F040	IFS0	31:16	CCP2IF	CCT1IF	CCP1IF	—	—	—	U1EIF	U1TXIF	U1RXIF	SPI1RXIF	SPI1TXIF	SPI1EIF	CLC2IF	CLC1IF	LVDIF	CRCIF	0000
		15:0	AD1IF	RTCCIF	CMP2IF	CMP1IF	T1IF	CNCIF(2)	CNBIF	CNAIF	INT4IF	INT3IF	INT2IF	INT1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
F050	IFS1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CPCIF	NVMIF	—	—	—	U2EIF	U2TXIF	U2RXIF	SPI2RXIF	SPI2TXIF	SPI2EIF	—	—	CCT3IF	CCP3IF	CCT2IF	0000
F0C0	IEC0	31:16	CCP2IE	CCT1IE	CCP1IE	—	—	—	U1EIE	U1TXIE	U1RXIE	SPI1RXIE	SPI1TXIE	SPI1EIE	CLC2IE	CLC1IE	LVDIE	CRCIE	0000
		15:0	AD1IE	RTCCIE	CMP2IE	CMP1IE	T1IE	CNCIE(2)	CNBIE	CNAIE	INT4IE	INT3IE	INT2IE	INT1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
F0D0	IEC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CPCIE	NVMIE	—	—	—	U2EIE	U2TXIE	U2RXIE	SPI2RXIE	SPI2TXIE	SPI2EIE	—	—	CCT3IE	CCP3IE	CCT2IE	0000
F140	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
F150	IPC1	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
F160	IPC2	31:16	—	—	—	T1IP<2:0>			T1IS<1:0>		—	—	—	CNCIP<2:0>(2)			CNCIS<1:0>(2)		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
F170	IPC3	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
F180	IPC4	31:16	—	—	—	CLC2IP<2:0>			CLC2IS<1:0>		—	—	—	CLC1IP<2:0>			CLC1IS<1:0>		0000
		15:0	—	—	—	LVDIP<2:0>			LVDIS<1:0>		—	—	—	CRCIP<2:0>			CRCIS<1:0>		0000
F190	IPC5	31:16	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
		15:0	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		0000
F1A0	IPC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	U1EIP<2:0>			U1EIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
F1B0	IPC7	31:16				CCP2IP<2:0>			CCP2IS<1:0>		—	—	—	CCT1IP<2:0>			CCT1IS<1:0>		0000
		15:0	—	—	—	CCP1IP<2:0>			CCP1IS<1:0>		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 20-pin devices.

FIGURE 8-1: PIC32MM0064GPL036 FAMILY OSCILLATOR DIAGRAM



Note 1: Refer to Table 26-18 in **Section 26.0 "Electrical Characteristics"** for frequency limitations.

REGISTER 8-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 8-1 for details). A value of '0' selects no divider.

bit 15 **ON:** Reference Oscillator Output Enable bit(1)
1 = Reference oscillator module is enabled
0 = Reference oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on the REFCLKO pin
0 = Reference clock is not driven out on the REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference oscillator module output continues to run in Sleep
0 = Reference oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

TABLE 9-7: PERIPHERAL PIN SELECT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2480	RPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	IOLOCK	—	—	—	—	—	—	—	—	—	—	—	0000
24A0	RPINR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0												INT4R<4:0>					0000
24B0	RPINR2	31:16	—	—	—	ICM2R<4:0>					—	—	—	ICM1R<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
24C0	RPINR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ICM3R<4:0>					0000
24E0	RPINR5	31:16	—	—	—	OCFBR<4:0>					—	—	—	OCFAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
24F0	RPINR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0				TCKIBR<4:0>					—	—	—	TCKIAR<4:0>					0000
2520	RPINR9	31:16	—	—	—	U2CTSR<4:0>					—	—	—	U2RXR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2540	RPINR11	31:16	—	—	—	—	—	—	—	—	—	—	—	SS2INR<4:0>					0000
		15:0	—	—	—	SCK2INR<4:0>					—	—	—	SDI2R<4:0>					0000
2550	RPINR12	31:16	—	—	—	CLCINBR<4:0>					—	—	—	CLCINAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2590	RPOR0	31:16					RP4R<3:0>				—	—	—	—	RP3R<3:0>				0000
		15:0	—	—	—	—	RP2R<3:0>				—	—	—	—	RP1R<3:0>				0000
25A0	RPOR1	31:16	—	—	—	—	RP8R<3:0>				—	—	—	—	RP7R<3:0>				0000
		15:0	—	—	—	—	RP6R<3:0>				—	—	—	—	RP5R<3:0>				0000
25B0	RPOR2	31:16	—	—	—	—	RP12R<3:0>				—	—	—	—	RP11R<3:0>				0000
		15:0	—	—	—	—	RP10R<3:0>				—	—	—	—	RP9R<3:0>				0000
25C0	RPOR3	31:16	—	—	—	—	RP16R<3:0>				—	—	—	—	RP15R<3:0>				0000
		15:0	—	—	—	—	RP14R<3:0>				—	—	—	—	RP13R<3:0>				0000
25D0	RPOR4	31:16	—	—	—	—	RP20R<3:0>				—	—	—	—	RP19R<3:0>				0000
		15:0	—	—	—	—	RP18R<3:0>				—	—	—	—	RP17R<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 14-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to the empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

REGISTER 15-1: RTCCON1: RTCC CONTROL 1 REGISTER (CONTINUED)

bit 11 **WRLOCK:** RTCC Registers Write Lock bit(2)
1 = Registers associated with accurate timekeeping are locked
0 = Registers associated with accurate timekeeping may be written to by user

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin
0 = RTCC clock output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Signal Output Selection bits
111 = Reserved
• • •
011 = Reserved
010 = RTCC input clock source
001 = Seconds clock
000 = Alarm event

bit 3-0 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: To clear this bit, an unlock sequence is required. Refer to **Section 23.4 "System Registers Write Protection"** for details.

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 20 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

bit 19 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 3
0 = The Data Source 2 signal is disabled for Gate 3

bit 18 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 3
0 = The Data Source 2 inverted signal is disabled for Gate 3

bit 17 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 3
0 = The Data Source 1 signal is disabled for Gate 3

bit 16 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 3
0 = The Data Source 1 inverted signal is disabled for Gate 3

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 2
0 = The Data Source 4 signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 2
0 = The Data Source 3 signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 2
0 = The Data Source 2 signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 2
0 = The Data Source 1 signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 1
0 = The Data Source 4 signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 1
0 = The Data Source 3 signal is disabled for Gate 1

22.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Modes"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes power-saving features for the PIC32MM0064GPL036 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

22.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted, and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a `WAIT` instruction is executed.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- If WDT is enabled, the Run mode counter is not cleared upon entry to Sleep and the Sleep mode counter is reset upon entering Sleep.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC and Timer1).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The on-chip regulator enters Standby mode if the VREGS bit (PWRCON<0>) is set.
- A separate special low-power, low-voltage/ retention regulator is activated if the RETVR Configuration bit (FPOR<2>) is programmed to zero and the RETEN bit (PWRCON<1>) is set.

The processor will exit, or "wake-up", from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than, or equal to, the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

22.2 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than, or equal to, the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

26.2 AC Characteristics and Timing Parameters

FIGURE 26-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

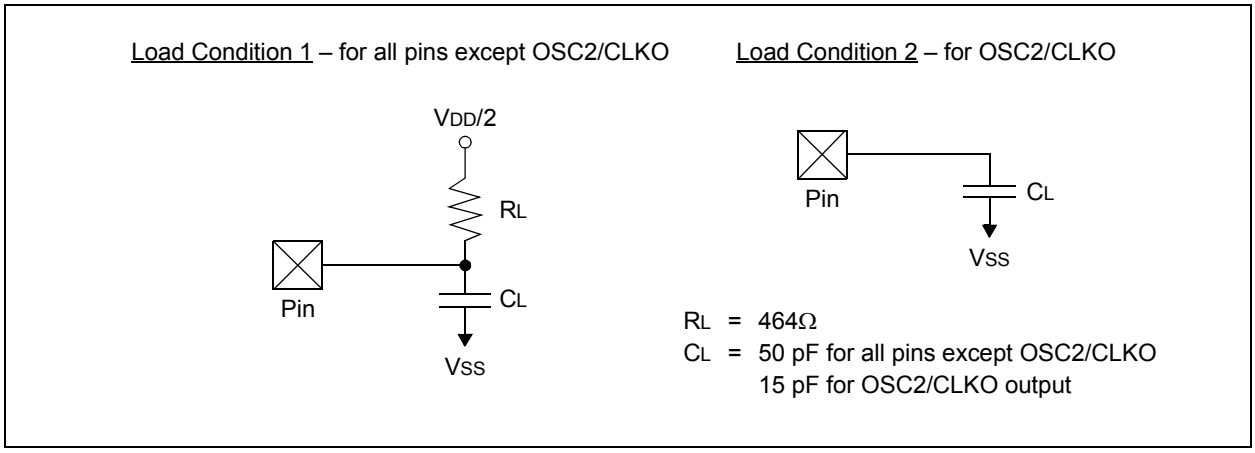


TABLE 26-16: CAPACITIVE LOADING CONDITIONS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
DO50	COSCO	OSC2/CLKO Pin	—	15	pF	In XT and HS modes when external clock is used to drive OSC1/CLKI
DO56	CIO	All I/O Pins and OSC2	—	50	pF	EC mode

FIGURE 26-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

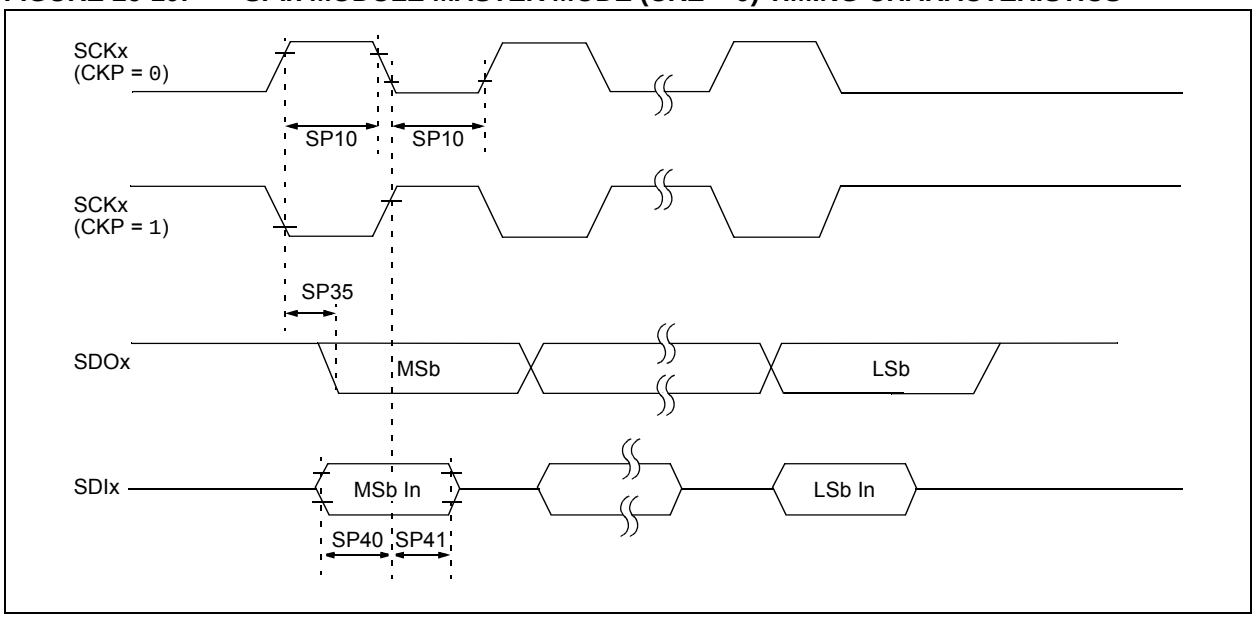
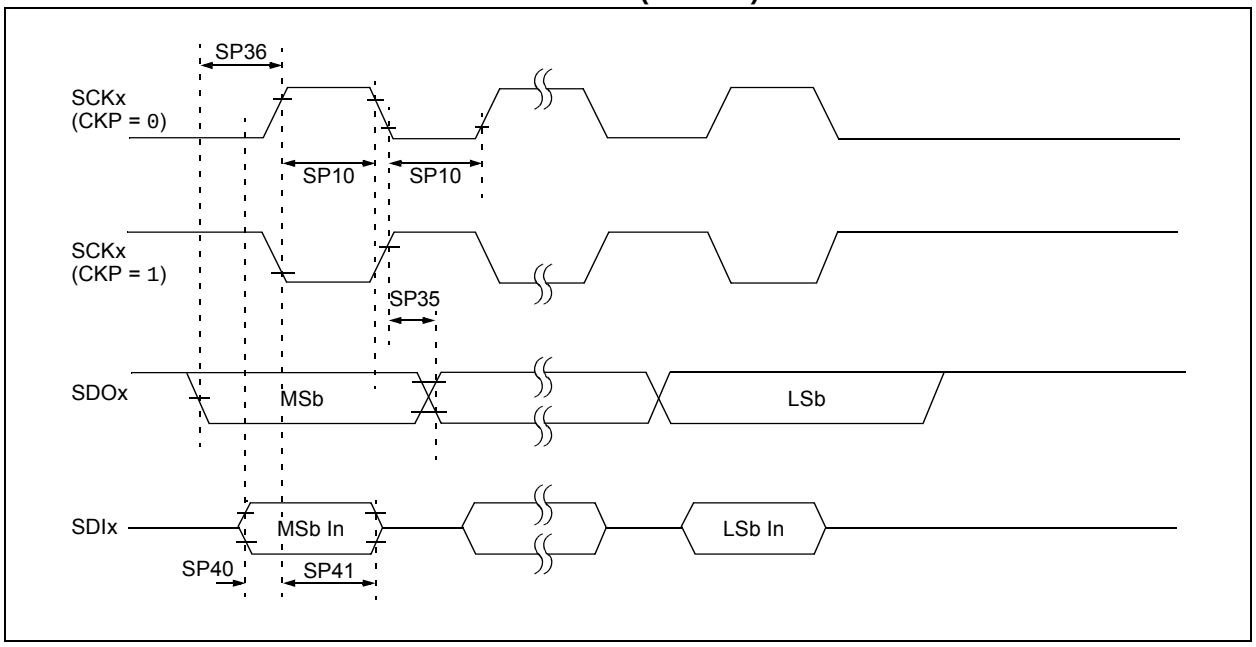
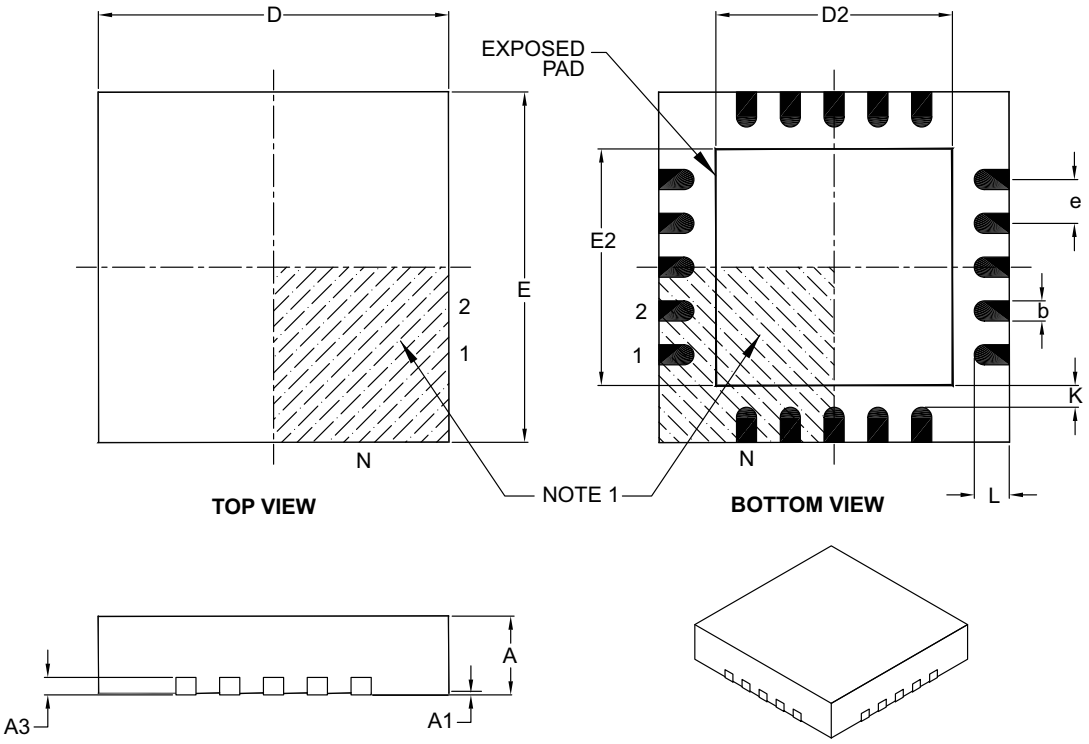


FIGURE 26-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

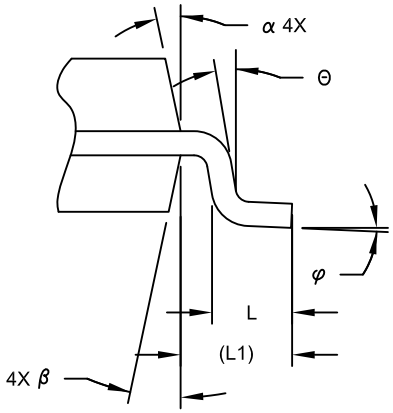
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

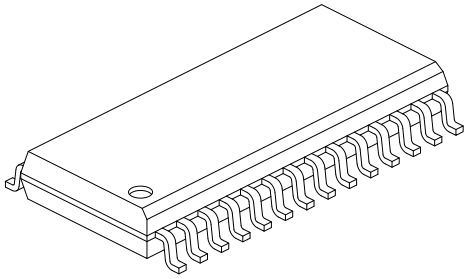
Microchip Technology Drawing C04-126B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

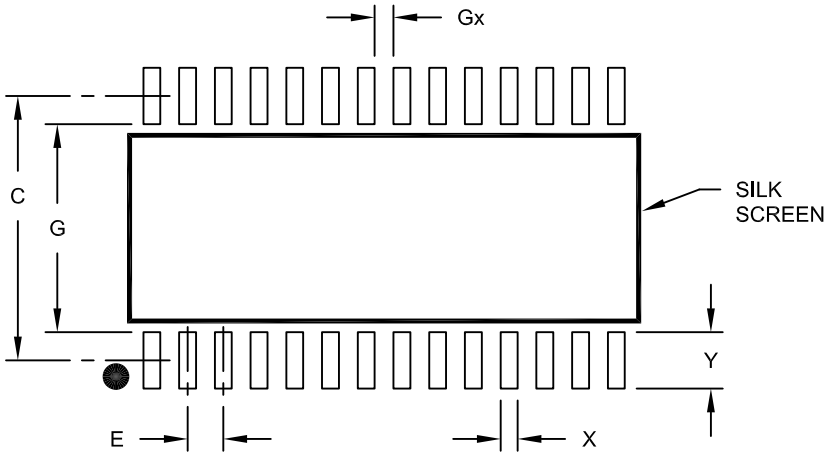
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

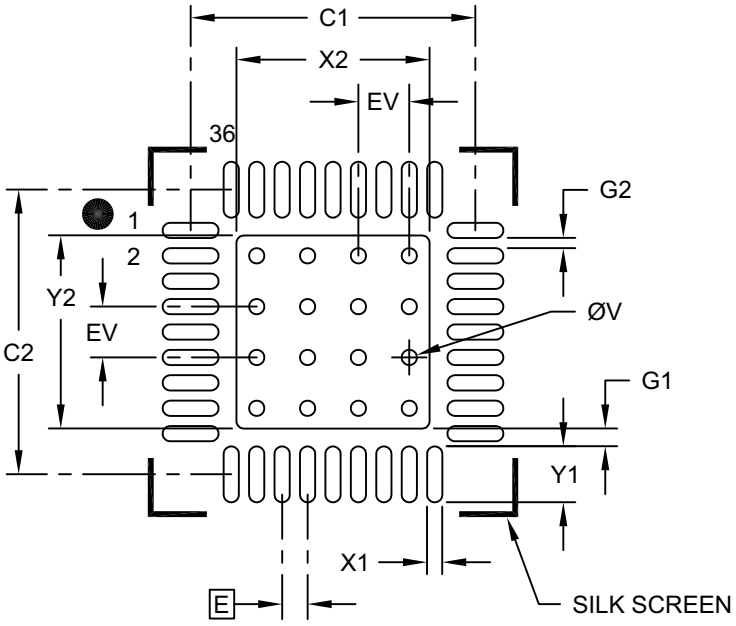
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x0.9 mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.60	
Contact Pad Spacing	C2		5.60	
Contact Pad Width (X36)	X1			0.30
Contact Pad Length (X36)	Y1			1.10
Contact Pad to Center Pad (X36)	G1	0.35		
Space Between Contact Pads (X32)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2272B-M2