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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I ² S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028-e-so

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NOTES:

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM. This data sheet contains device-specific information for the PIC32MM0064GPL036 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0064GPL036 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0064GPL036 FAMILY BLOCK DIAGRAM



	Pin Number									
Pin Name	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN	Pin Type	Buffer Type	Description	
PGEC1	2	5	2	5	36	39	Ι	ST	ICSP Port 1 programming clock input	
PGEC2	19	2	19	22	25	28	I	ST	ICSP Port 2 programming clock input	
PGEC3	7	10	12	15	16	16	Ι	ST	ICSP Port 3 programming clock input	
PGED1	1	4	1	4	35	38	I/O	ST/DIG	ICSP Port 1 programming data	
PGED2	20	3	18	21	24	27	I/O	ST/DIG	ICSP Port 2 programming data	
PGED3	6	9	11	14	15	15	I/O	ST/DIG	ICSP Port 3 programming data	
PWRLCLK	7	10	9	12	10	10	Ι	ST	Real-Time Clock 50/60 Hz clock input	
RA0	19	2	27	2	33	36	I/O	ST/DIG	PORTA digital I/O	
RA1	20	3	28	3	34	37	I/O	ST/DIG	PORTA digital I/O	
RA2	4	7	6	9	7	7	I/O	ST/DIG	PORTA digital I/O	
RA3	5	8	7	10	8	8	I/O	ST/DIG	PORTA digital I/O	
RA4	7	10	9	12	10	10	I/O	ST/DIG	PORTA digital I/O	
RA9	_	_	_	—	11	11	I/O	ST/DIG	PORTA digital I/O	
RB0	1	4	1	4	35	38	I/O	ST/DIG	PORTB digital I/O	
RB1	2	5	2	5	36	39	I/O	ST/DIG	PORTB digital I/O	
RB2	3	6	3	6	1	1	I/O	ST/DIG	PORTB digital I/O	
RB3	_	_	4	7	2	2	I/O	ST/DIG	PORTB digital I/O	
RB4	6	9	8	11	9	9	I/O	ST/DIG	PORTB digital I/O	
RB5	_	_	11	14	15	15	I/O	ST/DIG	PORTB digital I/O	
RB6	_	_	12	15	16	16	I/O	ST/DIG	PORTB digital I/O	
RB7	8	11	13	16	17	17	I/O	ST/DIG	PORTB digital I/O	
RB8	9	12	14	17	18	18	I/O	ST/DIG	PORTB digital I/O	
RB9	10	13	15	18	19	20	I/O	ST/DIG	PORTB digital I/O	
RB10	_	_	18	21	24	27	I/O	ST/DIG	PORTB digital I/O	
RB11	_	_	19	22	25	28	I/O	ST/DIG	PORTB digital I/O	
RB12	12	15	20	23	26	29	I/O	ST/DIG	PORTB digital I/O	
RB13	13	16	21	24	27	30	I/O	ST/DIG	PORTB digital I/O	
RB14	14	17	22	25	28	31	I/O	ST/DIG	PORTB digital I/O	
RB15	15	18	23	26	29	32	I/O	ST/DIG	PORTB digital I/O	
RC0				—	3	3	I/O	ST/DIG	PORTC digital I/O	
RC1		—		—	4	4	I/O	ST/DIG	PORTC digital I/O	
RC2		—		—	5	5	I/O	ST/DIG	PORTC digital I/O	
RC3				—	14	14	I/O	ST/DIG	PORTC digital I/O	
RC8		—		—	20	21	I/O	ST/DIG	PORTC digital I/O	
RC9	_	_	16	19	21	22	I/O	ST/DIG	PORTC digital I/O	
REFCLKI	10	13	15	18	19	20	Ι	ST	Reference clock input	
REFCLKO	15	18	23	26	29	32	0	DIG	Reference clock output	

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Legend: ST = Schmitt Trigger input buffer

DIG = Digital input/output

ANA = Analog level input/output

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0064GPL036 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVSS pins, even if the ADC module is not used (see Section 2.2 "Decoupling Capacitors")
- MCLR pin (see Section 2.3 "Master Clear (MCLR) Pin")
- VCAP pin (see Section 2.4 "Capacitor on Internal Voltage Regulator (VCAP)")
- PGECx/PGEDx pins, used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see Section 2.7 "External Oscillator Pins")

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A value of $0.1 \ \mu F$ (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31:24	NVMDATAx<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:10				NVMDA	TAx<23:16>				
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	NVMDATAx<15:8>								
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	NVMDATAx<7:0>								

REGISTER 5-4: NVMDATAX: NVM FLASH DATA x REGISTER (x = 0-1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMDATAx<31:0>: NVM Flash Data x bits

Double-Word Program: Writes NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the least significant instruction word.

REGISTER 5-5: NVMSRCADDR: NVM SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24	NVMSRCADDR<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:10				NVMSRCA	DDR<23:16>	>			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	NVMSRCADDR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	NVMSRCADDR<7:0>								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMSRCADDR<31:0>: NVM Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-1, HS	R/W-1, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
31:24	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—		—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	U-0
15:8	_	_		—	—	_	CMR	_
7.0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
7:0	EXTR	SWR		WDTO	SLEEP	IDLE ⁽²⁾	BOR	POR

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

Legend:	HS = Hardware Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31	PORIO: VDD POR Flag bit
	Set by hardware at detection of a VDD POR event. 1 = A Power-on Reset has occurred due to VDD voltage 0 = A Power-on Reset has not occurred due to VDD voltage
bit 30	PORCORE: Core Voltage POR Flag bit
	Set by hardware at detection of a core POR event. 1 = A Power-on Reset has occurred due to core voltage
hit 20.20	U = A Power-on Reset has not occurred due to core voltage
DIL 29-28	
DIT 27	BCFGERR: Primary Configuration Registers Error Flag bit
	 a error occurred during a read of the Primary Configuration registers 0 = No error occurred during a read of the Primary Configuration registers
bit 26	BCFGFAIL: Primary/Secondary Configuration Registers Error Flag bit
	1 = An error occurred during a read of the Primary and Alternate Configuration registers 0 = No error occurred during a read of the Primary and Alternate Configuration registers
bit 25-10	Unimplemented: Read as '0'
bit 9	CMR: Configuration Mismatch Reset Flag bit
	1 = A Configuration Mismatch Reset has occurred
	0 = A Configuration Mismatch Reset has not occurred
bit 8	Unimplemented: Read as '0'
bit 7	EXTR: External Reset (MCLR) Pin Flag bit
	1 = Master Clear (pin) Reset has occurred0 = Master Clear (pin) Reset has not occurred
bit 6	SWR: Software Reset Flag bit
	1 = Software Reset was executed0 = Software Reset was not executed
bit 5	Unimplemented: Read as '0'
bit 4	WDTO: Watchdog Timer Time-out Flag bit
	1 = WDT time-out has occurred
	0 = WDT time-out has not occurred
Note 1:	User software must clear bits in this register to view the next detection.

2: The IDLE bit will also be set when the device wakes from Sleep mode.

7.2 Interrupts

The PIC32MM0064GPL036 family uses fixed offset for vector spacing. For details, refer to **Section 8. "Interrupts"** (DS60001108) in the *"PIC32 Family Reference Manual"*. Table 7-2 provides the interrupt related vectors and bits information.

Interrunt Source		Vector		Persisten			
interrupt oource	MPLAB [®] XC32 vector name	Number	Flag	Enable	Priority	Subpriority	Interrupt
Core Timer	_CORE_TIMER_VECTOR	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software 0	_CORE_SOFTWARE_0_VECTOR	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software 1	_CORE_SOFTWARE_1_VECTOR	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External 0	_external_0_vector	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
External 1	_EXTERNAL_1_VECTOR	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
External 2	_EXTERNAL_2_VECTOR	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	No
External 3	_external_3_vector	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	No
External 4	_EXTERNAL_4_VECTOR	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
PORTA Change Notification	_CHANGE_NOTICE_A_VECTOR	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
PORTB Change Notification	_CHANGE_NOTICE_B_VECTOR	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
PORTC Change Notification	_CHANGE_NOTICE_C_VECTOR	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	No
Timer1	_TIMER_1_VECTOR	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	No
Comparator 1	_COMPARATOR_1_VECTOR	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
Comparator 2	_COMPARATOR_2_VECTOR	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Real-Time Clock Alarm	_RTCC_VECTOR	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
ADC Conversion	_ADC_VECTOR	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	No
CRC	_CRC_VECTOR	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
High/Low-Voltage Detect	_HLVD_VECTOR	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	Yes
Logic Cell 1	_CLC1_VECTOR	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Logic Cell 2	_CLC2_VECTOR	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
SPI1 Error	_SPI1_ERR_VECTOR	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
SPI1 Transmission	_SPI1_TX_VECTOR	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes
SPI1 Reception	_SPI1_RX_VECTOR	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	Yes

9.8.4 INPUT MAPPING

The RPINRx registers are used to assign the peripheral input to the required remappable pin, RPn (refer to the peripheral inputs and the corresponding RPINRx registers listed in Table 9-2). Each RPINRx register contains sets of 5-bit fields. Programming these bits with the remappable pin number will connect the peripheral to this RPn pin. Example 9-1 and Figure 9-2 illustrate the remappable pin selection for the U2RX input.

EXAMPLE 9-1: UART2 RX INPUT ASSIGNMENT TO RP9/RB14 PIN

RPINR9bits.U2RXR	=	9;	11	connect UART2 RX
			//	input to RP9 pin

FIGURE 9-2: REMA

REMAPPABLE INPUT EXAMPLE FOR U2RX



TABLE 9-2: INPUT PIN SELECTION

Input Name	Function Name	Register	Function Bits
External Interrupt 4	INT4	RPINR1	INT4R<4:0>
MCCP1 Input Capture	ICM1	RPINR2	ICM1R<4:0>
SCCP2 Input Capture	ICM2	RPINR2	ICM2R<4:0>
SCCP3 Input Capture	ICM3	RPINR3	ICM3R<4:0>
Output Compare Fault A	OCFA	RPINR5	OCFAR<4:0>
Output Compare Fault B	OCFB	RPINR5	OCFBR<4:0>
CCP Clock Input A	TCKIA	RPINR6	TCKIAR<4:0>
CCP Clock Input B	TCKIB	RPINR6	TCKIBR<4:0>
UART2 Receive	U2RX	RPINR9	U2RXR<4:0>
UART2 Clear-to-Send	U2CTS	RPINR9	U2CTSR<4:0>
SPI2 Data Input	SDI2	RPINR11	SDI2R<4:0>
SPI2 Clock Input	SCK2IN	RPINR11	SCK2INR<4:0>
SPI2 Slave Select Input	SS2IN	RPINR11	SS2INR<4:0>
CLC Input A	CLCINA	RPINR12	CLCINAR<4:0>
CLC Input B	CLCINB	RPINR12	CLCINBR<4:0>

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24 FRMEN		FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
00.40	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
23:16	MCLKSEL ⁽¹⁾	—		—	—	—	SPIFE	ENHBUF ⁽¹⁾
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON	—	SIDL	DISSDO ⁽⁴⁾	MODE32	MODE16	SMP	CKE ⁽²⁾
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	SSEN	CKP ⁽³⁾	MSTEN	DISSDI ⁽⁴⁾	STXISE	L<1:0>	SRXIS	EL<1:0>

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 FRMEN: Framed SPI Support bit

- 1 = Framed SPI support is enabled (\overline{SSx} pin is used as the FSYNC1 input/output)
- 0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on <u>SSx</u> Pin bit (Framed SPI mode only)
 - 1 = Frame sync pulse input (Slave mode)
 - 0 = Frame sync pulse output (Master mode)
- bit 29 FRMPOL: Frame Sync Polarity bit (Framed SPI mode only)
 - 1 = Frame pulse is active-high
 - 0 = Frame pulse is active-low
- bit 28 **MSSEN:** Master Mode Slave Select Enable bit
 - 1 = Slave select SPI support is enabled; the SSx pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
 - 0 = Slave select SPI support is disabled
- bit 27 FRMSYPW: Frame Sync Pulse-Width bit
 - 1 = Frame sync pulse is one character wide
 - 0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits

Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.

- 111 = Reserved
- 110 = Reserved
- 101 = Generates a frame sync pulse on every 32 data characters
- 100 = Generates a frame sync pulse on every 16 data characters
- 011 = Generates a frame sync pulse on every 8 data characters
- 010 = Generates a frame sync pulse on every 4 data characters
- 001 = Generates a frame sync pulse on every 2 data characters
- 000 = Generates a frame sync pulse on every data character
- **Note 1:** These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.
 - 2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - **3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
 - 4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see Section 9.8 "Peripheral Pin Select (PPS)" for more information).

REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER (CONTINUED)

- bit 3 SPITBE: SPIx Transmit Buffer Empty Status bit
 - 1 = Transmit buffer, SPIxTXB, is empty

0 = Transmit buffer, SPIxTXB, is not empty Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 Unimplemented: Read as '0'

bit 1 SPITBF: SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPIxTXB is full

0 = Transmit buffer is not full

Standard Buffer mode:

Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:

Set when the CPU Write Pointer (CWPTR) + 1 = SPI Read Pointer (SRPTR); cleared otherwise.

bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive buffer, SPIxRXB, is full

0 = Receive buffer, SPIxRXB, is not full

Standard Buffer mode:

Automatically set in hardware when the SPIx module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	4 — HRTEN<2:0>		HRONE<3:0>					
00.40	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	—	MINTEN<2:0>			MINONE<3:0>			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	SECTEN<3:0>		SECONE<3:0>					
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	—	_		—		_	

REGISTER 15-4: RTCTIME/ALMTIME: RTCC/ALARM TIME REGISTERS

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 Unimplemented: Read as '0'

- bit 30-28 **HRTEN<2:0>:** Binary Coded Decimal Value of Hours 10-Digit bits Contains a value from 0 to 2.
- bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours 1-Digit bits Contains a value from 0 to 9.
- bit 23 Unimplemented: Read as '0'
- bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes 10-Digit bits Contains a value from 0 to 5.
- bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes 1-Digit bits Contains a value from 0 to 9.
- bit 15-12 **SECTEN<3:0>:** Binary Coded Decimal Value of Seconds 10-Digit bits Contains a value from 0 to 5.
- bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds 1-Digit bits Contains a value from 0 to 9.
- bit 7-0 Unimplemented: Read as '0'

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 20	G3D3N: Gate 3 Data Source 3 Negated Enable bit
	1 = The Data Source 3 inverted signal is enabled for Gate 3
	0 = The Data Source 3 inverted signal is disabled for Gate 3
bit 19	G3D2T: Gate 3 Data Source 2 True Enable bit
	 1 = The Data Source 2 signal is enabled for Gate 3 0 = The Data Source 2 signal is disabled for Gate 3
bit 18	G3D2N: Gate 3 Data Source 2 Negated Enable bit
	1 = The Data Source 2 inverted signal is enabled for Gate 30 = The Data Source 2 inverted signal is disabled for Gate 3
bit 17	G3D1T: Gate 3 Data Source 1 True Enable bit
	1 = The Data Source 1 signal is enabled for Gate 30 = The Data Source 1 signal is disabled for Gate 3
bit 16	G3D1N: Gate 3 Data Source 1 Negated Enable bit
	1 = The Data Source 1 inverted signal is enabled for Gate 3 0 = The Data Source 1 inverted signal is disabled for Gate 3
bit 15	G2D4T: Gate 2 Data Source 4 True Enable bit
	 1 = The Data Source 4 signal is enabled for Gate 2 0 = The Data Source 4 signal is disabled for Gate 2
bit 14	G2D4N: Gate 2 Data Source 4 Negated Enable bit
	1 = The Data Source 4 inverted signal is enabled for Gate 2
	0 = The Data Source 4 inverted signal is disabled for Gate 2
bit 13	G2D3T: Gate 2 Data Source 3 True Enable bit
	 1 = The Data Source 3 signal is enabled for Gate 2 0 = The Data Source 3 signal is disabled for Gate 2
bit 12	G2D3N: Gate 2 Data Source 3 Negated Enable bit
	1 = The Data Source 3 inverted signal is enabled for Gate 20 = The Data Source 3 inverted signal is disabled for Gate 2
bit 11	G2D2T: Gate 2 Data Source 2 True Enable bit
	1 = The Data Source 2 signal is enabled for Gate 20 = The Data Source 2 signal is disabled for Gate 2
bit 10	G2D2N: Gate 2 Data Source 2 Negated Enable bit
	1 = The Data Source 2 inverted signal is enabled for Gate 20 = The Data Source 2 inverted signal is disabled for Gate 2
bit 9	G2D1T: Gate 2 Data Source 1 True Enable bit
	1 = The Data Source 1 signal is enabled for Gate 20 = The Data Source 1 signal is disabled for Gate 2
bit 8	G2D1N: Gate 2 Data Source 1 Negated Enable bit
	1 = The Data Source 1 inverted signal is enabled for Gate 2
hit 7	0 = The Data Source T Inverted signal is disabled for Gate 2
	1 = The Data Source 4 signal is enabled for Gate 1
	0 = The Data Source 4 signal is disabled for Gate 1
bit 6	G1D4N: Gate 1 Data Source 4 Negated Enable bit
	 1 = The Data Source 4 inverted signal is enabled for Gate 1 0 = The Data Source 4 inverted signal is disabled for Gate 1
bit 5	G1D3T: Gate 1 Data Source 3 True Enable bit
	1 = The Data Source 3 signal is enabled for Gate 10 = The Data Source 3 signal is disabled for Gate 1

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 4	G1D3N: Gate 1 Data Source 3 Negated Enable bit 1 = The Data Source 3 inverted signal is enabled for Gate 1 0 = The Data Source 3 inverted signal is disabled for Gate 1
bit 3	G1D2T: Gate 1 Data Source 2 True Enable bit
	 1 = The Data Source 2 signal is enabled for Gate 1 0 = The Data Source 2 signal is disabled for Gate 1
bit 2	G1D2N: Gate 1 Data Source 2 Negated Enable bit
	 1 = The Data Source 2 inverted signal is enabled for Gate 1 0 = The Data Source 2 inverted signal is disabled for Gate 1
bit 1	G1D1T: Gate 1 Data Source 1 True Enable bit
	 1 = The Data Source 1 signal is enabled for Gate 1 0 = The Data Source 1 signal is disabled for Gate 1
bit 0	G1D1N: Gate 1 Data Source 1 Negated Enable bit
	 1 = The Data Source 1 inverted signal is enabled for Gate 1 0 = The Data Source 1 inverted signal is disabled for Gate 1

REGISTER 19-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 AND 2) (CONTINUED)

bit 7-6 EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits

11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)10 = Trigger/event/interrupt is generated on transition of the comparator output:

If CPOL = 0 (non-inverted polarity):

High-to-low transition only. If CPOL = 1 (inverted polarity):

Low-to-high transition only.

01 = Trigger/event/interrupt is generated on transition of the comparator output:

If CPOL = 0 (non-inverted polarity):

Low-to-high transition only.

If CPOL = 1 (inverted polarity):

High-to-low transition only.

00 = Trigger/event/interrupt generation is disabled

- bit 5 **Unimplemented:** Read as '0'
- bit 4 CREF: Comparator Reference Select bit (non-inverting input)
 - 1 = Non-inverting input connects to the internal reference defined by the CVREFSEL bit in the CMSTAT register 0 = Non-inverting input connects to the CXINA pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Channel Select bits
 - 11 = Inverting input of the comparator connects to the band gap reference voltage
 - 10 = Inverting input of the comparator connects to the CxIND pin
 - 01 = Inverting input of the comparator connects to the CxINC pin
 - 00 = Inverting input of the comparator connects to the CxINB pin

21.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 21-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 21-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



25.0 INSTRUCTION SET

The PIC32MM0064GPL036 family instruction set complies with the MIPS[®] Release 3 instruction set architecture. Only microMIPS32[™] instructions are supported. The PIC32MM0064GPL036 family does not have the following features:

- · Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note:	Refer to the "M	IPS [®] Archite	ecture for
	Programmers	Volume II-	B: The
	microMIPS32™	Instruction	Set" at
	www.imgtec.com f	or more infori	mation.

TABLE 26-4: OPERATING CURRENT (IDD)⁽²⁾

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Parameter No.	Typical ⁽¹⁾	Max	Units	Vdd	Conditions		
DC10	0.45	0.65	mA	2.0V			
DC19	0.45	0.65	mA	3.3V			
DC23	2.5	3.5	mA	2.0V			
	2.5	3.5	mA	3.3V	- 1 313 - 0 WI 12		
DC24	7.0	9.2	mA	2.0V	Esve - 25 MHz		
	7.0	9.2	mA	3.3V	1 313 – 23 WHZ		
DC25	0.26	0.35	mA	2.0V			
	0.26	0.35	mA	3.3V	- 1515 - 52 NIZ		

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: Base IDD current is measured with:
 - Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
 - + OSC1 pin is driven with external square wave with levels from 0.3V to VDD 0.3V
 - OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
 - FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
 - Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
 - Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
 - Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
 - · All I/O pins (except OSC1) are configured as outputs and driving low
 - No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
 - NOP instructions are executed

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	С		7.20	
Contact Pad Width (X20)	X1	0.45		0.45
Contact Pad Length (X20) Y1				1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072B

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2