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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028-e-ss

Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 5. "Flash Programming"** (DS60001121)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupts"** (DS60001108)
- **Section 10. "Power-Saving Modes"** (DS60001130)
- **Section 14. "Timers"** (DS60001105)
- **Section 19. "Comparator"** (DS60001110)
- **Section 21. "UART"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359)
- **Section 28. "RTCC with Timestamp"** (DS60001362)
- **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381)
- **Section 33. "Programming and Diagnostics"** (DS61129)
- **Section 36. "Configurable Logic Cell"** (DS60001363)
- **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 59. "Oscillators with DCO"** (DS60001329)
- **Section 60. "32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS60001336)
- **Section 62. "Dual Watchdog Timer"** (DS60001365)

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
PGEC1	2	5	2	5	36	39	I	ST	ICSP Port 1 programming clock input
PGEC2	19	2	19	22	25	28	I	ST	ICSP Port 2 programming clock input
PGEC3	7	10	12	15	16	16	I	ST	ICSP Port 3 programming clock input
PGED1	1	4	1	4	35	38	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	20	3	18	21	24	27	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	6	9	11	14	15	15	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	7	10	9	12	10	10	I	ST	Real-Time Clock 50/60 Hz clock input
RA0	19	2	27	2	33	36	I/O	ST/DIG	PORTA digital I/O
RA1	20	3	28	3	34	37	I/O	ST/DIG	PORTA digital I/O
RA2	4	7	6	9	7	7	I/O	ST/DIG	PORTA digital I/O
RA3	5	8	7	10	8	8	I/O	ST/DIG	PORTA digital I/O
RA4	7	10	9	12	10	10	I/O	ST/DIG	PORTA digital I/O
RA9	—	—	—	—	11	11	I/O	ST/DIG	PORTA digital I/O
RB0	1	4	1	4	35	38	I/O	ST/DIG	PORTB digital I/O
RB1	2	5	2	5	36	39	I/O	ST/DIG	PORTB digital I/O
RB2	3	6	3	6	1	1	I/O	ST/DIG	PORTB digital I/O
RB3	—	—	4	7	2	2	I/O	ST/DIG	PORTB digital I/O
RB4	6	9	8	11	9	9	I/O	ST/DIG	PORTB digital I/O
RB5	—	—	11	14	15	15	I/O	ST/DIG	PORTB digital I/O
RB6	—	—	12	15	16	16	I/O	ST/DIG	PORTB digital I/O
RB7	8	11	13	16	17	17	I/O	ST/DIG	PORTB digital I/O
RB8	9	12	14	17	18	18	I/O	ST/DIG	PORTB digital I/O
RB9	10	13	15	18	19	20	I/O	ST/DIG	PORTB digital I/O
RB10	—	—	18	21	24	27	I/O	ST/DIG	PORTB digital I/O
RB11	—	—	19	22	25	28	I/O	ST/DIG	PORTB digital I/O
RB12	12	15	20	23	26	29	I/O	ST/DIG	PORTB digital I/O
RB13	13	16	21	24	27	30	I/O	ST/DIG	PORTB digital I/O
RB14	14	17	22	25	28	31	I/O	ST/DIG	PORTB digital I/O
RB15	15	18	23	26	29	32	I/O	ST/DIG	PORTB digital I/O
RC0	—	—	—	—	3	3	I/O	ST/DIG	PORTC digital I/O
RC1	—	—	—	—	4	4	I/O	ST/DIG	PORTC digital I/O
RC2	—	—	—	—	5	5	I/O	ST/DIG	PORTC digital I/O
RC3	—	—	—	—	14	14	I/O	ST/DIG	PORTC digital I/O
RC8	—	—	—	—	20	21	I/O	ST/DIG	PORTC digital I/O
RC9	—	—	16	19	21	22	I/O	ST/DIG	PORTC digital I/O
REFCLKI	10	13	15	18	19	20	I	ST	Reference clock input
REFCLKO	15	18	23	26	29	32	O	DIG	Reference clock output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM

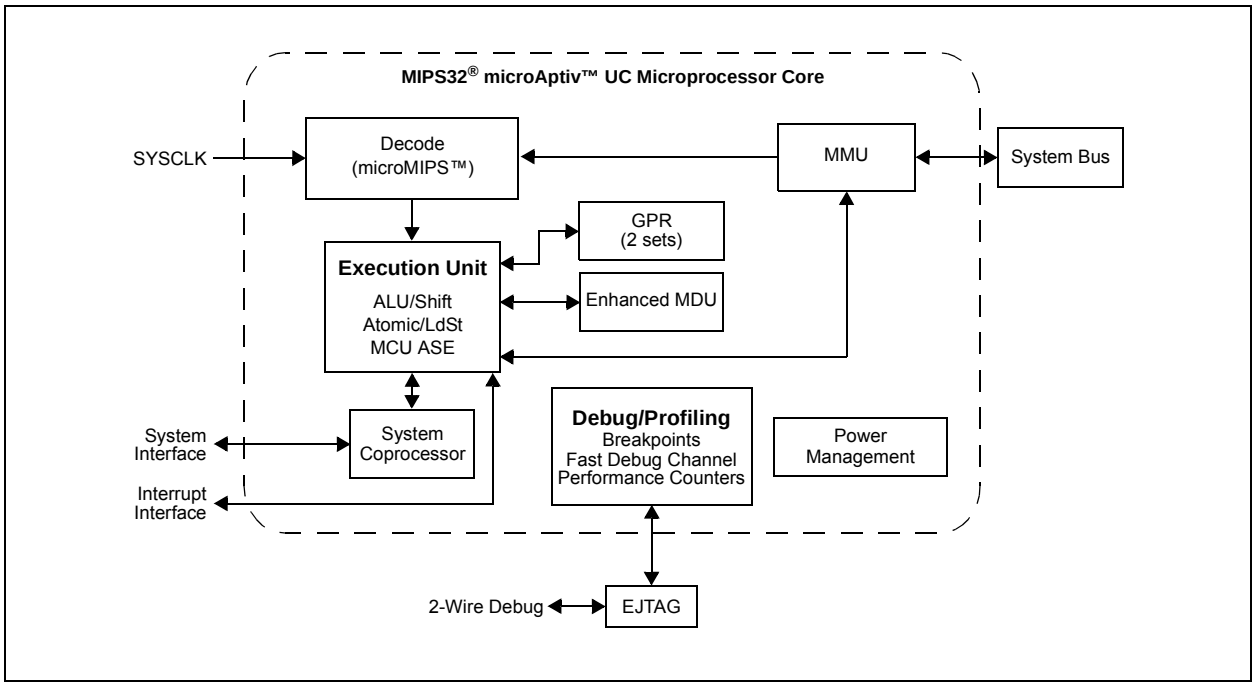


TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.	EBASE + 0x180	CU, EXL	—	CpU (0x0B)	_general_exception_handler
RI	Execution of a reserved instruction.	EBASE + 0x180	EXL	—	RI (0x0A)	_general_exception_handler
Ov	Execution of an arithmetic instruction that overflowed.	EBASE + 0x180	EXL	—	Ov (0x0C)	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE + 0x180	EXL	—	Tr (0x0D)	_general_exception_handler
DDBL	EJTAG data address break (address only) or EJTAG data value break on load (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
DDBS	EJTAG data address break (address only) or EJTAG data value break on store (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
AdES	Store address alignment error.	EBASE + 0x180	EXL	—	ADES (0x05)	_general_exception_handler
DBE	Load or store bus error.	EBASE + 0x180	EXL	—	DBE (0x07)	_general_exception_handler
CBrk	EJTAG complex breakpoint.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIBImpr, DDBLImpr and/or DDBSImpr	—	—
Lowest Priority						

12.0 CAPTURE/COMPARE/PWM/ TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

12.1 Introduction

PIC32MM0064GPL036 family devices include three Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 32-bit microcontrollers. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all earlier PIC32 devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single Capture/Compare/PWM/Timer (SCCPs) output modules provide only one PWM output. Multiple Capture/Compare/PWM/Timer (MCCPs) output modules can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features:

- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for module Interrupt Events or Triggers
- Synchronization Output Signal for Coordinating other MCCP/SCCP modules with User-Configurable Alternate and Auxiliary Source Options
- Fully Asynchronous Operation in all modes and in Low-Power Operation
- Special Output Trigger for ADC Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture modes:
  - Backward compatible with previous input capture peripherals of the PIC32 family
  - 16-bit or 32-bit capture of time base on external event
  - Up to four-level deep FIFO capture buffer
  - Capture source input multiplexer
  - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
  - Backward compatible with previous output compare peripherals of the PIC32 family
  - Single Edge and Dual Edge Compare modes
  - Center-Aligned Compare mode
  - Variable Frequency Pulse mode
  - External Input mode

MCCP modules also include these extended PWM features:

- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can be operated in only one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in Figure 12-1. All three modes use the time base generator and the common Timer register pair (CCPxTMR). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

REGISTER 13-2: SPIxCON2: SPIx CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN(1)	—	—	—	AUDMONO(1,2)	—	AUDMOD<1:0>(1,2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** SPIx Sign-Extend Read Data from the RX FIFO bit
1 = Data from RX FIFO is sign-extended
0 = Data from RX FIFO is not sign-extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
1 = Frame error overflow generates error events
0 = Frame error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
1 = Receive Overflow (ROV) generates error events
0 = Receive Overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
1 = Transmit Underrun (TUR) generates error events
0 = Transmit Underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow (ROV) bit (for audio data transmissions)
1 = A ROV is not a critical error; during ROV, data in the FIFO is not overwritten by receive data
0 = A ROV is a critical error which stops SPIx operation

bit 8 **IGNTUR:** Ignore Transmit Underrun (TUR) bit (for audio data transmissions)
1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error which stops SPIx operation

bit 7 **AUDEN:** Enable Audio Codec Support bit(1)
1 = Audio protocol is enabled
0 = Audio protocol is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
1 = Audio data is mono (each data word is transmitted on both left and right channels)
0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bits(1,2)
11 = PCM/DSP mode
10 = Right Justified mode
01 = Left Justified mode
00 = I^2S mode

Note 1: These bits can only be written when the ON bit = 0.
2: These bits are only valid for AUDEN = 1.

REGISTER 15-1: RTCCON1: RTCC CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	WRLOCK(2)	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RTCOE	OUTSEL<2:0>			—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits(1)
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: To clear this bit, an unlock sequence is required. Refer to **Section 23.4 "System Registers Write Protection"** for details.

16.2 Control Registers

The ADC module has the following Special Function Registers (SFRs):

- **AD1CON1: ADC Control Register 1**
- **AD1CON2: ADC Control Register 2**
- **AD1CON3: ADC Control Register 3**
- **AD1CON5: ADC Control Register 5**

  The AD1CON1, AD1CON2, AD1CON3 and AD1CON5 registers control the operation of the ADC module.

- **AD1CHS: ADC Input Select Register**

  The AD1CHS register selects the input pins to be connected to the SHA.

- **AD1CSS: ADC Input Scan Select Register**

  The AD1CSS register selects inputs to be sequentially scanned.

- **AD1CHIT: ADC Compare Hit Register**

  The AD1CHIT register indicates the channels meeting specified comparison requirements.

Table 16-1 provides a summary of all ADC module related registers, including their addresses and formats. Corresponding registers appear after the summary, followed by a detailed description of each register. All unimplemented registers and/or bits within a register read as zero.

REGISTER 16-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	BUFREGEN(1)	CSCNA	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BUFS	—	SMPI<3:0>				BUFM	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC VR+	ADC VR-
000	AVDD	AVSS
001	AVDD	External VREF- Pin
010	External VREF+ Pin	AVSS
011	External VREF+ Pin	External VREF- Pin
1xx	Unimplemented; do not use	

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference
0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit(1)

1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Mode bit

1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1 (ADC buffers split into 2 x 8-word buffers).
1 = ADC is currently filling Buffers 8-15, user should access data in 0-7
0 = ADC is currently filling Buffers 0-7, user should access data in 8-15

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF(0...7), ADC1BUF(8...15)
0 = Buffer configured as one 16-word buffer, ADC1BUF(0...15)

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit only takes effect when the auto-scan feature is enabled (ASEN (AD1CON5<15>) = 1.

REGISTER 18-1: CLCxCON: CLCx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	G4POL	G3POL	G2POL	G1POL
15:8	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	ON	—	—	—	INTP(1)	INTN(1)	—	—
7:0	R/W-0	R-0, HS, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>		

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 18 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 17 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 16 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

bit 15 **ON:** CLCx Enable bit
1 = CLCx is enabled and mixing input signals
0 = CLCx is disabled and has logic zero outputs

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **INTP:** CLCx Positive Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** CLCx Negative Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **LCOE:** CLCx Port Enable bit
1 = CLCx port pin output is enabled
0 = CLCx port pin output is disabled

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

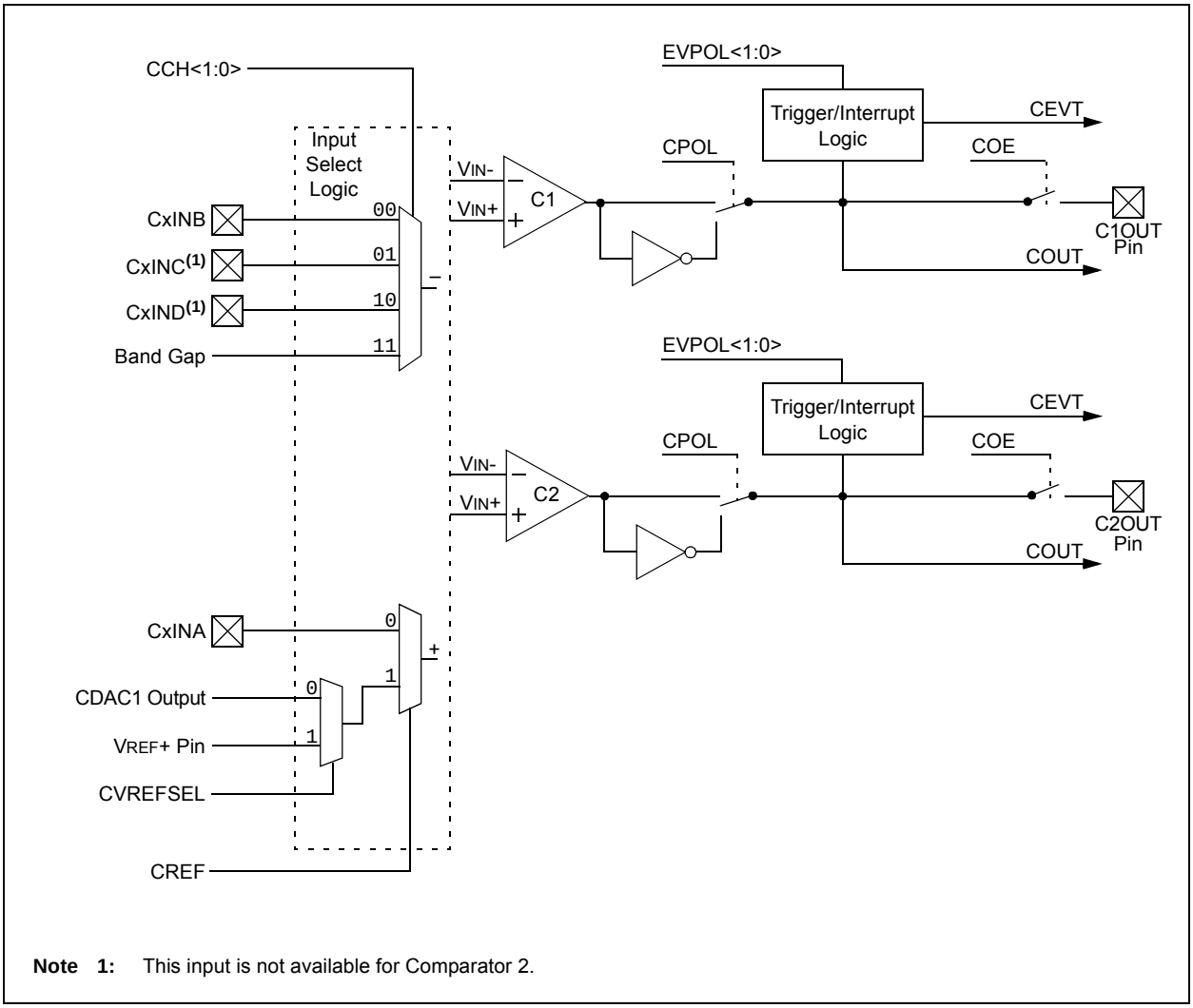
19.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides two dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 19-1. Each comparator has its own control register, CMxCON (Register 19-2), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (Register 19-1).

FIGURE 19-1: DUAL COMPARATOR MODULE BLOCK DIAGRAM



Note 1: This input is not available for Comparator 2.

22.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not take effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default).

To prevent accidental configuration changes under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK bit in PMDCON register (PMDCON<11>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes. To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

Table 22-1 lists the module disable bits and locations for all modules.

TABLE 22-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name	Register Name and Bit Location
Analog-to-Digital Converter (ADC)	ADCMD	PMD1<0>
Voltage Reference (VR)	VREFMD	PMD1<12>
High/Low-Voltage Detect (HLVD)	HLVDMD	PMD1<20>
Comparator 1 (CMP1)	CMP1MD	PMD2<0>
Comparator 2 (CMP2)	CMP2MD	PMD2<1>
Configurable Logic Cell 1 (CLC1)	CLC1MD	PMD2<24>
Configurable Logic Cell 2 (CLC2)	CLC2MD	PMD2<25>
Multiple Outputs Capture/Compare/PWM/ Timer1 (MCCP1)	CCP1MD	PMD3<8>
Single Output Capture/Compare/PWM/Timer2 (SCCP2)	CCP2MD	PMD3<9>
Single Output Capture/Compare/PWM/Timer3 (SCCP3)	CCP3MD	PMD3<10>
Timer1 (TMR1)	T1MD	PMD4<0>
Universal Asynchronous Receiver Transmitter 1 (UART1)	U1MD	PMD5<0>
Universal Asynchronous Receiver Transmitter 2 (UART2)	U2MD	PMD5<1>
Serial Peripheral Interface 1 (SPI1)	SPI1MD	PMD5<8>
Serial Peripheral Interface 2 (SPI2)	SPI2MD	PMD5<9>
Real-Time Clock and Calendar (RTCC)	RTCCMD	PMD6<0>
Reference Clock Output (REFCLKO)	REFOMD	PMD6<8>
Programmable Cyclic Redundancy Check (CRC)	CRCMD	PMD7<3>

TABLE 22-3: PERIPHERAL MODULE DISABLE REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2C00	PMDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PMDLOCK	—	—	—	—	—	—	—	—	—	—	—	0000
2C10	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	HLVDMD	—	—	—	—	FFEF
		15:0	—	—	—	VREFMD	—	—	—	—	—	—	—	—	—	—	—	ADCMD	EFFE
2C20	PMD2	31:16	—	—	—	—	—	—	CLC2MD	CLC1MD	—	—	—	—	—	—	—	—	FCFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP2MD	CMP1MD	FFFC
2C30	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	CCP3MD	CCP2MD	CCP1MD	—	—	—	—	—	—	—	—	F8FF
2C40	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	T1MD	FFFE
2C50	PMD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	r	r	FFFC
		15:0	—	—	—	—	—	—	SPI2MD	SPI1MD	—	—	—	—	—	—	U2MD	U1MD	FCFC
2C60	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	REFOMD	—	—	—	—	—	—	—	RTCCMD	FEFE
2C70	PMD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CRCMD	—	—	—	FFF7

Legend: — = unimplemented, read as '1'; r = reserved bit, maintain as '1'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

REGISTER 23-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER (CONTINUED)

bit 6-5 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Watchdog Timer window size is 25%
10 = Watchdog Timer window size is 37.5%
01 = Watchdog Timer window size is 50%
00 = Watchdog Timer window size is 75%

bit 4-0 **SWDTPS<4:0>:** Sleep Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

24.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

24.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

24.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

24.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

24.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

24.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

TABLE 26-5: IDLE CURRENT (I_{IDLE})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC40	0.26	0.46	mA	2.0V	FSYS = 1 MHz
	0.26	0.46	mA	3.3V	
DC41	0.85	1.5	mA	2.0V	FSYS = 8 MHz
	0.85	1.5	mA	3.3V	
DC42	2.3	3.7	mA	2.0V	FSYS = 25 MHz
	2.3	3.7	mA	3.3V	
DC44	0.18	0.34	mA	2.0V	FSYS = 32 kHz
	0.18	0.34	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = `010` and POSCMOD<1:0> (FOSCSEL<9:8>) = `00`)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = `1`)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = `00`)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = `0` and SOSCSEL (FOSCSEL<12>) = `0`)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = `00` and LPBOREN (FPOR<3>) = `0`)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = `0`)
- All I/O pins (excepting OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

TABLE 26-14: COMPARATOR SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
D300	VIOFF	Input Offset Voltage	-20	—	20	mV
D301	VICM	Input Common-Mode Voltage	AVSS – 0.3V	—	AVDD + 0.3V	V
D307	TRESP(1)	Response Time	—	150	—	ns

Note 1: Measured with one input at VDD/2 and the other transitioning from VSS to VDD.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-15: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
VRD310	TSET	Settling Time(1)	—	—	10	µs
VRD311	VRA	Accuracy	-1	—	1	LSb
VRD312	VRUR	Unit Resistor Value (R)	—	4.5	—	kΩ

Note 1: Measures the interval while VRDAT<4:0> transitions from '11111' to '00000'.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 26-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

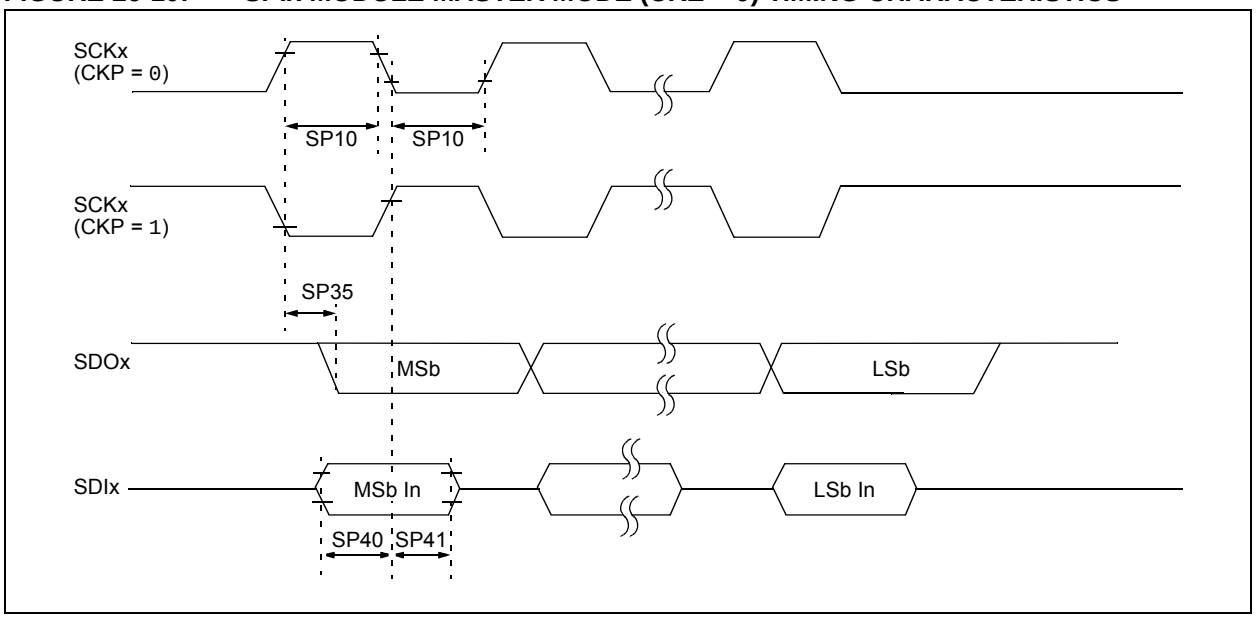
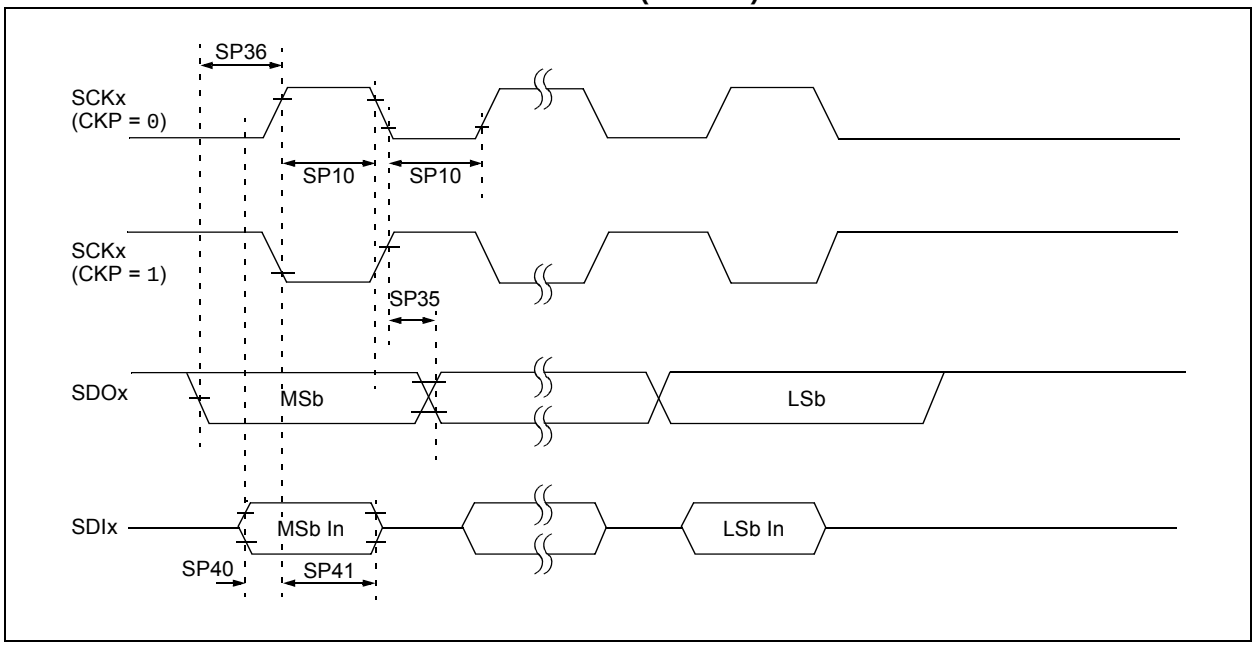


FIGURE 26-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



NOTES: