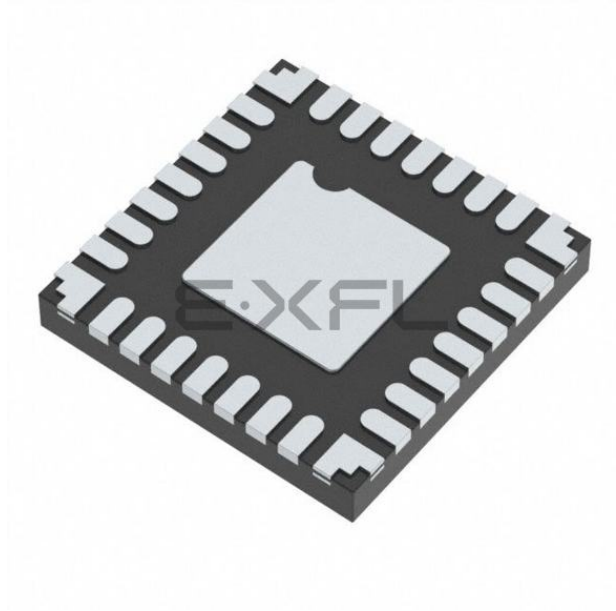


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028-i-m6

NOTES:

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0064GPL036 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0064GPL036 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0064GPL036 FAMILY BLOCK DIAGRAM

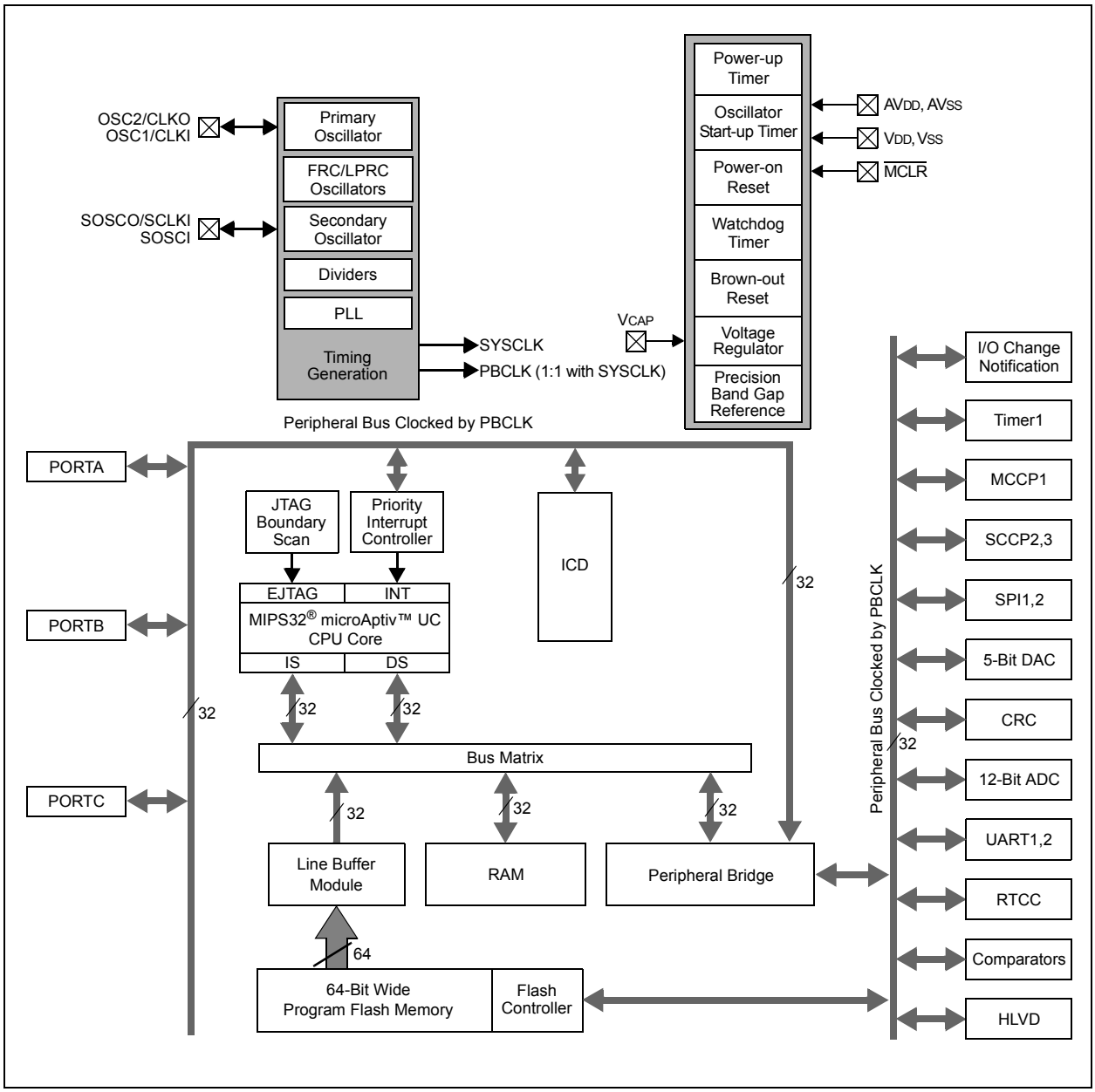


TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
RP1	19	2	27	2	33	36	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	20	3	28	3	34	37	I/O	ST/DIG	
RP3	4	7	6	9	7	7	I/O	ST/DIG	
RP4	5	8	7	10	8	8	I/O	ST/DIG	
RP5	6	9	8	11	9	9	I/O	ST/DIG	
RP6	7	10	9	12	10	10	I/O	ST/DIG	
RP7	9	12	14	17	18	18	I/O	ST/DIG	
RP8	10	13	15	18	19	20	I/O	ST/DIG	
RP9	14	17	22	25	28	31	I/O	ST/DIG	
RP10	15	18	23	26	29	32	I/O	ST/DIG	
RP11	8	11	13	16	17	17	I/O	ST/DIG	
RP12	12	15	20	23	26	29	I/O	ST/DIG	
RP13	13	16	21	24	27	30	I/O	ST/DIG	
RP14	1	4	1	4	35	38	I/O	ST/DIG	
RP15	2	5	2	5	36	39	I/O	ST/DIG	
RP16	3	6	3	6	1	1	I/O	ST/DIG	
RP17	—	—	18	21	24	27	I/O	ST/DIG	
RP18	—	—	19	22	25	28	I/O	ST/DIG	
RP19	—	—	16	19	21	22	I/O	ST/DIG	
RP20	—	—	—	—	11	11	I/O	ST/DIG	
RTCC	14	17	22	25	28	31	O	DIG	Real-Time Clock alarm/seconds output
SCK1	9	12	14	17	18	18	I/O	ST/DIG	SPI1 clock (input or output)
SCLKI	7	10	9	12	10	10	I	ST	Secondary Oscillator external clock input
SDI1	14	17	22	25	28	31	I	ST	SPI1 data input
SDO1	10	13	15	18	19	20	O	DIG	SPI1 data output
SOSCI	6	9	8	11	9	9	—	—	Secondary Oscillator crystal
SOSCO	7	10	9	12	10	10	—	—	Secondary Oscillator crystal
$\overline{SS1}$	15	18	23	26	29	32	I	ST	SPI1 slave select input
T1CK	10	13	15	18	19	20	I	ST	Timer1 external clock input
T1G	10	13	15	18	19	20	I	ST	Timer1 clock gate input
TCK	9	12	14	17	18	18	I	ST	JTAG clock input
TDI	13	16	19	22	25	28	I	ST	JTAG data input
TDO	12	15	18	21	24	27	O	DIG	JTAG data output
TMS	10	13	15	18	19	20	I	ST	JTAG mode select input
U1BCLK	10	13	15	18	19	20	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{U1CTS}$	9	12	14	17	18	18	I	ST	UART1 transmission control input
$\overline{U1RTS}$	10	13	15	18	19	20	O	DIG	UART1 reception control output
U1RX	15	18	23	26	29	32	I	ST	UART1 receive data input
U1TX	14	17	22	25	28	31	O	DIG	UART1 transmit data output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

REGISTER 10-1: T1CON: TIMER1 CONTROL REGISTER (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Selection bit

When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized

When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit

1 = External clock is defined by the TECS<1:0> bits
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

REGISTER 12-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>		
15:8	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
	PWMRSEN	ASDGM	—	SSDG	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ASDG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **OC<F:A>EN:** Output Enable/Steering Control bits(1)
1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 23-22 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 21 **Unimplemented:** Read as '0'

bit 20-19 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output depends on module operating mode
01 = Time base rollover event (all modes)
00 = Disabled

bit 18-16 **ICS<2:0>:** Input Capture Source Select bits
111 = Reserved
110 = Reserved
101 = CLC2 output
100 = CLC1 output
011 = Reserved
010 = Comparator 2 output
001 = Comparator 1 output
000 = ICMx pin (remappable)

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0 = ASEVT must be cleared in software to resume PWM activity on output pins

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.

REGISTER 15-5: RTCDATE: RTCC DATE REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	YRTEN<3:0>				YRONE<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YRTEN<3:0>:** Binary Coded Decimal Value of Years 10-Digit bits

bit 27-24 **YRONE<3:0>:** Binary Coded Decimal Value of Years 1-Digit bits

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

TABLE 16-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(3)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07E0	ADC1BUF14	31:16	ADC1BUF14<31:0>																0000
		15:0																	0000
07F0	ADC1BUF15	31:16	ADC1BUF15<31:0>																0000
		15:0																	0000
0800	AD1CON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON		SIDL	—	—	FORM<2:0>			SSRC<3:0>				MODE12	ASAM	SAMP	DONE	0000
0810	AD1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	—	0000
0820	AD1CON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	EXTSAM	—	SAMC<4:0>					ADCS<7:0>								0000
0840	AD1CHS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CH0NA<2:0>			CH0SA<4:0>					0000
0850	AD1CSS	31:16	—	CSS<30:28>			—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CSS<13:0>(1,2)														0000
0870	AD1CON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ASEN	LPEN	—	BGREQ	—	—	ASINT<1:0>		—	—	—	—	WM<1:0>		CM<1:0>		0000
0880	AD1CHIT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CHH<13:0>(1,2)														0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

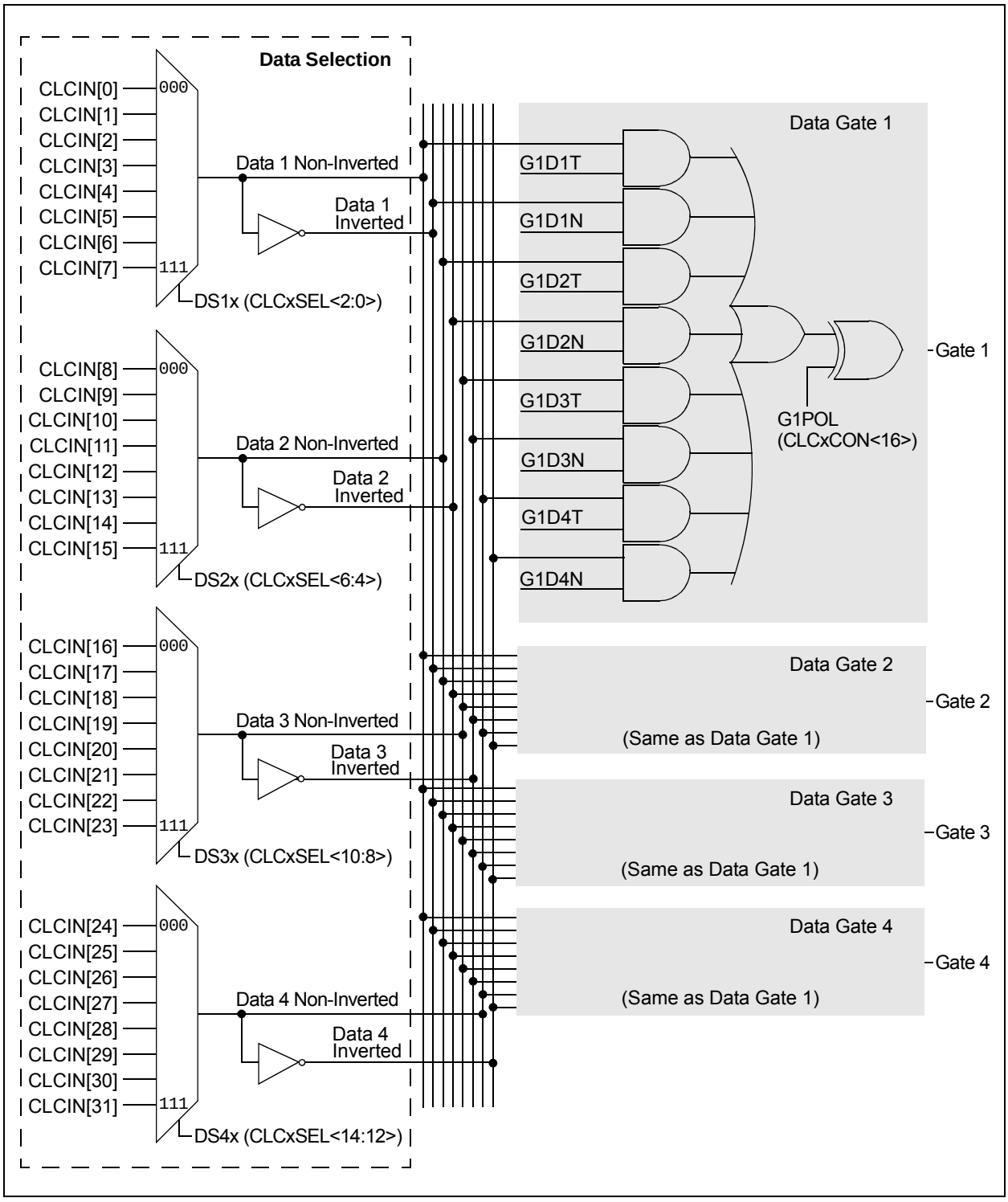
Note 1: The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

2: The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

NOTES:

FIGURE 18-3: CLCx INPUT SOURCE SELECTION DIAGRAM



22.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not take effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default).

To prevent accidental configuration changes under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK bit in PMDCON register (PMDCON<11>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes. To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

Table 22-1 lists the module disable bits and locations for all modules.

TABLE 22-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name	Register Name and Bit Location
Analog-to-Digital Converter (ADC)	ADCMD	PMD1<0>
Voltage Reference (VR)	VREFMD	PMD1<12>
High/Low-Voltage Detect (HLVD)	HLVDMD	PMD1<20>
Comparator 1 (CMP1)	CMP1MD	PMD2<0>
Comparator 2 (CMP2)	CMP2MD	PMD2<1>
Configurable Logic Cell 1 (CLC1)	CLC1MD	PMD2<24>
Configurable Logic Cell 2 (CLC2)	CLC2MD	PMD2<25>
Multiple Outputs Capture/Compare/PWM/ Timer1 (MCCP1)	CCP1MD	PMD3<8>
Single Output Capture/Compare/PWM/Timer2 (SCCP2)	CCP2MD	PMD3<9>
Single Output Capture/Compare/PWM/Timer3 (SCCP3)	CCP3MD	PMD3<10>
Timer1 (TMR1)	T1MD	PMD4<0>
Universal Asynchronous Receiver Transmitter 1 (UART1)	U1MD	PMD5<0>
Universal Asynchronous Receiver Transmitter 2 (UART2)	U2MD	PMD5<1>
Serial Peripheral Interface 1 (SPI1)	SPI1MD	PMD5<8>
Serial Peripheral Interface 2 (SPI2)	SPI2MD	PMD5<9>
Real-Time Clock and Calendar (RTCC)	RTCCMD	PMD6<0>
Reference Clock Output (REFCLKO)	REFOMD	PMD6<8>
Programmable Cyclic Redundancy Check (CRC)	CRCMD	PMD7<3>

REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	SOSCSEL	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	IESO	SOSCEN	—	PLLSRC	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
- 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
- 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
- 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
- 1 = Crystal is used (RA4 and RB4 pins are controlled by SOSC)
- 0 = External clock is connected to the SOSCO pin (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
- 1 = OSC2/CLKO pin operates as normal I/O
- 0 = System clock is connected to the OSC2/CLKO pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit
- 1 = Two-Speed Start-up is enabled
- 0 = Two-Speed Start-up is disabled

bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Secondary Oscillator is enabled
- 0 = Secondary Oscillator is disabled

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit
- 1 = FRC oscillator is selected as the PLL reference input on a device Reset
- 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

TABLE 23-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 23-10: ANCFG: BAND GAP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS, HC	R/W-0, HS, HC	U-0
	—	—	—	—	—	VBGADC	VBGCMP	—

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **VBGADC:** ADC Band Gap Enable bit
1 = ADC band gap is enabled
0 = ADC band gap is disabled

bit 1 **VBGCMP:** Comparator Band Gap Enable bit
1 = Comparator band gap is enabled
0 = Comparator band gap is disabled

bit 0 **Unimplemented:** Read as '0'

TABLE 26-6: POWER-DOWN CURRENT (I_{PD})(2)

Parameter No.	Typical(1)	Max	Units	Operating Temperature	VDD	Conditions
DC60	134	198	µA	-40°C	2.0V	Sleep with active main voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) =0)
	136	208	µA	+25°C		
	141	217	µA	+85°C		
	139	209	µA	-40°C	3.3V	
	141	217	µA	+25°C		
	143	231	µA	+85°C		
DC61	4.3	11.7	µA	-40°C	2.0V	Sleep with main voltage regulator in Standby mode (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 0)
	5.1	15.6	µA	+25°C		
	11.4	34.3	µA	+85°C		
	6.1	16.8	µA	-40°C	3.3V	
	6.9	20.1	µA	+25°C		
	12.7	36.0	µA	+85°C		
DC62	2.3	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	2.7	—	µA	+25°C		
	5.2	—	µA	+85°C		
	2.3	—	µA	-40°C	3.3V	
	2.7	—	µA	+25°C		
	5.4	—	µA	+85°C		
DC63	0.28	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	0.44	—	µA	+25°C		
	2.52	—	µA	+85°C		
	0.29	—	µA	-40°C	3.3V	
	0.44	—	µA	+25°C		
	2.62	—	µA	+85°C		

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with:

- Oscillator is configured in FRC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 000)
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

TABLE 26-7: INCREMENTAL PERIPHERAL Δ CURRENT(2)

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)			
Parameter No.	**Typ(1)**	**Units**	**Conditions**
Brown-out Reset Incremental Current (ΔBOR)			
DC71	2.7	µA	
Watchdog Timer Incremental Current (ΔWDT)			
DC72	80	nA	with LPRC
High/Low-Voltage Detect Incremental Current (ΔHLVD)			
DC73	2.1	µA	
Real-Time Clock and Calendar Incremental Current (ΔRTCC)			
DC74	1.0	µA	with SOSC
DC75	0.4	µA	with LPRC
ADC Incremental Current (ΔADC)			
DC76	450	µA	12-bit, 100 ksps, with FRC
FRC Oscillator Incremental Current (ΔFRC)			
DC78	305	µA	
PLL Incremental Current (ΔPLL)			
DC79	1230	µA	FVCO = 24 MHz
DC80	1550	µA	FVCO = 48 MHz
Digital-to-Analog Converter Incremental Current, CDAC (ΔDAC)			
DC81	27.5	µA	
Low-Power BOR Incremental Current (ΔLPBOR)			
DC82	200	nA	
Comparator Incremental Current (ΔCMP)			
DC83	24.0	µA	

Note 1: Data in the “Typ” column is for design guidance only and is not tested.

2: The Δ current is an additional current consumed when the module is enabled. This current should be added to the base IPD current.

TABLE 26-10: I/O PIN OUTPUT SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**				
DO10		I/O Ports	—	0.36	V	IOL = 6.0 mA, VDD = 3.6V
			—	0.21	V	IOL = 3.0 mA, VDD = 2V
DO16		RA3, RB8, RB9 and RB15 I/O Ports	—	0.16	V	IOL = 6.0 mA, VDD = 3.6V
			—	0.12	V	IOL = 3.0 mA, VDD = 2V
	VOH	**Output High Voltage**				
DO20		I/O Ports	3.25	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.4	—	V	IOH = -3.0 mA, VDD = 2V
DO26		RA3, RB8, RB9 and RB15 I/O Ports	3.3	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.55	—	V	IOH = -3.0 mA, VDD = 2V

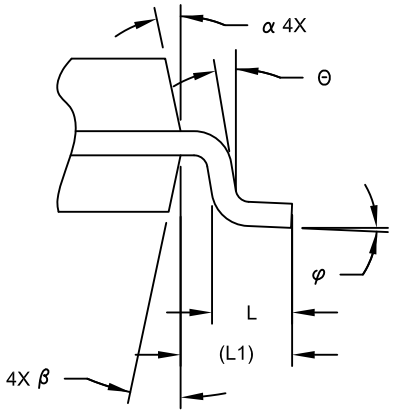
TABLE 26-11: PROGRAM FLASH MEMORY SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D130	EP	Cell Endurance	10000	20000	—	E/W	
D131	VICSP	VDD for In-Circuit Serial Programming™ (ICSP™)	VBOR	—	3.6	V	
D132	VRTSP	VDD for Run-Time Self-Programming (RTSP)	2.0	—	3.6	V	
D133	TIW	Self-Timed Double-Word Write Cycle Time	19.7	21.0	22.3	µs	8 bytes, data is not all ‘1’s
		Self-Timed Row Write Cycle Time	1.3	1.4	1.5	ms	256 bytes, data is not all ‘1’s, SYSCLK > 2 MHz
D133	TIE	Self-Timed Page Erase Time	15.0	16.0	17.0	ms	2048 bytes
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D136	TCE	Self-Timed Chip Erase Time	16.0	17.0	18.0	ms	

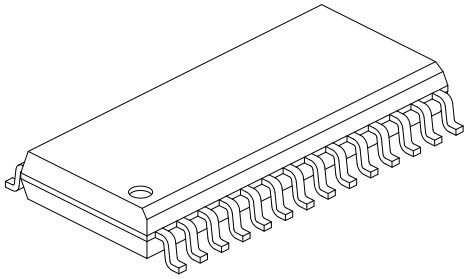
Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

NOTES:

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-0653-2