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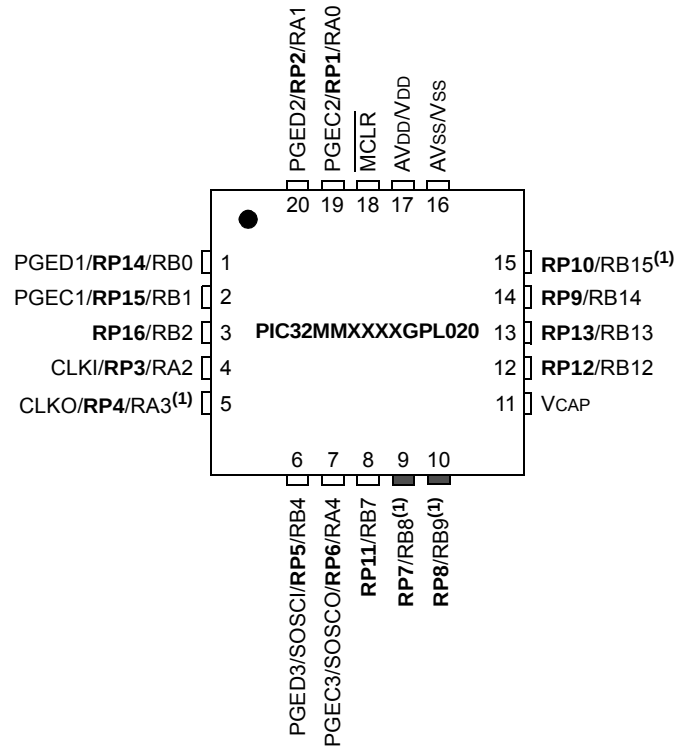
Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I ² S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028-i-so

PIC32MM0064GPL036 FAMILY

Pin Diagrams (Continued)

20-Pin QFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 “Electrical Characteristics”** for details.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN QFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/RP14/RB0	11	VCAP
2	PGEC1/AN3/C1INC/C2INA/RP15/RB1	12	TDO/AN7/LVDIN/RP12/RB12
3	AN4/RP16/RB2	13	TDI/AN8/RP13/RB13
4	OSC1/CLKI/AN5/C1INB/RP3/OCM1C/RA2	14	CDAC1/AN9/RP9/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
5	OSC2/CLKO/AN6/C1INA/RP4/OCM1D/RA3 ⁽¹⁾	15	AN10/REFCLKO/RP10/U1RX/SS1/FSYNC1/INT0/RB15 ⁽¹⁾
6	PGED3/SOSCI/RP5/RB4	16	AVss/Vss
7	PGEC3/SOSCO/SCLKI/RP6/PWRLCLK/RA4	17	AVdd/Vdd
8	RP11/RB7	18	MCLR
9	TCK/RP7/U1CTS/SCK1/OCM1A/RB8 ⁽¹⁾	19	PGEC2/VREF+/AN0/RP1/OCM1E/INT3/RA0
10	TMS/REFCLKI/RP8/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9 ⁽¹⁾	20	PGED2/VREF-/AN1/RP2/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

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NOTES:

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REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit
1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit
0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® are present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating-Point Unit bit
0 = Floating-Point Unit is not implemented

TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
UART1 Reception	_UART1_RX_VECTOR	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	Yes
UART1 Transmission	_UART1_TX_VECTOR	24	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	Yes
UART1 Error	_UART1_ERR_VECTOR	25	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	Yes
CCP1 Input Capture or Output Compare	_CCP1_VECTOR	29	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	No
CCP1 Timer	_CCT1_VECTOR	30	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	No
CCP2 Input Capture or Output Compare	_CCP2_VECTOR	31	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
CCP2 Timer	_CCT2_VECTOR	32	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
CCP3 Input Capture or Output Compare	_CCP3_VECTOR	33	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	No
CCP3 Timer	_CCT3_VECTOR	34	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	No
RESERVED	—	35	—	—	—	—	—
RESERVED	—	36	—	—	—	—	—
SPI2 Error	_SPI2_ERR_VECTOR	37	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
SPI2 Transmission	_SPI2_TX_VECTOR	38	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
SPI2 Reception	_SPI2_RX_VECTOR	39	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	Yes
UART2 Reception	_UART2_RX_VECTOR	40	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	Yes
UART2 Transmission	_UART2_TX_VECTOR	41	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
UART2 Error	_UART2_ERR_VECTOR	42	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
NVM Program or Erase Complete	_NVM_VECTOR	46	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
Core Performance Counter	_PERFORMANCE_COUNTER_VECTOR	47	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	No

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REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	SRIPL<2:0> ⁽¹⁾		
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SIRQ<7:0>							

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level for Single Vector Mode bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits

11111111-00000000 = The last interrupt request number serviced by the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:	W = Writable bit	U = Unimplemented bit, read as '0'
R = Readable bit	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown
-n = Value at POR		

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the interrupt proximity timer as a reload value when the interrupt proximity timer is triggered by an interrupt event.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x⁽¹⁾

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note 1: This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

11.0 WATCHDOG TIMER (WDT)

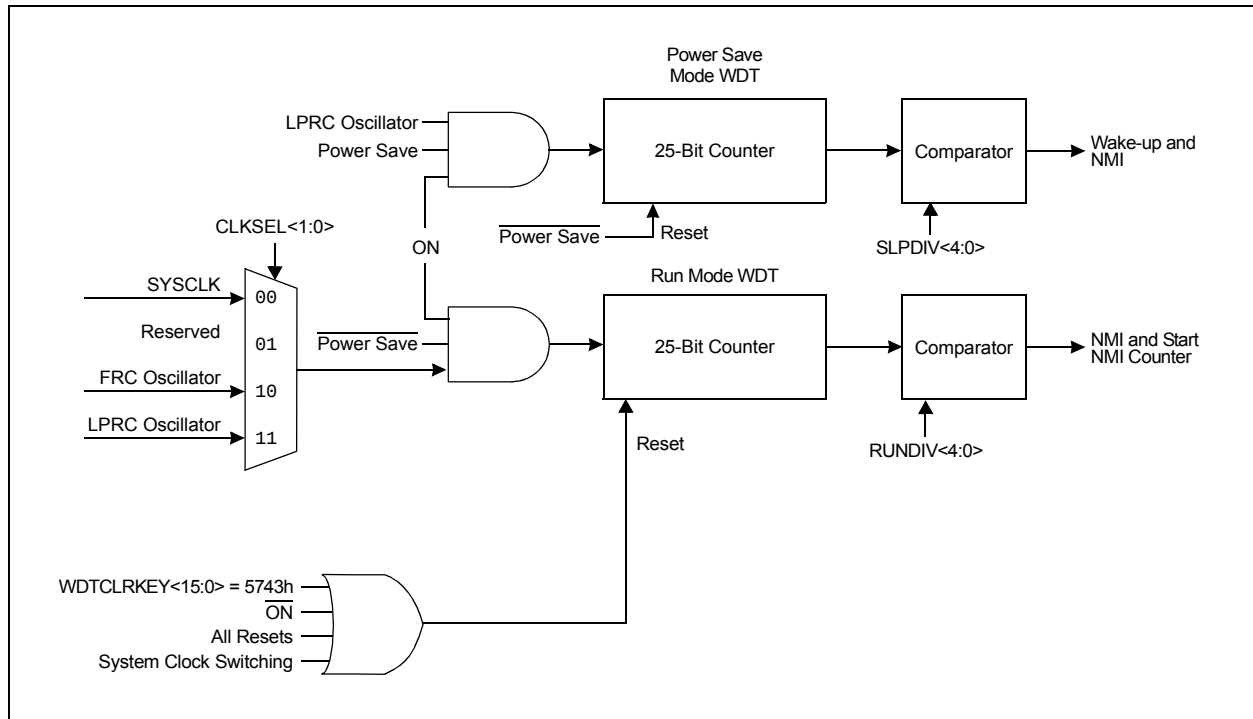
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. “Dual Watchdog Timer”** (DS60001365) in the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 12-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER (CONTINUED)

- bit 3 **SCEVT:** Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred
- bit 2 **ICDIS:** Input Capture Disable bit
1 = Event on input capture pin does not generate a capture event
0 = Event on input capture pin will generate a capture event
- bit 1 **ICOV:** Input Capture Buffer Overflow Status bit
1 = The input capture FIFO buffer has overflowed
0 = The input capture FIFO buffer has not overflowed
- bit 0 **ICBNE:** Input Capture Buffer Status bit
1 = The input capture buffer has data available
0 = The input capture buffer is empty

Note 1: This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

15.1 RTCC Control Registers

TABLE 15-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
0000	RTCCON1	31:16	ALRMEN	CHIME	—	—	AMASK<3:0>				ALMRPT<7:0>							0000	
		15:0	ON	—	—	—	WRLOCK	—	—	—	RTCOE	OUTSEL<2:0>			—	—	—	—	0000
0010	RTCCON2	31:16	DIV<15:0>															0000	
		15:0	FDIV<4:0>					—	—	—	—	—	—	—	—	—	CLKSEL<1:0>	0000	
0030	RTCSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC	0000
0040	RTCTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>					SECONE<3:0>				—	—	—	—	—	—	—	—
0050	RTCDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MHTTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000
0060	ALMTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>					SECONE<3:0>				—	—	—	—	—	—	—	—
0070	ALMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MHTTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

16.2 Control Registers

The ADC module has the following Special Function Registers (SFRs):

- **AD1CON1: ADC Control Register 1**
- **AD1CON2: ADC Control Register 2**
- **AD1CON3: ADC Control Register 3**
- **AD1CON5: ADC Control Register 5**

The AD1CON1, AD1CON2, AD1CON3 and AD1CON5 registers control the operation of the ADC module.

- **AD1CHS: ADC Input Select Register**

The AD1CHS register selects the input pins to be connected to the SHA.

- **AD1CSS: ADC Input Scan Select Register**

The AD1CSS register selects inputs to be sequentially scanned.

- **AD1CHIT: ADC Compare Hit Register**

The AD1CHIT register indicates the channels meeting specified comparison requirements.

Table 16-1 provides a summary of all ADC module related registers, including their addresses and formats. Corresponding registers appear after the summary, followed by a detailed description of each register. All unimplemented registers and/or bits within a register read as zero.

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REGISTER 16-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	BUFREGEN ⁽¹⁾	CSCNA	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BUFS	—	SMPI<3:0>				BUFM	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC Vr+	ADC Vr-
000	AVDD	AVss
001	AVDD	External VREF- Pin
010	External VREF+ Pin	AVss
011	External VREF+ Pin	External VREF- Pin
1xx	Unimplemented; do not use	

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference

0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit⁽¹⁾

1 = Conversion result is loaded into the buffer location determined by the converted channel

0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Mode bit

1 = Scans inputs

0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1 (ADC buffers split into 2 x 8-word buffers).

1 = ADC is currently filling Buffers 8-15, user should access data in 0-7

0 = ADC is currently filling Buffers 0-7, user should access data in 8-15

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence

1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence

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0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence

0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF(0...7), ADC1BUF(8...15)

0 = Buffer configured as one 16-word buffer, ADC1BUF(0...15)

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit only takes effect when the auto-scan feature is enabled (ASEN (AD1CON5<15>) = 1).

TABLE 18-1: CLC1 AND CLC2 REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A80	CLC1CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	—	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
0A90	CLC1SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
0AA0	CLC1GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
0B00	CLC2CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	—	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
0B10	CLC2SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
0B20	CLC2GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 19-1: CMSTAT: COMPARATOR MODULE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	—	C2EVT	C1EVT
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SIDL	—	—	—	—	CVREFSEL
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-18 **Unimplemented:** Read as '0'

bit 17 **C2EVT:** Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 16 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all enabled comparators in Idle mode

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **CVREFSEL:** Comparator Reference Voltage Select Enable bit
1 = External voltage reference from the VREF+ pin is selected
0 = Voltage from CDAC1 is selected

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

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TABLE 26-18: PLL CLOCK TIMING SPECIFICATIONS

Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ (unless otherwise stated)					
Param No.	Symbol	Characteristic	Min	Max	Units
OS50	FPLLI	PLL Input Frequency Range ⁽¹⁾	2	24	MHz
OS54	FPLLO	PLL Output Frequency Range ⁽¹⁾	16	96	MHz
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	24	μs
OS53	DCLK	CLKO Stability (Jitter)	-0.12	0.12	%

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 26-19: INTERNAL OSCILLATOR ACCURACY⁽¹⁾

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	Characteristic	Min	Typ ⁽²⁾	Max	Units
F20	FRC Accuracy @ 8 MHz	-3	—	3	%
F21	LPRC @ 32 kHz	-20	—	20	%
F22	FRC Tune Step-Size (in OSCTUN register)	—	0.05	—	%/Bit

Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

2: Data in the “Typ” column is 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-20: INTERNAL OSCILLATOR START-UP TIME

Operating Conditions: $2.0V \leq V_{DD} \leq 3.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ (unless otherwise stated)				
Param No.	Symbol	Characteristic	Max	Units
FR0	TFRC	FRC Oscillator Start-up Time	2	μs
FR1	TLPRC	Low-Power RC Oscillator Start-up Time	70	μs

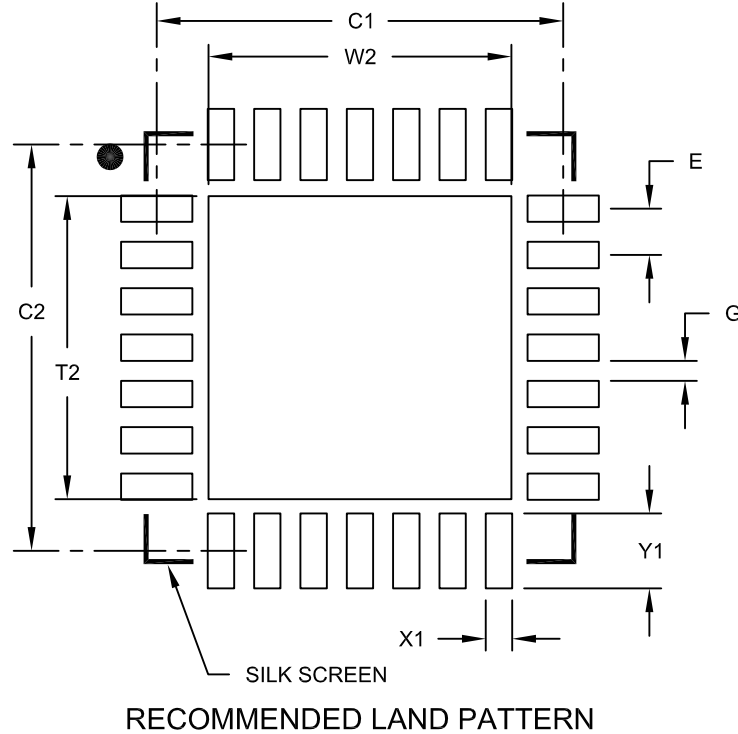
PIC32MM0064GPL036 FAMILY

NOTES:

PIC32MM0064GPL036 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

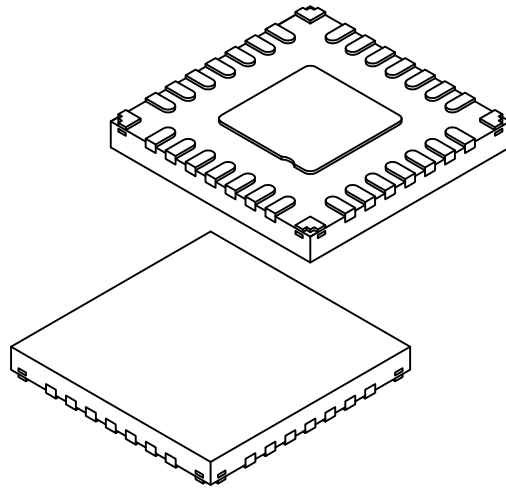
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

PIC32MM0064GPL036 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.40 BSC		
Overall Height	A	-	-	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.152 REF		
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	1.80	1.90	2.00
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	1.80	1.90	2.00
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1	0.40	0.45	0.50
Corner Pad, Metal Free Zone	b2	0.18	0.23	0.28
Terminal Length	L	0.30	0.45	0.50
Terminal-to-Exposed-Pad	K	-	0.60	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

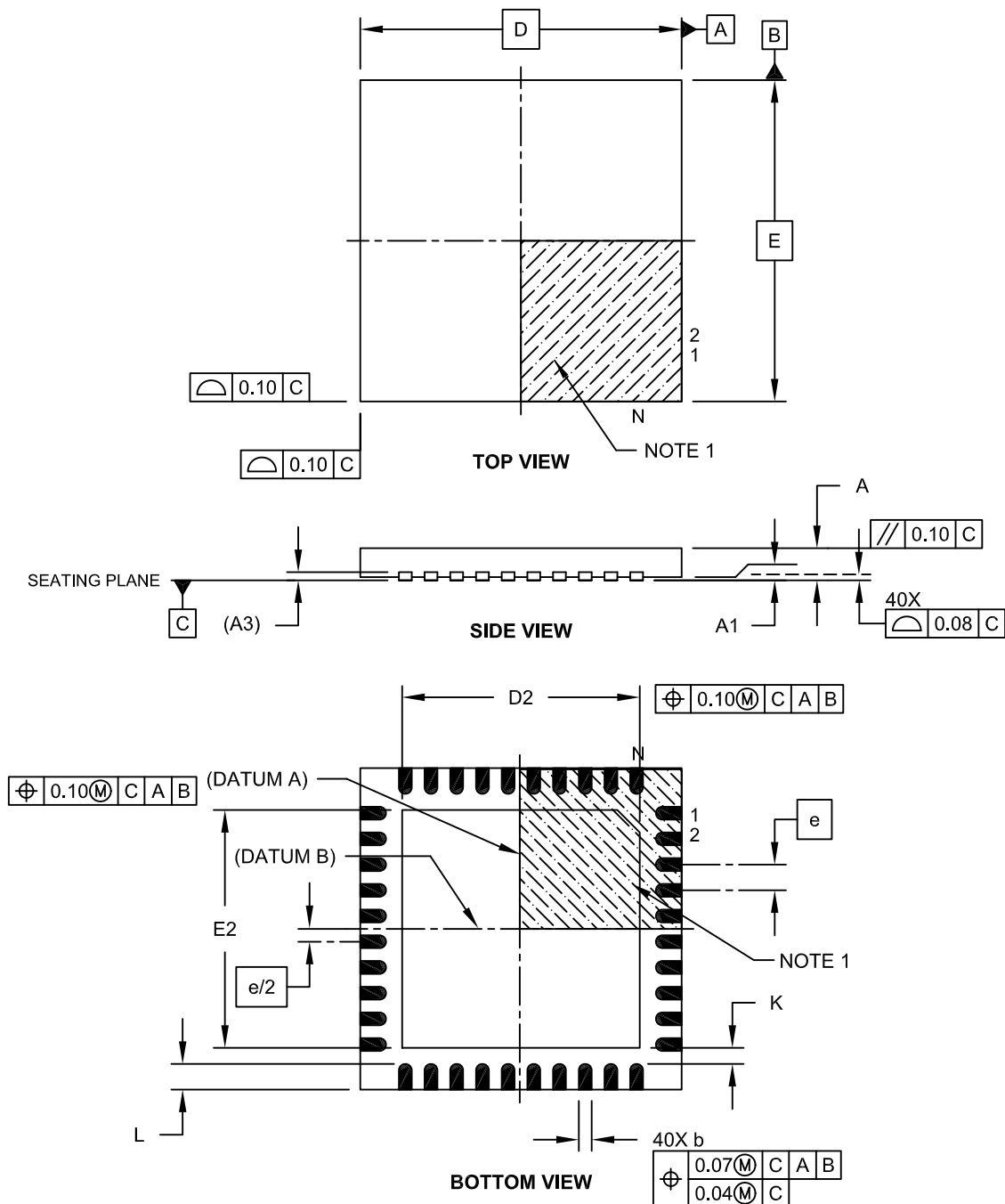
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-333-M6 Rev A Sheet 2 of 2

PIC32MM0064GPL036 FAMILY

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-156A Sheet 1 of 2

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PIC32MM0064GPL036 FAMILY

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

	PIC32	MM	XXXX	GP	L	XXX	T - XXX
Microchip Brand	_____	_____	_____	_____	_____	_____	_____
Architecture	_____	_____	_____	_____	_____	_____	_____
Flash Memory Size	_____	_____	_____	_____	_____	_____	_____
Family	_____	_____	_____	_____	_____	_____	_____
Key Feature Set	_____	_____	_____	_____	_____	_____	_____
Pin Count	_____	_____	_____	_____	_____	_____	_____
Tape and Reel Flag (if applicable)	_____	_____	_____	_____	_____	_____	_____
Pattern	_____	_____	_____	_____	_____	_____	_____

Architecture	MM = MIPS32® microAptiv™ UC CPU Core
Flash Memory Size	0016 = 16 Kbytes 0032 = 32 Kbytes 0064 = 64 Kbytes
Family	GP = General Purpose Family
Key Feature	L = Up to 25 MHz operating frequency with basic peripheral set of 2 UART and 2 SPI modules
Pin Count	020 = 20-pin 028 = 28-pin 036 = 36/40-pin
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample

Example:
PIC32MM0064GPL036-I/M2:
PIC32 General Purpose Device
with MIPS32® microAptiv™ UC
Core, 64-Kbyte Program Memory,
36-Pin Package.