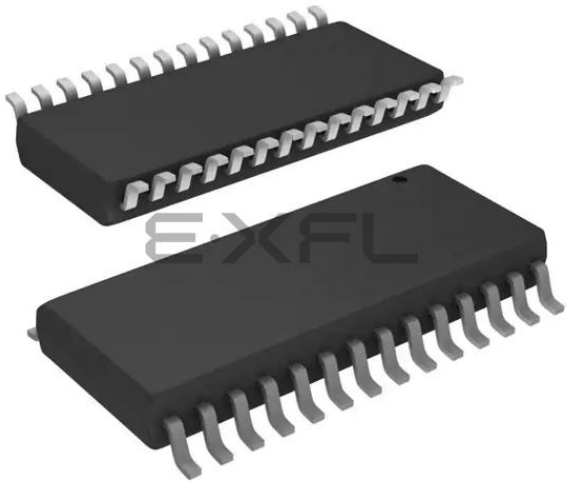
Microchip Technology - PIC32MM0064GPL028T-I/SO Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028t-i-so

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit
1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit
0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® are present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating-Point Unit bit
0 = Floating-Point Unit is not implemented

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

5.2 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2380	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	—	—	—	—	NVMOP<3:0>				0000
2390	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
23A0	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
23B0	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
23C0	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
23D0	NVMSRCADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
23E0	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
23F0	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BWPULOCK	—	—	—	—	BWP<2:0>			—	—	—	—	—	—	—	—	8700

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

REGISTER 8-4: REFO1TRIM: REFERENCE OSCILLATOR TRIM REGISTER(1,2,3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to the RODIVx value
111111110 = 510/512 divisor added to the RODIVx value
•
•
•
100000000 = 256/512 divisor added to the RODIVx value
•
•
•
000000010 = 2/512 divisor added to the RODIVx value
000000001 = 1/512 divisor added to the RODIVx value
000000000 = 0 divisor added to the RODIVx value

bit 22-0 **Unimplemented:** Read as '0'

Note 1: While the ON bit (REFO1CON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

2: Do not write to this register when the ON bit (REFO1CON<15>) is not equal to the ACTIVE bit (REFO1CON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFO1CON<30:16>) = 0.

REGISTER 12-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>		
15:8	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
	PWMRSEN	ASDGM	—	SSDG	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ASDG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **OC<F:A>EN:** Output Enable/Steering Control bits(1)
1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 23-22 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 21 **Unimplemented:** Read as '0'

bit 20-19 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output depends on module operating mode
01 = Time base rollover event (all modes)
00 = Disabled

bit 18-16 **ICS<2:0>:** Input Capture Source Select bits
111 = Reserved
110 = Reserved
101 = CLC2 output
100 = CLC1 output
011 = Reserved
010 = Comparator 2 output
001 = Comparator 1 output
000 = ICMx pin (remappable)

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0 = ASEVT must be cleared in software to resume PWM activity on output pins

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.

REGISTER 12-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER (CONTINUED)

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
1 = Waits until the next Time Base Reset or rollover for shutdown to occur
0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting the ASDGM bit still applies)
0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
1xxx xxxx = Auto-shutdown is controlled by the OCFB pin (remappable)
x1xx xxxx = Auto-shutdown is controlled by the OCFA pin (remappable)
xx1x xxxx = Auto-shutdown is controlled by CLC1 for MCCP1/SCCP2 and by CLC2 for SCCP3
xxx1 xxxx = Auto-shutdown is controlled by the SCCP2 output for MCCP1 and by MCCP1 for SCCP2/SCCP3
xxxx 1xxx = Auto-shutdown is controlled by the SCCP3 output for MCCP1/SCCP2 and by SCCP2 for SCCP3
xxxx x1xx = Reserved
xxxx xx1x = Auto-shutdown is controlled by Comparator 2
xxxx xxx1 = Auto-shutdown is controlled by Comparator 1

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.

REGISTER 15-3: RTCSTAT: RTCC STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0, HS, HC	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
- 1 = An alarm event has occurred
- 0 = An alarm event has not occurred

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Synchronization Status bit
- 1 = Time registers may change during software read
- 0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization status bit
- 1 = Alarm registers (ALMTIME and ALMDATE) and RTCCON1 should not be modified; the ALRMEN and ALMRPT<7:0> bits may change during software read
- 0 = Alarm registers and Alarm Control registers may be modified safely

bit 0 **HALFSEC:** Half Second Status bit
- 1 = Second half of 1-second period
- 0 = First half of 1-second period

REGISTER 15-4: RTCTIME/ALMTIME: RTCC/ALARM TIME REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	HRTEN<2:0>			HRONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SECTEN<3:0>				SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-28 **HRTEN<2:0>:** Binary Coded Decimal Value of Hours 10-Digit bits
Contains a value from 0 to 2.

bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours 1-Digit bits
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes 10-Digit bits
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes 1-Digit bits
Contains a value from 0 to 9.

bit 15-12 **SECTEN<3:0>:** Binary Coded Decimal Value of Seconds 10-Digit bits
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds 1-Digit bits
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 20 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

bit 19 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 3
0 = The Data Source 2 signal is disabled for Gate 3

bit 18 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 3
0 = The Data Source 2 inverted signal is disabled for Gate 3

bit 17 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 3
0 = The Data Source 1 signal is disabled for Gate 3

bit 16 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 3
0 = The Data Source 1 inverted signal is disabled for Gate 3

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 2
0 = The Data Source 4 signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 2
0 = The Data Source 3 signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 2
0 = The Data Source 2 signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 2
0 = The Data Source 1 signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 1
0 = The Data Source 4 signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 1
0 = The Data Source 3 signal is disabled for Gate 1

19.1 Comparator Control Registers

TABLE 19-1: COMPARATOR 1 AND 2 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0900	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C2EVT	C1EVT	0000
		15:0	—	—	SIDL	—	—	—	—	CVREFSEL	—	—	—	—	—	—	C2OUT	C1OUT	0000
0910	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
0930	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 19-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	ON	COE	CPOL	—	—	—	CEVT	COUT
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Enable bit
- 1 = Comparator is enabled
- 0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is present on the CxOUT pin
- 0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
- 1 = Comparator output is inverted
- 0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
- 1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
- 0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit

When CPOL = 0:
- 1 = $V_{IN+} > V_{IN-}$
- 0 = $V_{IN+} < V_{IN-}$

When CPOL = 1:
- 1 = $V_{IN+} < V_{IN-}$
- 0 = $V_{IN+} > V_{IN-}$

REGISTER 19-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 AND 2) (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
High-to-low transition only.
If CPOL = 1 (inverted polarity):
Low-to-high transition only.
01 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
Low-to-high transition only.
If CPOL = 1 (inverted polarity):
High-to-low transition only.
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (non-inverting input)
1 = Non-inverting input connects to the internal reference defined by the CVREFSEL bit in the CMSTAT register
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = Inverting input of the comparator connects to the band gap reference voltage
10 = Inverting input of the comparator connects to the CxIND pin
01 = Inverting input of the comparator connects to the CxINC pin
00 = Inverting input of the comparator connects to the CxINB pin

NOTES:

REGISTER 23-2: FICD/AFICD: ICD/DEBUG CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	R/P	R/P	R/P	r-1	r-1
	—	—	—	ICS<1:0>		JTAGEN	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Reserved:** Program as '1'

bit 4-3 **ICS<1:0>:** ICE/ICD Communication Channel Selection bits
- 11 = Communicates on PGEC1/PGED1
- 10 = Communicates on PGEC2/PGED2
- 01 = Communicates on PGEC3/PGED3
- 00 = Not connected

bit 2 **JTAGEN:** JTAG Enable bit
- 1 = JTAG is enabled
- 0 = JTAG is disabled

bit 1-0 **Reserved:** Program as '1'

TABLE 26-12: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ(1)**	**Max**	**Units**	**Comments**
DVR10	VBG	Band Gap Reference Voltage	—	1.2	—	V	
DVR20	VRGOUT	Regulator Output Voltage	—	1.8	—	V	VDD > 1.9V
DVR21	CEFC	External Filter Capacitor Value	4.7	10	—	µF	Series Resistance < 3Ω recommended; < 5Ω required
DVR30	VLVR	Low-Voltage Regulator Output Voltage	0.9	—	1.2	V	RETEN = 1, RETVR (FPOR<2>) = 0

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-13: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ(2)**	**Max**	**Units**
DC18	VHLVD(1)	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0101	3.25	—	3.63	V
			HLVDL<3:0> = 0110	2.95	—	3.30	V
			HLVDL<3:0> = 0111	2.75	—	3.09	V
			HLVDL<3:0> = 1000	2.65	—	2.98	V
			HLVDL<3:0> = 1001	2.45	—	2.80	V
			HLVDL<3:0> = 1010	2.35	—	2.69	V
			HLVDL<3:0> = 1011	2.25	—	2.55	V
			HLVDL<3:0> = 1100	2.15	—	2.44	V
			HLVDL<3:0> = 1101	2.08	—	2.33	V
			HLVDL<3:0> = 1110	2.00	—	2.22	V
DC101	VTHL	HLVD Voltage on LVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.2	—	V

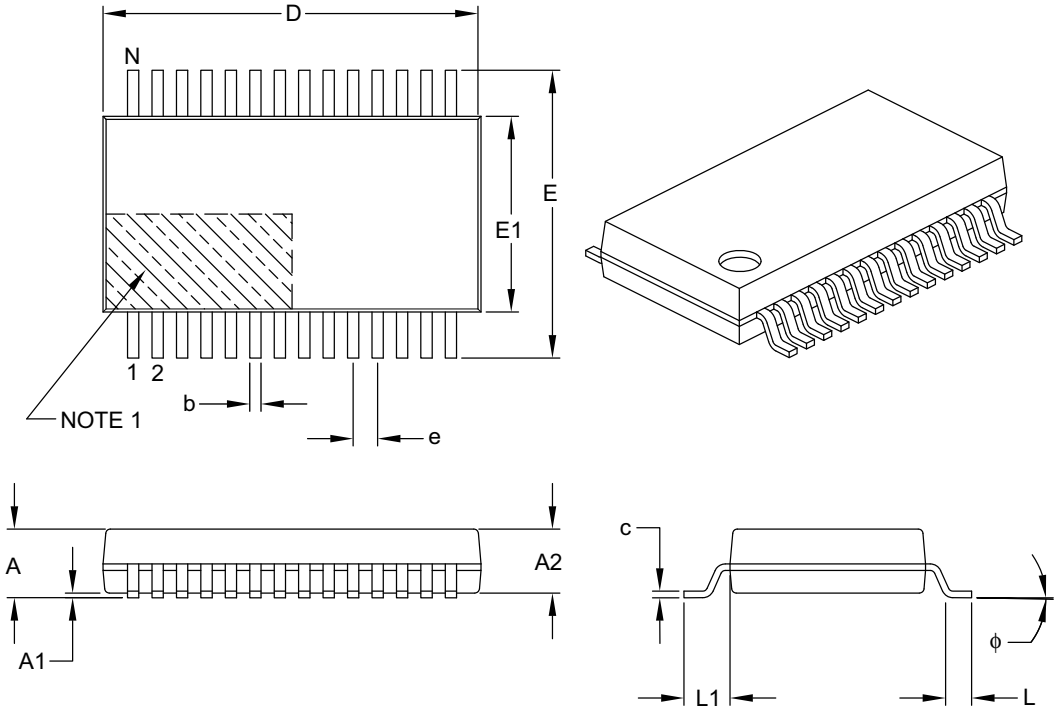
Note 1: Trip points for values of HLVD<3:0>, from '0000' to '0100', are not implemented.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

NOTES:

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

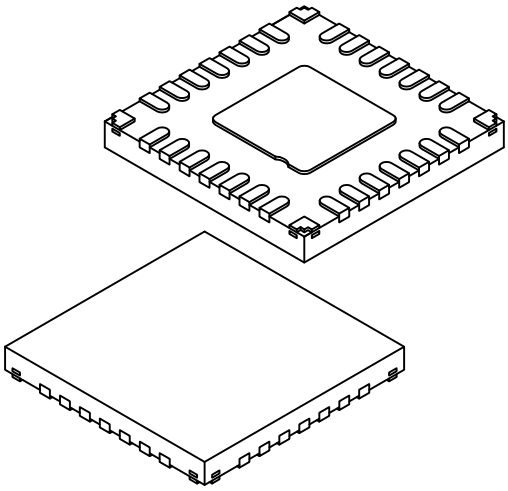
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	-	-	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.80	1.90	2.00
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.80	1.90	2.00
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1	0.40	0.45	0.50
Corner Pad, Metal Free Zone	b2	0.18	0.23	0.28
Terminal Length	L	0.30	0.45	0.50
Terminal-to-Exposed-Pad	K	-	0.60	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

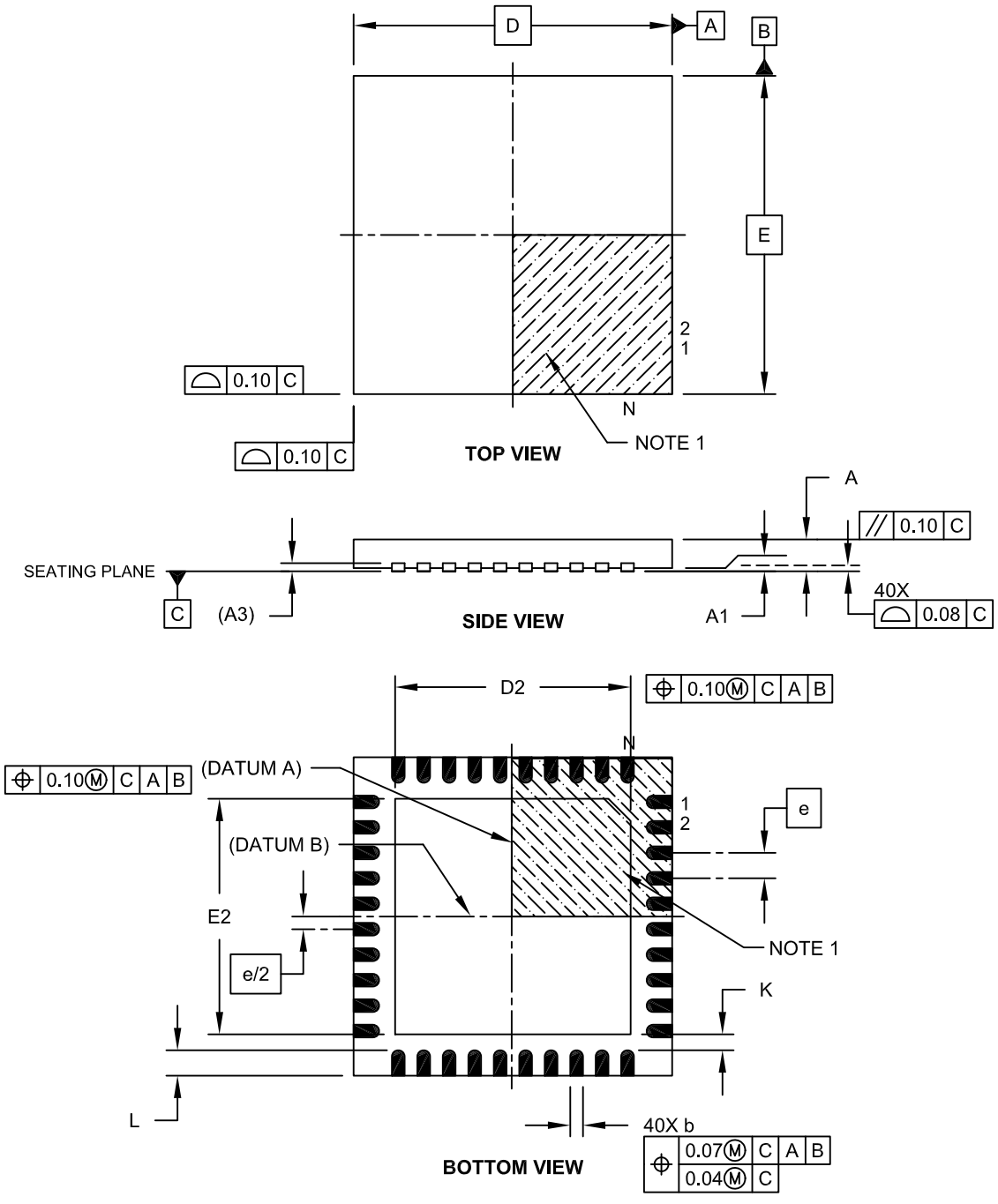
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-333-M6 Rev A Sheet 2 of 2

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-156A Sheet 1 of 2

NOTES: