Microchip Technology - PIC32MM0064GPL028T-I/SS Datasheet

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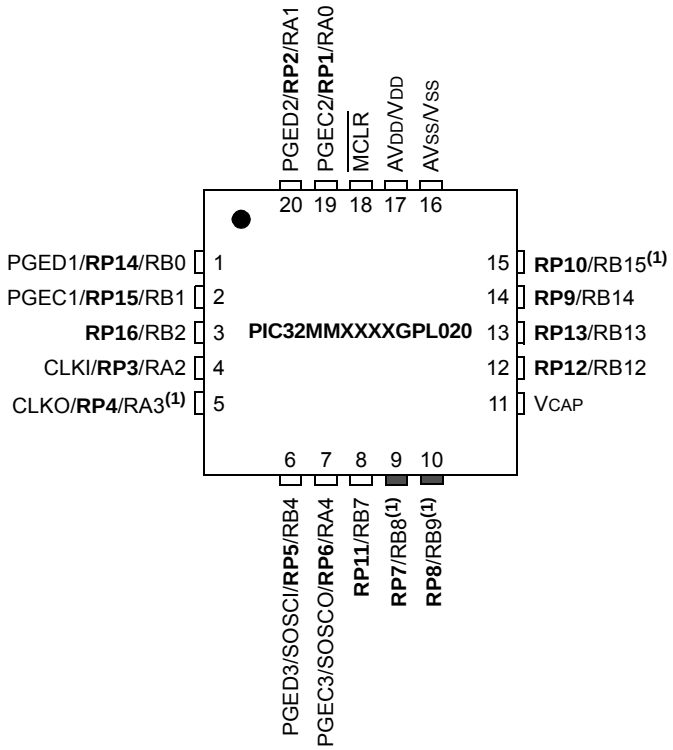
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl028t-i-ss

Pin Diagrams (Continued)

20-Pin QFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN QFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	11	VCAP
2	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	12	TDO/AN7/LVDIN/**RP12**/RB12
3	AN4/**RP16**/RB2	13	TDI/AN8/**RP13**/RB13
4	OSC1/CLKI/AN5/C1INB/**RP3**/OCM1C/RA2	14	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
5	OSC2/CLKO/AN6/C1INA/**RP4**/OCM1D/RA3(1)	15	AN10/REFCLKO/**RP10**/U1RX/$\overline{SS1}$/FSYNC1/INT0/RB15(1)
6	PGED3/SOSCI/**RP5**/RB4	16	AVSS/VSS
7	PGEC3/SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	17	AVDD/VDD
8	**RP11**/RB7	18	$\overline{MCLR}$
9	TCK/**RP7**/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	19	PGEC2/VREF+/AN0/**RP1**/OCM1E/INT3/RA0
10	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)	20	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0064GPL036 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0064GPL036 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0064GPL036 FAMILY BLOCK DIAGRAM

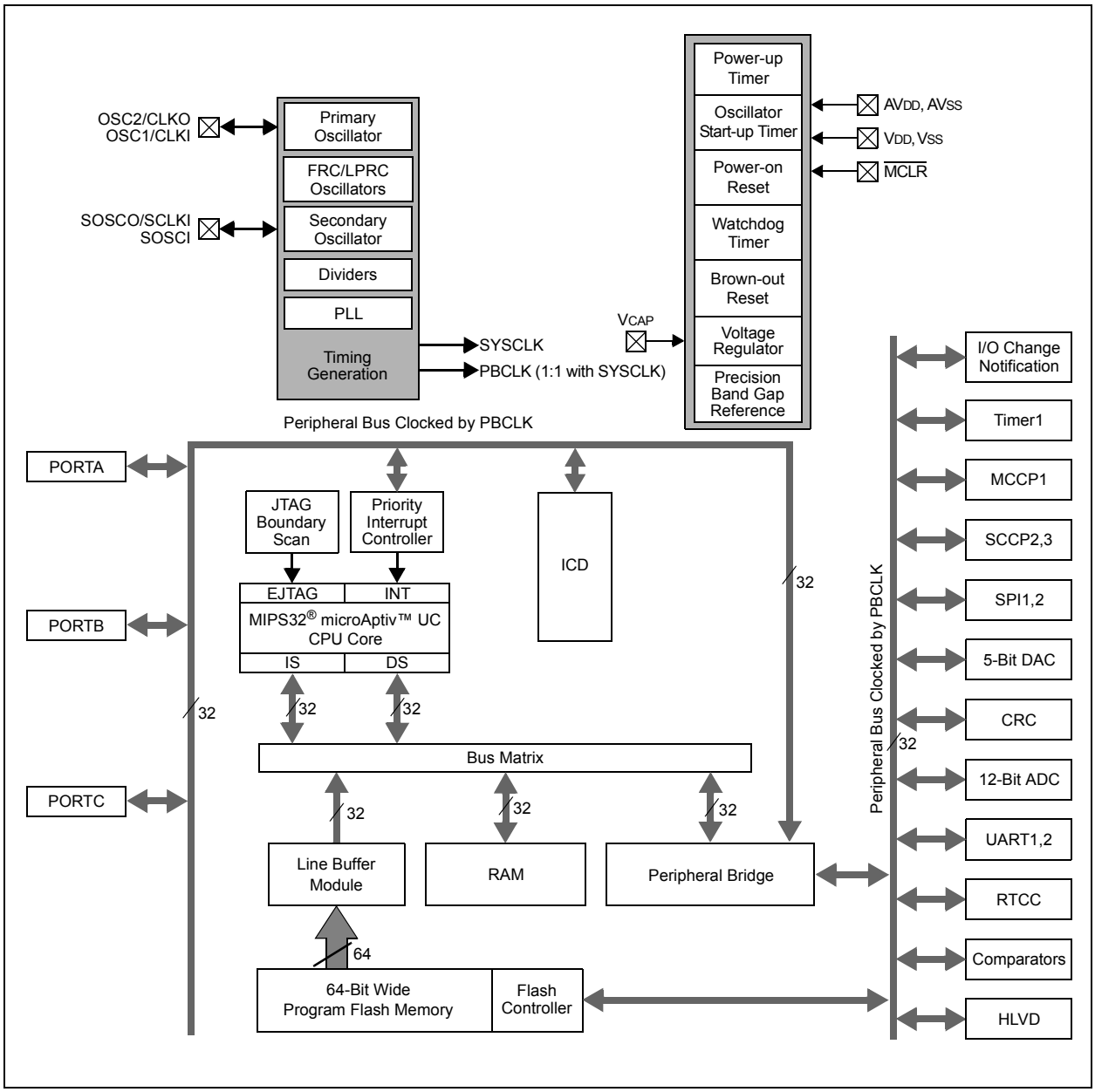


TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
PGEC1	2	5	2	5	36	39	I	ST	ICSP Port 1 programming clock input
PGEC2	19	2	19	22	25	28	I	ST	ICSP Port 2 programming clock input
PGEC3	7	10	12	15	16	16	I	ST	ICSP Port 3 programming clock input
PGED1	1	4	1	4	35	38	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	20	3	18	21	24	27	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	6	9	11	14	15	15	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	7	10	9	12	10	10	I	ST	Real-Time Clock 50/60 Hz clock input
RA0	19	2	27	2	33	36	I/O	ST/DIG	PORTA digital I/O
RA1	20	3	28	3	34	37	I/O	ST/DIG	PORTA digital I/O
RA2	4	7	6	9	7	7	I/O	ST/DIG	PORTA digital I/O
RA3	5	8	7	10	8	8	I/O	ST/DIG	PORTA digital I/O
RA4	7	10	9	12	10	10	I/O	ST/DIG	PORTA digital I/O
RA9	—	—	—	—	11	11	I/O	ST/DIG	PORTA digital I/O
RB0	1	4	1	4	35	38	I/O	ST/DIG	PORTB digital I/O
RB1	2	5	2	5	36	39	I/O	ST/DIG	PORTB digital I/O
RB2	3	6	3	6	1	1	I/O	ST/DIG	PORTB digital I/O
RB3	—	—	4	7	2	2	I/O	ST/DIG	PORTB digital I/O
RB4	6	9	8	11	9	9	I/O	ST/DIG	PORTB digital I/O
RB5	—	—	11	14	15	15	I/O	ST/DIG	PORTB digital I/O
RB6	—	—	12	15	16	16	I/O	ST/DIG	PORTB digital I/O
RB7	8	11	13	16	17	17	I/O	ST/DIG	PORTB digital I/O
RB8	9	12	14	17	18	18	I/O	ST/DIG	PORTB digital I/O
RB9	10	13	15	18	19	20	I/O	ST/DIG	PORTB digital I/O
RB10	—	—	18	21	24	27	I/O	ST/DIG	PORTB digital I/O
RB11	—	—	19	22	25	28	I/O	ST/DIG	PORTB digital I/O
RB12	12	15	20	23	26	29	I/O	ST/DIG	PORTB digital I/O
RB13	13	16	21	24	27	30	I/O	ST/DIG	PORTB digital I/O
RB14	14	17	22	25	28	31	I/O	ST/DIG	PORTB digital I/O
RB15	15	18	23	26	29	32	I/O	ST/DIG	PORTB digital I/O
RC0	—	—	—	—	3	3	I/O	ST/DIG	PORTC digital I/O
RC1	—	—	—	—	4	4	I/O	ST/DIG	PORTC digital I/O
RC2	—	—	—	—	5	5	I/O	ST/DIG	PORTC digital I/O
RC3	—	—	—	—	14	14	I/O	ST/DIG	PORTC digital I/O
RC8	—	—	—	—	20	21	I/O	ST/DIG	PORTC digital I/O
RC9	—	—	16	19	21	22	I/O	ST/DIG	PORTC digital I/O
REFCLKI	10	13	15	18	19	20	I	ST	Reference clock input
REFCLKO	15	18	23	26	29	32	O	DIG	Reference clock output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

NOTES:

3.3 Power Management

The processor core offers a number of power management features, including low-power design, active power management and Power-Down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during Idle periods.

The mechanism for invoking Power-Down mode is implemented through execution of the WAIT instruction. The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MM family makes extensive use of local gated clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The microAptiv UC core has an Enhanced JTAG (EJTAG) interface for use in the software debug. In addition to the standard mode of operation, the microAptiv UC core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the microAptiv UC core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

3.5 MIPS32® microAptiv™ UC Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the microAptiv UC core, which is included on PIC32MM0064GPL036 family devices.

6.0 RESETS

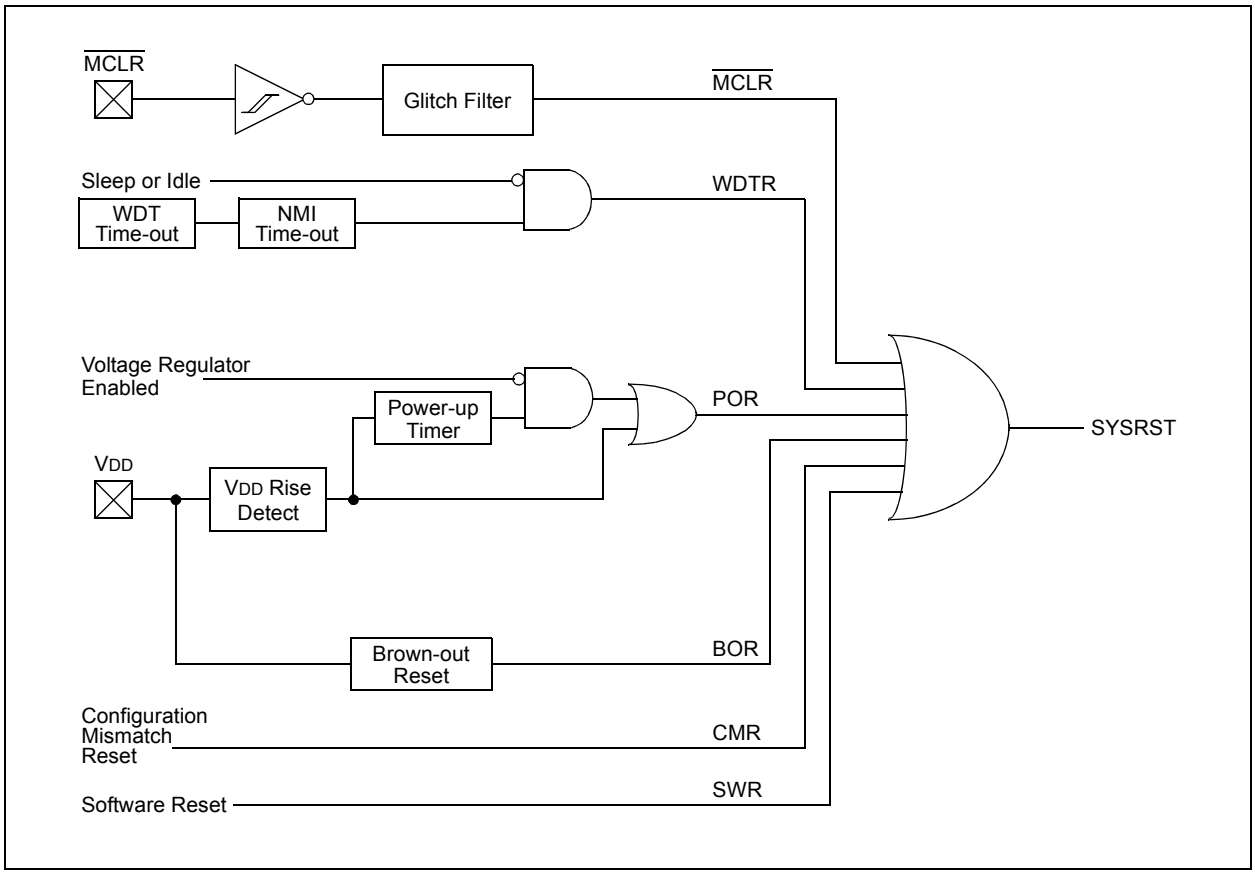
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset Pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



7.1 CPU Exceptions

CPU Coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion of $\overline{\text{MCLR}}$.	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Execution of a RESET instruction.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DINT	—	—
NMI	Non-maskable interrupt.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2	IPL<2:0>	—	Int (0x00)	See Table 7-2
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIB	—	—
AdEL	Load address alignment error.	EBASE + 0x180	EXL	—	ADEL (0x04)	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE + 0x180	EXL	—	IBE (0x06)	_general_exception_handler
DBp	EJTAG breakpoint (execution of SDBBP instruction).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	DBp	—	—	—
Sys	Execution of SYSCALL instruction.	EBASE + 0x180	EXL	—	Sys (0x08)	_general_exception_handler
Bp	Execution of BREAK instruction.	EBASE + 0x180	EXL	—	Bp (0x09)	_general_exception_handler

8.2 Oscillator Control Registers

TABLE 8-1: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name(2)	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			—	—	—	—	—	—	—	—	0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	—	SLPEN	CF	—	SOSCEN	OSWEN	xx0x
2020	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>								0001
		15:0	—	—	—	—	—	—	—	—	PLLICLK	—	—	—	—	—	—	—	0000
20A0	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
20B0	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
21D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	SPDIVRDY	FRCRDY	0000
2200	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the FOSCSEL Configuration bits and the type of Reset.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(3)
- 111 and 110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Reserved
- 010 = Primary Oscillator (POSC) (XT, HS or EC)
- 001 = System PLL (SPLL)
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit(4)
- 1 = Enables Secondary Oscillator
- 0 = Disables Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit(2)
- 1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits
- 0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

2: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) Configuration bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

3: The Reset value for these bits matches the setting of the FNOSC<2:0> (FOSCSEL<2:0>) Configuration bits.

4: The Reset value for this bit matches the setting of the SOSCEN (FOSCSEL<6>) Configuration bit.

TABLE 12-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0260	CCP2RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0270	CCP2RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0280	CCP2BUF	31:16	CCP2 BUFH<15:0>																0000
		15:0	CCP2 BUFL<15:0>																0000
0300	CCP3CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0310	CCP3CON2	31:16	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0320	CCP3CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0330	CCP3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0340	CCP3TMR	31:16	CCP3 TMRH<15:0>																0000
		15:0	CCP3 TMRL<15:0>																0000
0350	CCP3PR	31:16	CCP3 PRH<15:0>																0000
		15:0	CCP3 PRL<15:0>																0000
0360	CCP3RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0370	CCP3RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0380	CCP3BUF	31:16	CCP3 BUFH<15:0>																0000
		15:0	CCP3 BUFL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

13.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

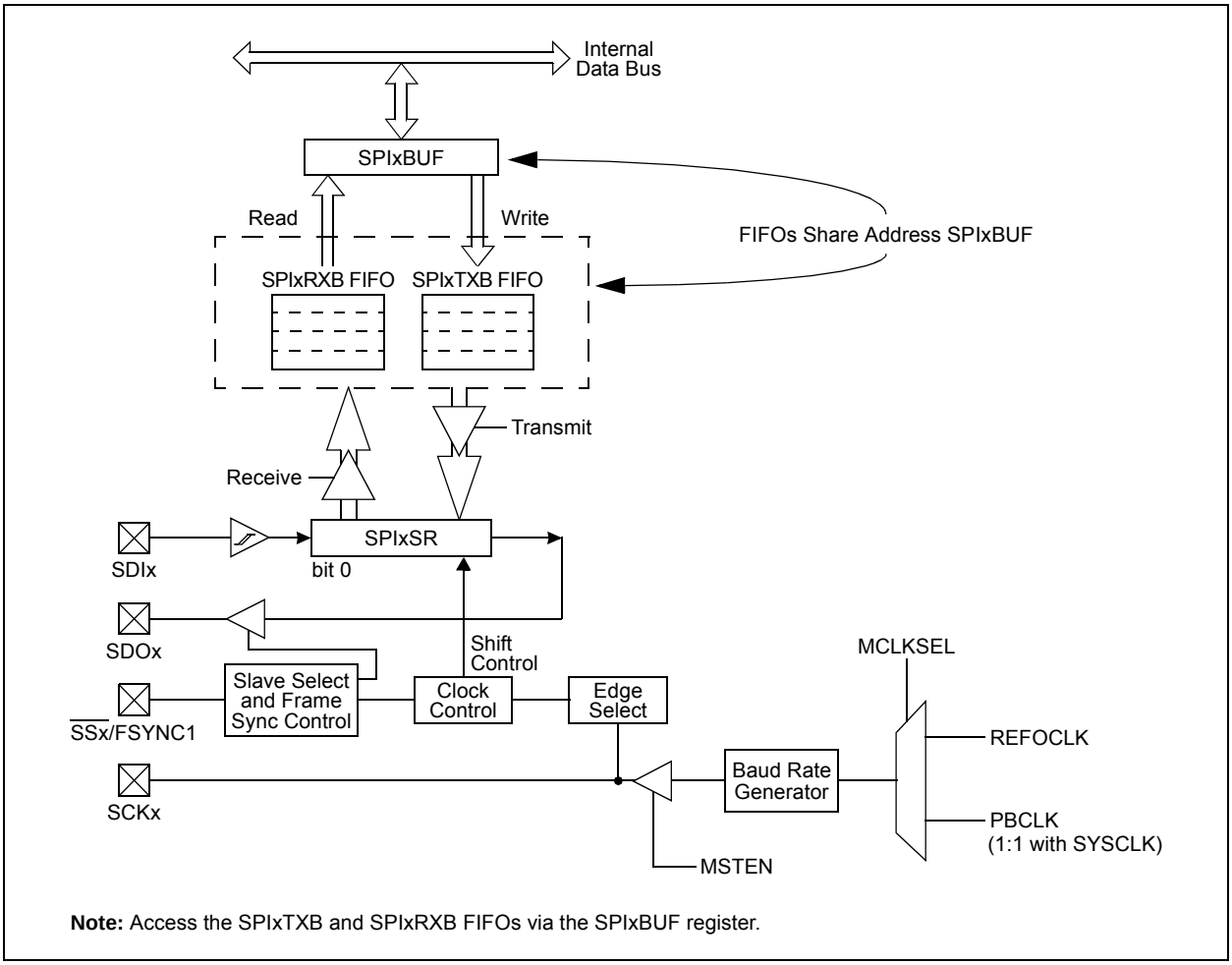
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes Support
- Four Different Clock Formats
- Enhanced Framed SPI Protocol Support
- User-Configurable 8-Bit, 16-Bit and 32-Bit Data Width
- Separate SPI FIFO Buffers for Receive and Transmit:
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable Interrupt Event on Every 8-Bit, 16-Bit and 32-Bit Data Transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol

FIGURE 13-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access the SPIxTXB and SPIxRXB FIFOs via the SPIxBUF register.

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL(1)	—	—	—	—	—	SPIFE	ENHBUF(1)
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO(4)	MODE32	MODE16	SMP	CKE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP(3)	MSTEN	DISSDI(4)	STXISEL<1:0>		SRXISEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
- 1 = Framed SPI support is enabled ($\overline{SSx}$ pin is used as the FSYNC1 input/output)
- 0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ Pin bit (Framed SPI mode only)
- 1 = Frame sync pulse input (Slave mode)
- 0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
- 1 = Frame pulse is active-high
- 0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
- 1 = Slave select SPI support is enabled; the $\overline{SSx}$ pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
- 0 = Slave select SPI support is disabled

bit 27 **FRMSYPW:** Frame Sync Pulse-Width bit
- 1 = Frame sync pulse is one character wide
- 0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits

Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
- 111 = Reserved
- 110 = Reserved
- 101 = Generates a frame sync pulse on every 32 data characters
- 100 = Generates a frame sync pulse on every 16 data characters
- 011 = Generates a frame sync pulse on every 8 data characters
- 010 = Generates a frame sync pulse on every 4 data characters
- 001 = Generates a frame sync pulse on every 2 data characters
- 000 = Generates a frame sync pulse on every data character

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

23.9 Configuration Words and System Registers

TABLE 23-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
17D4	FOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

REGISTER 23-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	r-0	U-0	r-0	r-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EXECADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-y	U-0	r-1	r-1
	—	—	—	—	JTAGEN	—	—	—

Legend:	r = Reserved bit	y = Value set from Configuration bits on Reset
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **Reserved:** Must be written as '0'

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **Reserved:** Must be written as '0'

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits

11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)
•
•
•
00000010 = RAM program space starts at the 2-Kbyte boundary (from 0xA0000800)
00000001 = RAM program space starts at the 1-Kbyte boundary (from 0xA0000400)
00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit

1 = JTAG port is enabled
0 = JTAG port is disabled
The Reset value of this bit is the value of the JTAGEN (FICD<2>) Configuration bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Must be written as '1'

TABLE 23-6: BAND GAP REGISTER MAP

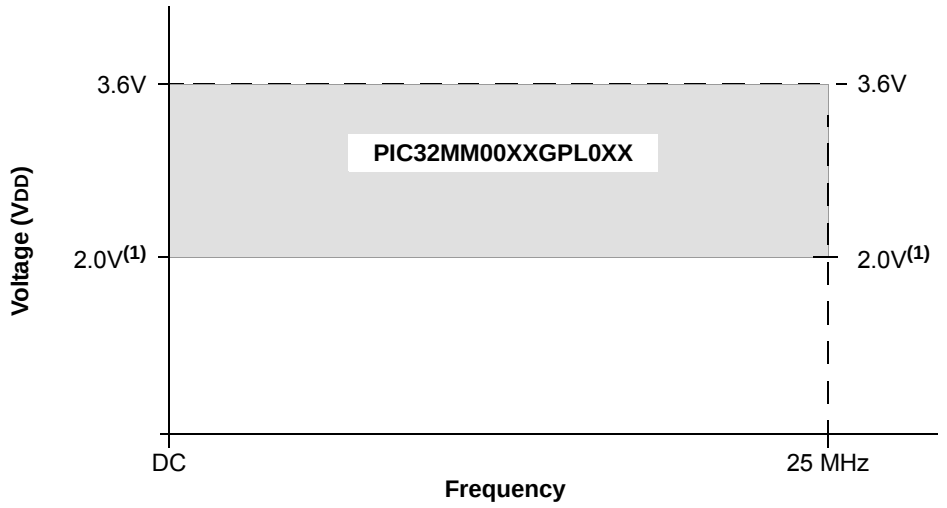
Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

26.1 DC Characteristics

FIGURE 26-1: PIC32MM0064GPL036 FAMILY VOLTAGE-FREQUENCY GRAPH



Note 1: Lower operating boundary is 2.0V or VBOR when BOR is enabled.

TABLE 26-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
PIC32MM00XXGPL0XX:					
Operating Junction Temperature Range	TJ	-40	—	+105	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: PI/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 26-2: PACKAGE THERMAL RESISTANCE(1)

Package	Symbol	Typ	Unit
20-Pin SSOP	θJA	87.3	°C/W
20-Pin QFN	θJA	43.0	°C/W
28-Pin SPDIP	θJA	60.0	°C/W
28-Pin SSOP	θJA	71.0	°C/W
28-Pin SOIC	θJA	69.7	°C/W
28-Pin UQFN	θJA	27.5	°C/W
28-Pin QFN	θJA	20.0	°C/W
36-Pin VQFN	θJA	31.1	°C/W
40-Pin UQFN	θJA	41.0	°C/W

Note 1: Junction to ambient thermal resistance; Theta-JA (θJA) numbers are achieved by package simulations.

26.2 AC Characteristics and Timing Parameters

FIGURE 26-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

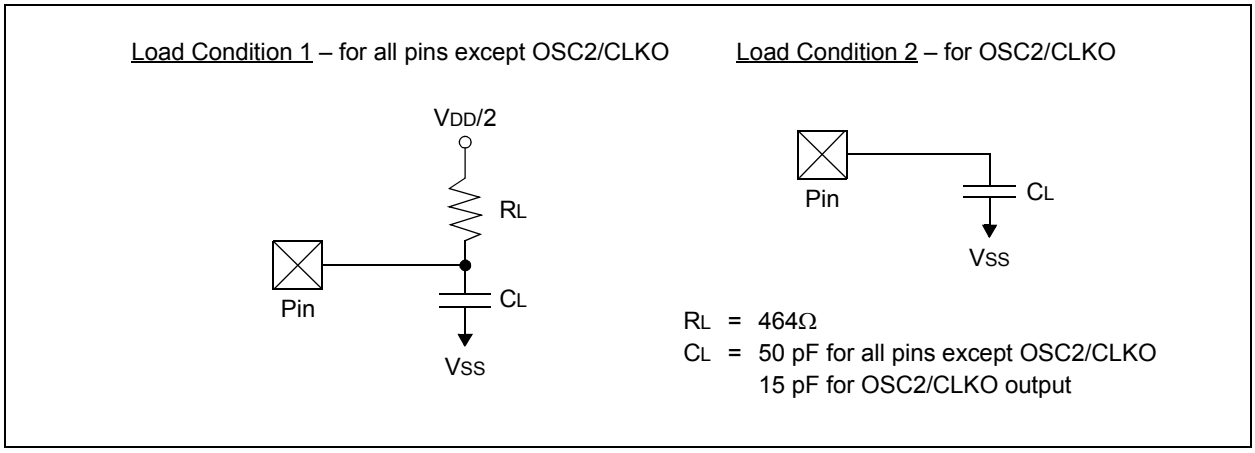


TABLE 26-16: CAPACITIVE LOADING CONDITIONS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
DO50	COSCO	OSC2/CLKO Pin	—	15	pF	In XT and HS modes when external clock is used to drive OSC1/CLKI
DO56	CIO	All I/O Pins and OSC2	—	50	pF	EC mode

FIGURE 26-9: MCCP AND SCCP PWMx MODE TIMING CHARACTERISTICS

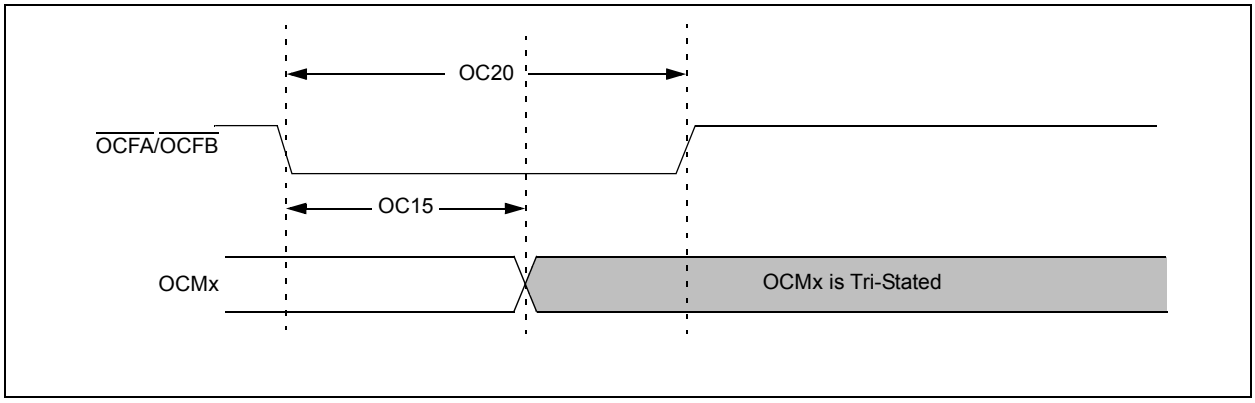


TABLE 26-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
OC15	TFD	Fault Input to PWM I/O Change	—	30	ns
OC20	TFLT	Fault Input Pulse Width	10	—	ns

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-14: EJTAG TIMING CHARACTERISTICS

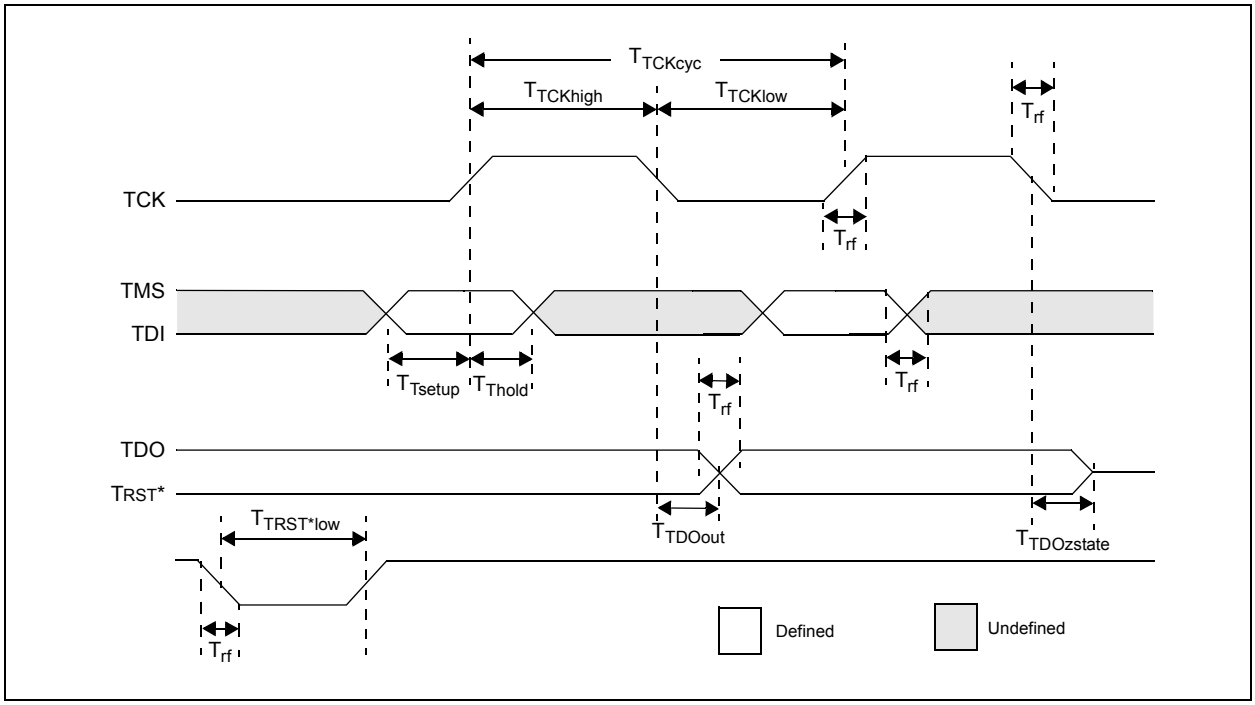


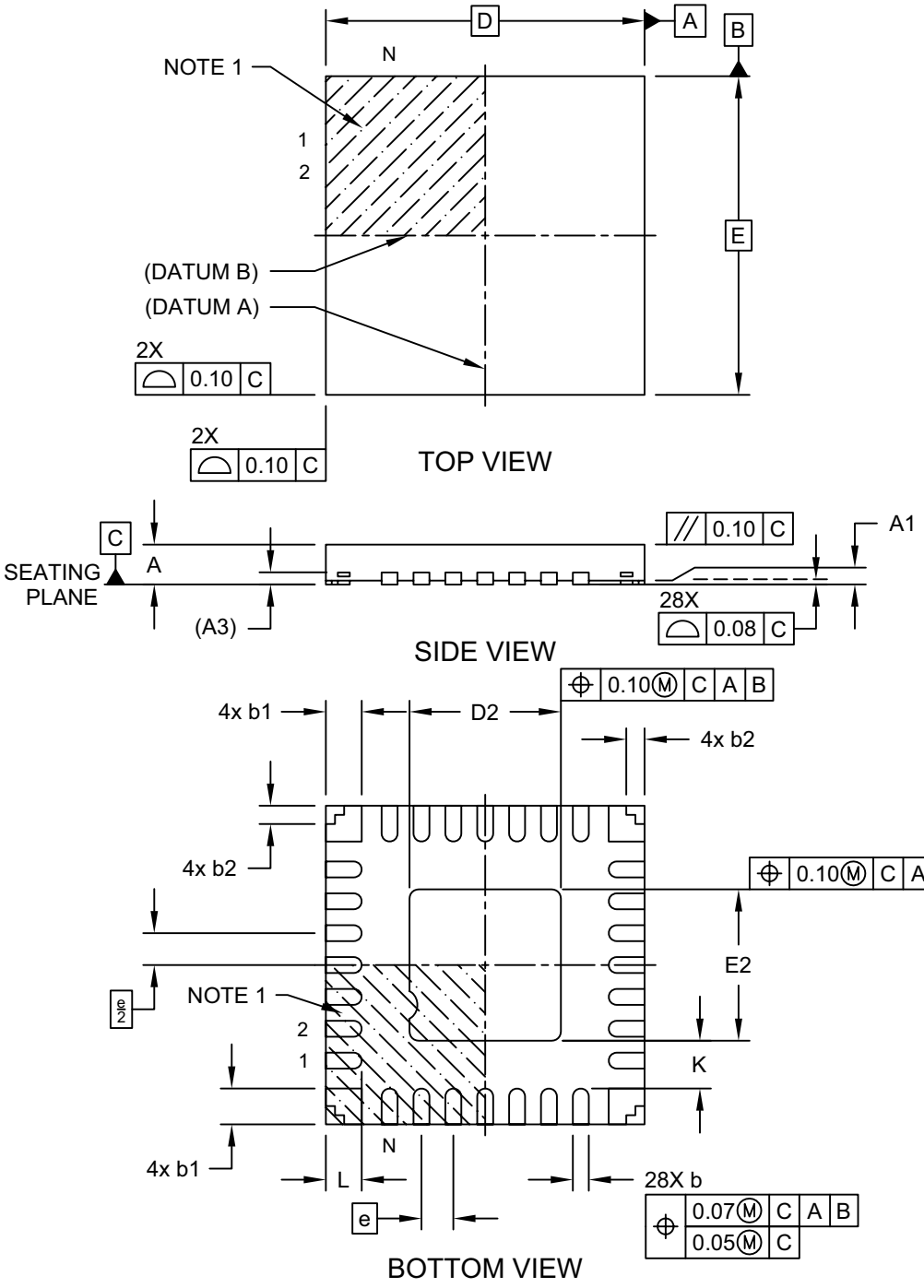
TABLE 26-33: EJTAG TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param. No.	**Symbol**	**Description(1)**	**Min**	**Max**	**Units**	**Conditions**
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	
EJ2	TTCKHIGH	TCK High Time	10	—	ns	
EJ3	TTCKLOW	TCK Low Time	10	—	ns	
EJ4	TTSETUP	TAP Signals Setup Time before Rising TCK	5	—	ns	
EJ5	TTHOLD	TAP Signals Hold Time after Rising TCK	3	—	ns	
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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