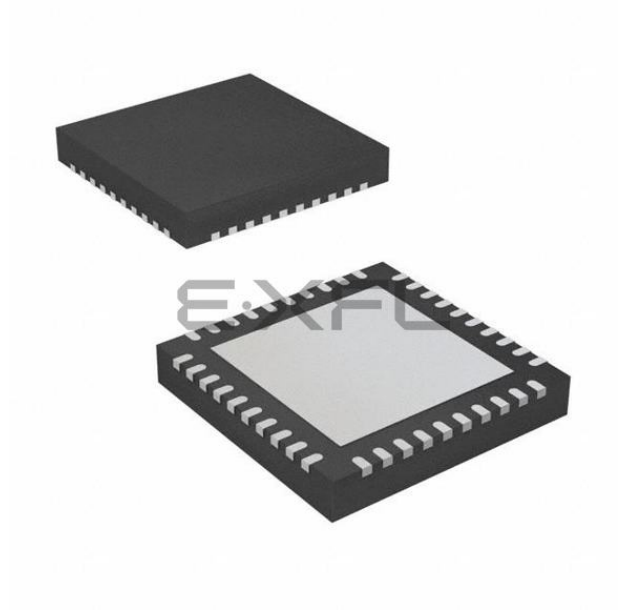
Microchip Technology - PIC32MM0064GPL036-E/MV Datasheet



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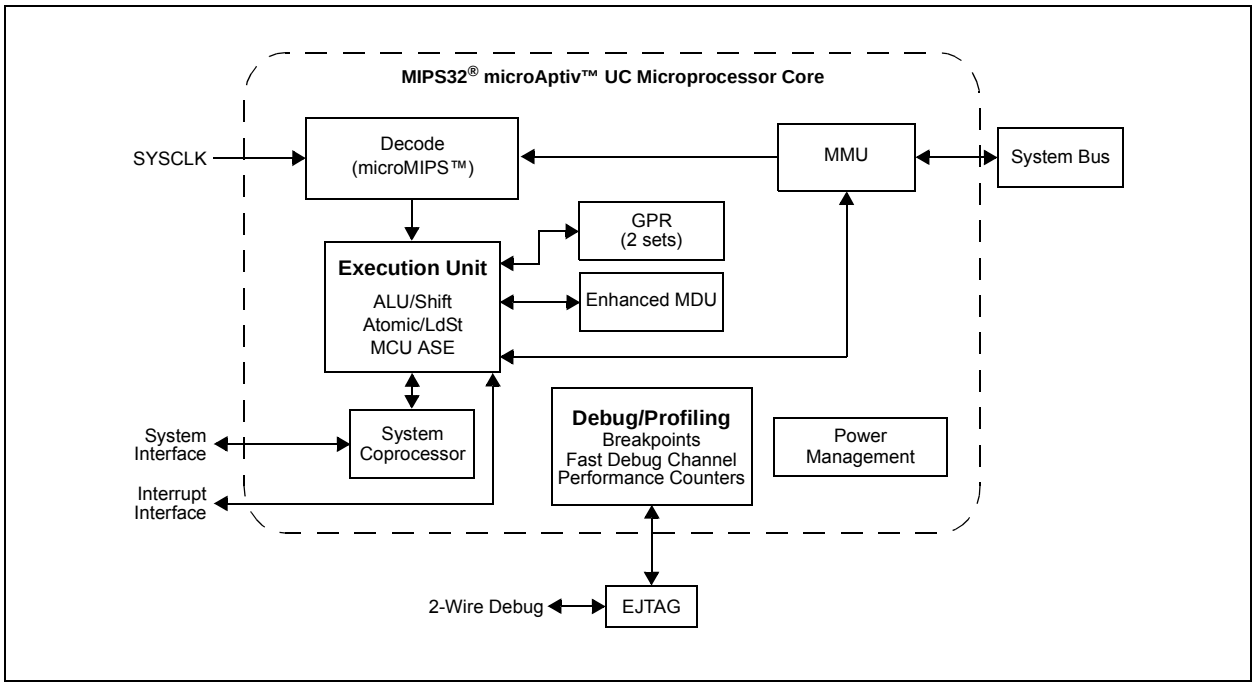
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpl036-e-mv

NOTES:

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

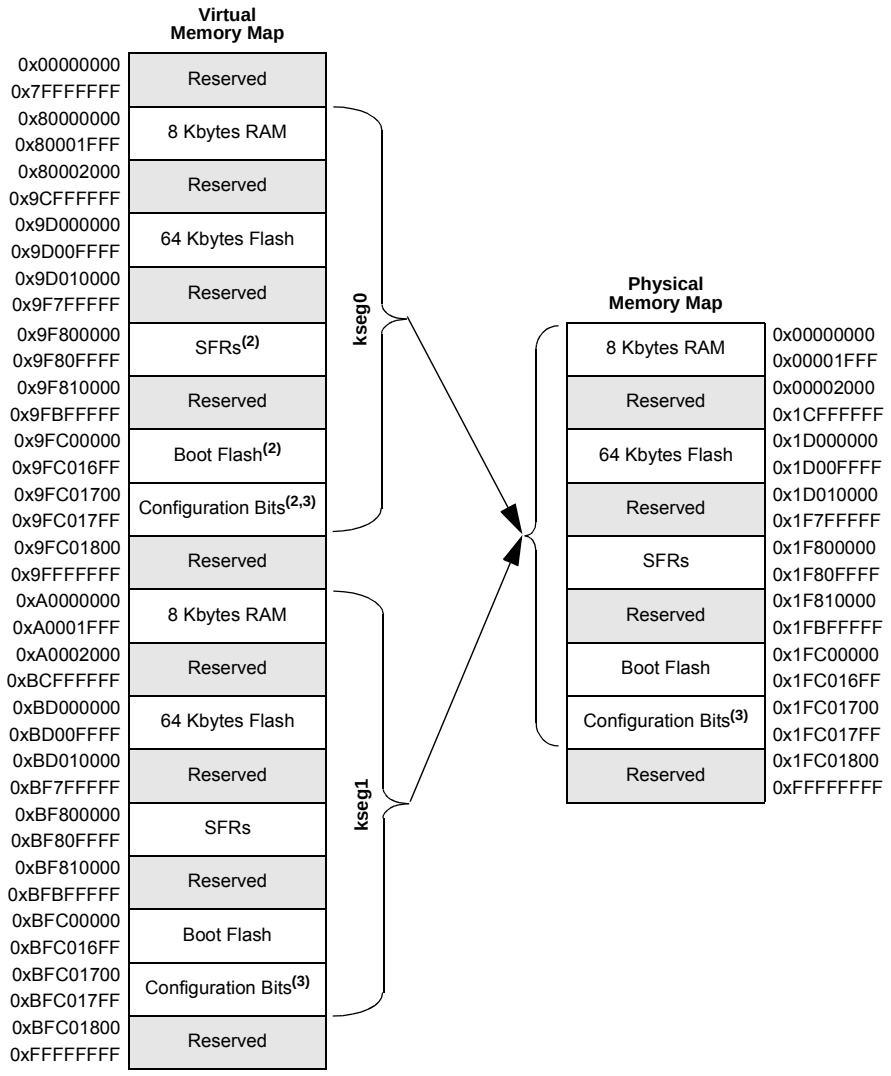
In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information is available by accessing the CP0 registers listed in Table 3-2.

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 64 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.	EBASE + 0x180	CU, EXL	—	CpU (0x0B)	_general_exception_handler
RI	Execution of a reserved instruction.	EBASE + 0x180	EXL	—	RI (0x0A)	_general_exception_handler
Ov	Execution of an arithmetic instruction that overflowed.	EBASE + 0x180	EXL	—	Ov (0x0C)	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE + 0x180	EXL	—	Tr (0x0D)	_general_exception_handler
DDBL	EJTAG data address break (address only) or EJTAG data value break on load (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
DDBS	EJTAG data address break (address only) or EJTAG data value break on store (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
AdES	Store address alignment error.	EBASE + 0x180	EXL	—	ADES (0x05)	_general_exception_handler
DBE	Load or store bus error.	EBASE + 0x180	EXL	—	DBE (0x07)	_general_exception_handler
CBrk	EJTAG complex breakpoint.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIBImpr, DDBLImpr and/or DDBSImpr	—	—
Lowest Priority						

REGISTER 7-5: IFSx: INTERRUPT FLAG STATUS REGISTER x(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS<31:0>:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note 1: This register represents a generic definition of the IFSx register. Refer to Table 7-3 for the exact bit definitions.

REGISTER 7-6: IECx: INTERRUPT ENABLE CONTROL REGISTER x(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC<31-0>:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This register represents a generic definition of the IECx register. Refer to Table 7-3 for the exact bit definitions.

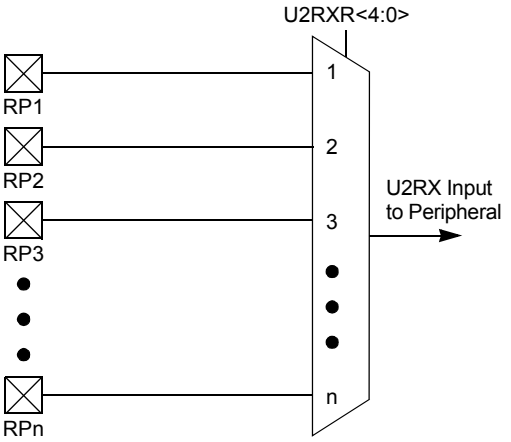
9.8.4 INPUT MAPPING

The RPINRx registers are used to assign the peripheral input to the required remappable pin, RPn (refer to the peripheral inputs and the corresponding RPINRx registers listed in Table 9-2). Each RPINRx register contains sets of 5-bit fields. Programming these bits with the remappable pin number will connect the peripheral to this RPn pin. Example 9-1 and Figure 9-2 illustrate the remappable pin selection for the U2RX input.

EXAMPLE 9-1: UART2 RX INPUT ASSIGNMENT TO RP9/RB14 PIN

```
RPINR9bits.U2RXR = 9; // connect UART2 RX
                      // input to RP9 pin
```

FIGURE 9-2: REMAPPABLE INPUT EXAMPLE FOR U2RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 9-2: INPUT PIN SELECTION

Input Name	Function Name	Register	Function Bits
External Interrupt 4	INT4	RPINR1	INT4R<4:0>
MCCP1 Input Capture	ICM1	RPINR2	ICM1R<4:0>
SCCP2 Input Capture	ICM2	RPINR2	ICM2R<4:0>
SCCP3 Input Capture	ICM3	RPINR3	ICM3R<4:0>
Output Compare Fault A	OCFA	RPINR5	OCFAR<4:0>
Output Compare Fault B	OCFB	RPINR5	OCFBR<4:0>
CCP Clock Input A	TCKIA	RPINR6	TCKIAR<4:0>
CCP Clock Input B	TCKIB	RPINR6	TCKIBR<4:0>
UART2 Receive	U2RX	RPINR9	U2RXR<4:0>
UART2 Clear-to-Send	$\overline{\text{U2CTS}}$	RPINR9	U2CTSR<4:0>
SPI2 Data Input	SDI2	RPINR11	SDI2R<4:0>
SPI2 Clock Input	SCK2IN	RPINR11	SCK2INR<4:0>
SPI2 Slave Select Input	SS2IN	RPINR11	SS2INR<4:0>
CLC Input A	CLCINA	RPINR12	CLCINAR<4:0>
CLC Input B	CLCINB	RPINR12	CLCINBR<4:0>

REGISTER 10-1: T1CON: TIMER1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer1 On bit
1 = Timer1 is enabled
0 = Timer1 is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer1 Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer mode functionality)

bit 11 **TWIP:** Asynchronous Timer1 Write in Progress bit
In Asynchronous Timer1 mode:
1 = Asynchronous write to TMR1 register is in progress
0 = Asynchronous write to TMR1 register is complete
In Synchronous Timer1 mode:
This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK Pin
00 = External clock comes from the Secondary Oscillator (SOSC)

bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

11.0 WATCHDOG TIMER (WDT)

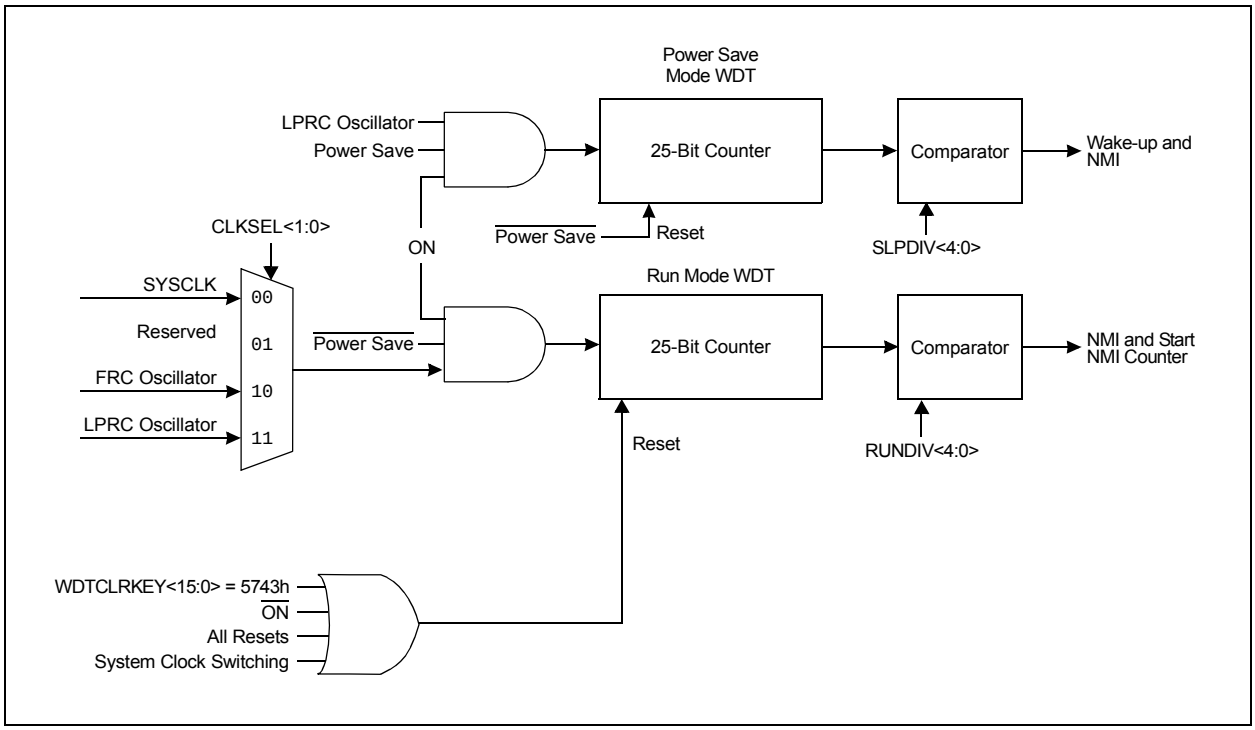
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. "Dual Watchdog Timer"** (DS60001365) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 12-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>		
15:8	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
	PWMRSEN	ASDGM	—	SSDG	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ASDG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **OC<F:A>EN:** Output Enable/Steering Control bits(1)
1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 23-22 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 21 **Unimplemented:** Read as '0'

bit 20-19 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output depends on module operating mode
01 = Time base rollover event (all modes)
00 = Disabled

bit 18-16 **ICS<2:0>:** Input Capture Source Select bits
111 = Reserved
110 = Reserved
101 = CLC2 output
100 = CLC1 output
011 = Reserved
010 = Comparator 2 output
001 = Comparator 1 output
000 = ICMx pin (remappable)

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0 = ASEVT must be cleared in software to resume PWM activity on output pins

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.

REGISTER 12-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER (CONTINUED)

bit 3 **SCEVT:** Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred

bit 2 **ICDIS:** Input Capture Disable bit
1 = Event on input capture pin does not generate a capture event
0 = Event on input capture pin will generate a capture event

bit 1 **ICOV:** Input Capture Buffer Overflow Status bit
1 = The input capture FIFO buffer has overflowed
0 = The input capture FIFO buffer has not overflowed

bit 0 **ICBNE:** Input Capture Buffer Status bit
1 = The input capture buffer has data available
0 = The input capture buffer is empty

Note 1: This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER (CONTINUED)

bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB, is empty
0 = Transmit buffer, SPIxTXB, is not empty
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit buffer is not full
Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.
Enhanced Buffer mode:
Set when the CPU Write Pointer (CWPTR) + 1 = SPI Read Pointer (SRPTR); cleared otherwise.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB, is full
0 = Receive buffer, SPIxRXB, is not full
Standard Buffer mode:
Automatically set in hardware when the SPIx module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise.

REGISTER 14-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to the empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

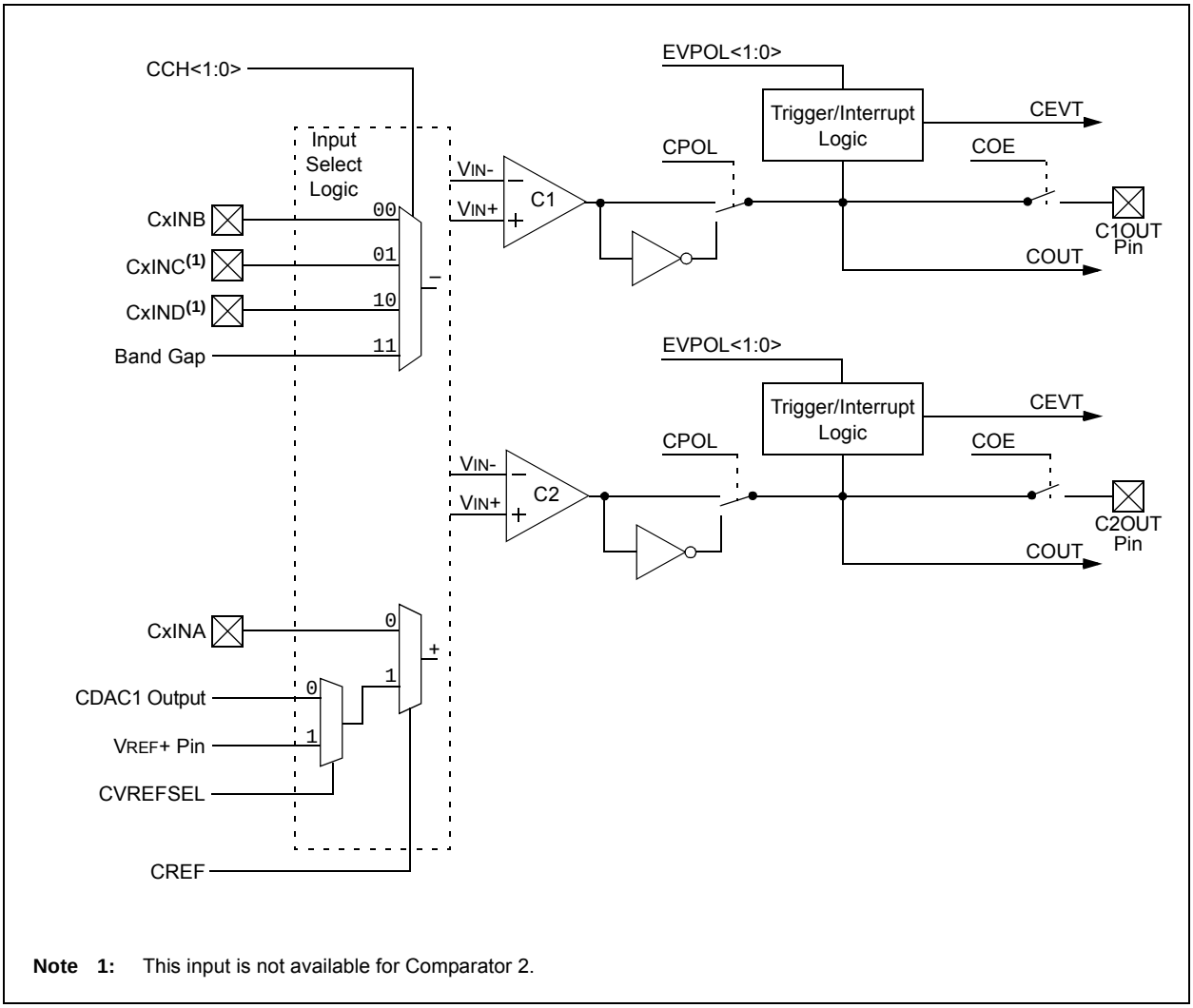
19.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides two dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 19-1. Each comparator has its own control register, CMxCON (Register 19-2), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (Register 19-1).

FIGURE 19-1: DUAL COMPARATOR MODULE BLOCK DIAGRAM



Note 1: This input is not available for Comparator 2.

REGISTER 23-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER (CONTINUED)

bit 6-5 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Watchdog Timer window size is 25%
10 = Watchdog Timer window size is 37.5%
01 = Watchdog Timer window size is 50%
00 = Watchdog Timer window size is 75%

bit 4-0 **SWDTPS<4:0>:** Sleep Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

TABLE 26-6: POWER-DOWN CURRENT (I_{PD})(2)

Parameter No.	Typical(1)	Max	Units	Operating Temperature	VDD	Conditions
DC60	134	198	µA	-40°C	2.0V	Sleep with active main voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) =0)
	136	208	µA	+25°C		
	141	217	µA	+85°C		
	139	209	µA	-40°C	3.3V	
	141	217	µA	+25°C		
	143	231	µA	+85°C		
DC61	4.3	11.7	µA	-40°C	2.0V	Sleep with main voltage regulator in Standby mode (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 0)
	5.1	15.6	µA	+25°C		
	11.4	34.3	µA	+85°C		
	6.1	16.8	µA	-40°C	3.3V	
	6.9	20.1	µA	+25°C		
	12.7	36.0	µA	+85°C		
DC62	2.3	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 1, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	2.7	—	µA	+25°C		
	5.2	—	µA	+85°C		
	2.3	—	µA	-40°C	3.3V	
	2.7	—	µA	+25°C		
	5.4	—	µA	+85°C		
DC63	0.28	—	µA	-40°C	2.0V	Sleep with enabled retention voltage regulator (VREGS (PWRCON<0>) = 0, RETEN (PWRCON<1>) = 1, RETVR (FPOR<2>) = 0)
	0.44	—	µA	+25°C		
	2.52	—	µA	+85°C		
	0.29	—	µA	-40°C	3.3V	
	0.44	—	µA	+25°C		
	2.62	—	µA	+85°C		

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with:

- Oscillator is configured in FRC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 000)
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

FIGURE 26-9: MCCP AND SCCP PWMx MODE TIMING CHARACTERISTICS

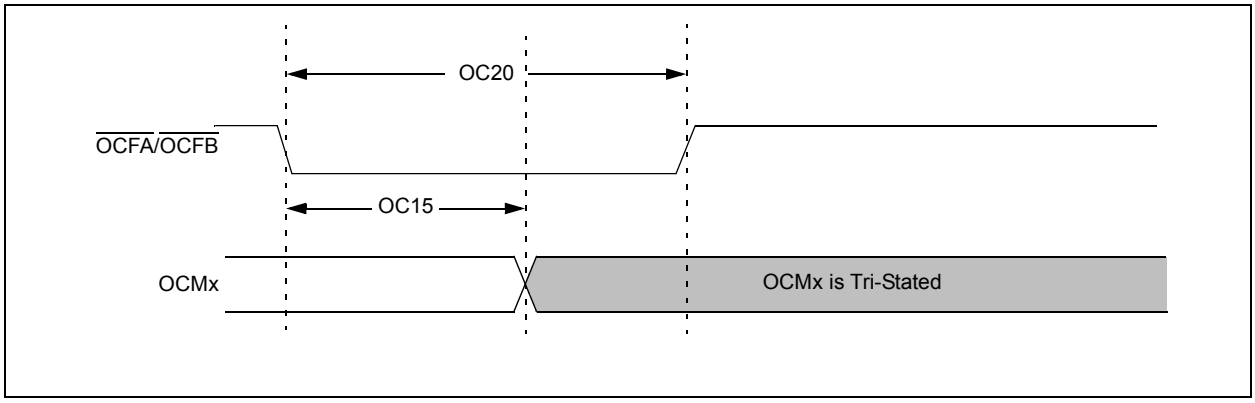


TABLE 26-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
OC15	TFD	Fault Input to PWM I/O Change	—	30	ns
OC20	TFLT	Fault Input Pulse Width	10	—	ns

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 26-30: ADC MODULE INPUTS SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**
Reference Inputs					
AD05	VREFH	Reference Voltage High	AVSS + 1.7	AVDD	V
AD06	VREFL	Reference Voltage Low	AVSS	AVDD – 1.7	V
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	AVDD + 0.3	V
Analog Inputs					
AD10	VINH-VINL	Full-Scale Input Span	VREFL	VREFH	V
AD11	VIN	Absolute Input Voltage	AVSS – 0.3	AVDD + 0.3	V
AD12	VINL	Absolute VINL Input Voltage	AVSS – 0.3	AVDD + 0.3	V
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	2.5K	Ω

TABLE 26-31: ADC ACCURACY AND CONVERSION TIMING REQUIREMENTS FOR 12-BIT MODE(1)

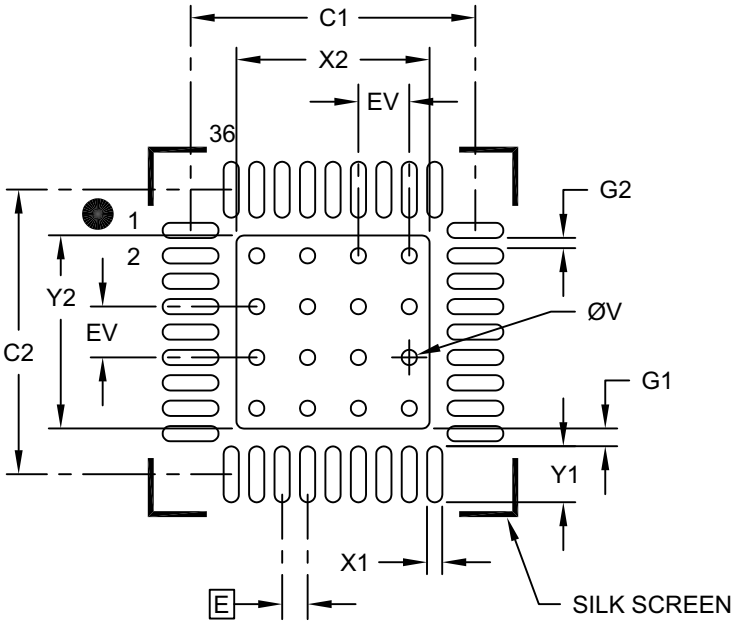
Operating Conditions: VDD = 3.3V, AVSS = VREFL = 0V, AVDD = VREFH = 3.3V, -40°C ≤ TA ≤ +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
ADC Accuracy						
AD20B	Nr	Resolution	—	12	—	bits
AD21B	INL	Integral Nonlinearity	—	±2.5	±3.5	LSb
AD22B	DNL	Differential Nonlinearity	—	±0.75	+1.75/-0.95	LSb
AD23B	GERR	Gain Error	–	+2	+3	LSb
AD24B	EOFF	Offset Error	—	+1	+2	LSb
Clock Parameters						
AD50B	TAD	ADC Clock Period	280	—	—	ns
AD61B	tPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	TAD
Conversion Rate						
AD55B	tCONV	Conversion Time	—	14	—	TAD
AD56B	FCNV	Throughput Rate	—	—	200	ksps

Note 1: Measurements are taken with the external VREF+ and VREF- used as the ADC voltage reference.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x0.9 mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.60	
Contact Pad Spacing	C2		5.60	
Contact Pad Width (X36)	X1			0.30
Contact Pad Length (X36)	Y1			1.10
Contact Pad to Center Pad (X36)	G1	0.35		
Space Between Contact Pads (X32)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2272B-M2

NOTES: