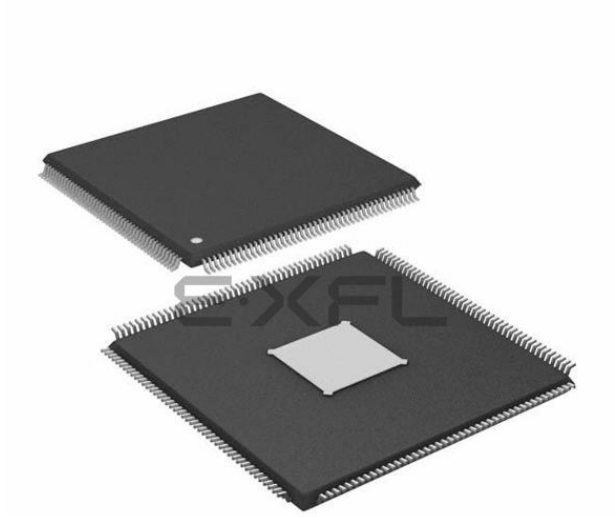
Microchip Technology - PIC32MZ1025DAA176T-I/2J Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

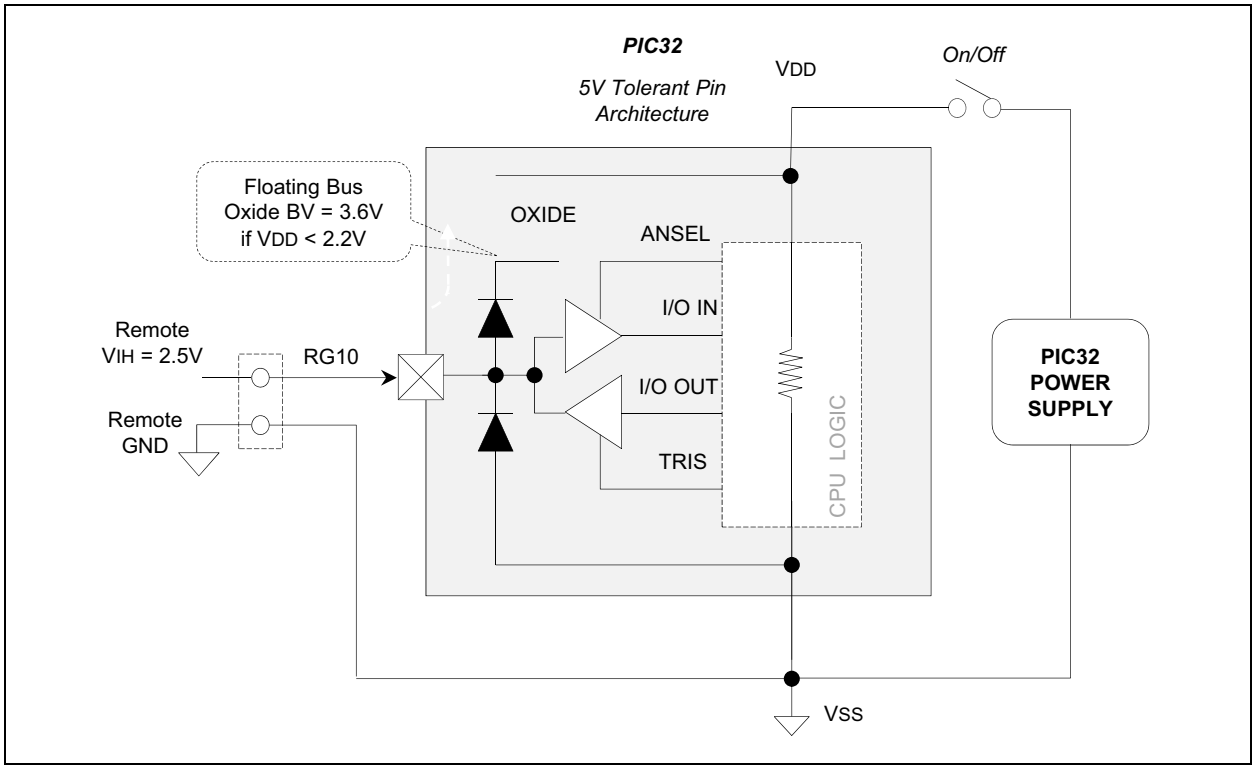
Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1025daa176t-i-2j

2.9.2 5V TOLERANT INPUT PINS

The internal high side diode on 5V tolerant pins are bussed to an internal floating node, rather than being connected to VDD, as shown in Figure 2-7. The voltage on these pins, if VDD < 2.2V, should not exceed 3.2V relative to VSS of the PIC32 device. The voltage of 3.6V or higher will violate the absolute maximum specification and will stress the oxide layer separating the high side floating node, which impacts device reliability.

If a remotely powered “digital-only” signal can be guaranteed to be ≤ 3.2V relative to Vss on the PIC32 device side, a 5V tolerant pin can be used without the need for a digital isolator. This is assuming there is no ground loop issue, that is, the logic ground of the two circuits are not at the same absolute level, and remote logic low input is not less than VSS - 0.3V.

FIGURE 2-7: PIC32 5V TOLERANT PIN ARCHITECTURE EXAMPLE



REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R/W-y
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC(1)
15:8	R-y	R-y	R-1	R-1	R-1	R-1	U-0	R-1
	ISA<1:0>(1)		ULRI	RXI	DSP2P	DSPP	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-1
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as '1' to indicate the presence of the Config4 register

bit 30-23 **Unimplemented:** Read as '0'

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8-bits in width

bit 20-18 **MMAR<2:0>:** microMIPS Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS MCU ASE Implemented bit
1 = MCU™ ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit(1)
1 = microMIPS is used on entrance to an exception vector
0 = MIPS32 ISA is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits(1)
11 = Both MIPS32 and microMIPS are implemented; microMIPS is used when coming out of reset
10 = Both MIPS32 and microMIPS are implemented; MIPS32 ISA used when coming out of reset

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11 **DSP2P:** MIPS DSP ASE Revision 2 Presence bit
1 = DSP Revision 2 is present

bit 10 **DSPP:** MIPS DSP ASE Presence bit
1 = DSP is present

bit 9 **Unimplemented:** Read as '0'

bit 8 **ITL:** Indicates that iFlowtrace hardware is present
1 = The iFlowtrace is implemented in the core

bit 7 **Unimplemented:** Read as '0'

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4 KB page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented (this is old trace logic, which is replaced by iFlowtrace (ITL bit))

Note 1: These bits are set based on the value of the BOOTISA Configuration bit (DEVCFG0<6>).

REGISTER 4-6: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, C	U-0	U-0	U-0	R/W-0, C	R/W-0, C	R/W-0, C	R/W-0, C
	MULTI	—	—	—	CODE<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	INITID<7:0>							
7:0	R-0	R-0	R-0	R-0	U-0	R-0	R-0	R-0
	REGION<3:0>				—	CMD<2:0>		

Legend:	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31 **MULTI:** Multiple Permission Violations Status bit
This bit is cleared by writing a '1'.
1 = Multiple errors have been detected
0 = No multiple errors have been detected

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CODE<3:0>:** Error Code bits
Indicates the type of error that was detected. These bits are cleared by writing a '1'.
1111 = Reserved
1101 = Reserved
•
•
•
0011 = Permission violation
0010 = Reserved
0001 = Reserved
0000 = No error

bit 23-16 **Unimplemented:** Read as '0'

Note: Refer to Table 4-8 for the list of available targets and their descriptions.

REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI reset counter.
1111111111111111-0000000000000001 = Number of SYSCLK cycles before a device Reset occurs(1)
0000000000000000 = No delay between NMI assertion and device Reset event

Note 1: If a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is cleared before this counter reaches '0', no device Reset is asserted. This NMI reset counter is only applicable to these two specific NMI events.

Note:	The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

7.2 Interrupts

The PIC32MZ DA family uses variable offsets for vector spacing. This allows the interrupt vector spacing to be configured according to application needs. A unique interrupt vector offset can be set for each vector using its associated OFFx register.

For details on the Variable Offset feature, refer to **8.5.2 "Variable Offset"** in **Section 8. "Interrupt Controller"** (DS60001108) of the *"PIC32 Family Reference Manual"*.

Table 7-2 provides the Interrupt IRQ, vector and bit location information.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority								
Core Timer Interrupt	_CORE_TIMER_VECTOR	0	OFF000<17:1>	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software Interrupt 0	_CORE_SOFTWARE_0_VECTOR	1	OFF001<17:1>	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software Interrupt 1	_CORE_SOFTWARE_1_VECTOR	2	OFF002<17:1>	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External Interrupt 0	_EXTERNAL_0_VECTOR	3	OFF003<17:1>	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
Timer1	_TIMER_1_VECTOR	4	OFF004<17:1>	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
Input Capture 1 Error	_INPUT_CAPTURE_1_ERROR_VECTOR	5	OFF005<17:1>	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
Input Capture 1	_INPUT_CAPTURE_1_VECTOR	6	OFF006<17:1>	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	Yes
Output Compare 1	_OUTPUT_COMPARE_1_VECTOR	7	OFF007<17:1>	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
External Interrupt 1	_EXTERNAL_1_VECTOR	8	OFF008<17:1>	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
Timer2	_TIMER_2_VECTOR	9	OFF009<17:1>	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
Input Capture 2 Error	_INPUT_CAPTURE_2_ERROR_VECTOR	10	OFF010<17:1>	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	Yes
Input Capture 2	_INPUT_CAPTURE_2_VECTOR	11	OFF011<17:1>	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	Yes
Output Compare 2	_OUTPUT_COMPARE_2_VECTOR	12	OFF012<17:1>	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
External Interrupt 2	_EXTERNAL_2_VECTOR	13	OFF013<17:1>	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Timer3	_TIMER_3_VECTOR	14	OFF014<17:1>	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
Input Capture 3 Error	_INPUT_CAPTURE_3_ERROR_VECTOR	15	OFF015<17:1>	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	Yes
Input Capture 3	_INPUT_CAPTURE_3_VECTOR	16	OFF016<17:1>	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
Output Compare 3	_OUTPUT_COMPARE_3_VECTOR	17	OFF017<17:1>	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
External Interrupt 3	_EXTERNAL_3_VECTOR	18	OFF018<17:1>	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer4	_TIMER_4_VECTOR	19	OFF019<17:1>	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
Input Capture 4 Error	_INPUT_CAPTURE_4_ERROR_VECTOR	20	OFF020<17:1>	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
Input Capture 4	_INPUT_CAPTURE_4_VECTOR	21	OFF021<17:1>	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes
Output Compare 4	_OUTPUT_COMPARE_4_VECTOR	22	OFF022<17:1>	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	No

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

TABLE 8-1: SYSTEM AND PERIPHERAL CLOCK DISTRIBUTION

Peripheral		Clock Source																
	FRC	LPRC	SOSC	SYSCLK	USBCLK	MPLL	PBCLK1(1)	PBCLK2	PBCLK3	PBCLK4	PBCLK5	PBCLK6	PBCLK7	REFCLKO1	REFCLKO2	REFCLKO3	REFCLKO4	REFOCLK5
CPU													X					
WDT		X		X			X(3)											
DMT				X			X(3)						X					
GLCD				X(3)														X(6)
GPU				X														
DDR2C				X(3)		X												
SDHC											X(3)						X	
Flash	X(2)			X(2)							X(2)							
ADC	X			X					X(3)							X		
Comparator									X(3)									
CTMU									X(3)									
Crypto											X(3)							
RNG											X(3)							
USB					X						X(3)							
USBCR(7)											X(3)							
CAN											X(3)							
Ethernet											X(3)							
PMP								X(3)										
I^2C								X(3)										
UART								X(3)										
RTCC		X	X									X(3)						
EBI				X														
SQI											X(3)				X			
SPI								X						X				
Timers		X	X(4)						X									
Output Compare									X									
Input Capture									X									
Ports										X(3)								
DMA				X														
Interrupts				X														
Prefetch				X														
OSC2 Pin							X(5)											
DSCTRL(8)				X								X						
HLVD							X(3)											

Note 1: PBCLK1 is used by system modules and cannot be turned off.

2: SYSCLK/PBCLK5 is used to fetch data from/to the Flash Controller, while the FRC clock is used for programming.

3: Special Function Register (SFR) access only.

4: Timer1 only.

5: PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.

6: REFCLKO5 (divided version of SPLL clock) is used for the Pixel Clock.

7: USBCR is the Clock/Reset Control block for the USB.

8: DSCTRL is the Deep Sleep Control Block.

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1380	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1390	PB6DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8803
13A0	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
13C0	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0000
13D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

REGISTER 8-5: REFOxTRIM: REFERENCE OSCILLATOR TRIM REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value
111111110 = 510/512 divisor added to RODIV value
•
•
•
100000000 = 256/512 divisor added to RODIV value
•
•
•
000000010 = 2/512 divisor added to RODIV value
000000001 = 1/512 divisor added to RODIV value
000000000 = 0 divisor added to RODIV value

bit 22-0 **Unimplemented:** Read as '0'

Note 1: While the ON bit (REFOxCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

2: Do not write to this register when the ON bit (REFOxCON<15>) is not equal to the ACTIVE bit (REFOxCON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFOxCON<30:16>) = 0.

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R/W-1, HS
	—	—	—	—	—	USBIF	USBRF	USBWKUP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	r-1	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	USB IDOVEN	USB IDVAL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **USBIF:** USB General Interrupt Flag bit
1 = An event on the USB Bus has occurred
0 = No interrupt from USB module or interrupts have not been enabled

bit 25 **USBRF:** USB Resume Flag bit
1 = Resume from Suspend state. Device wake-up activity can be started.
0 = No Resume activity detected during Suspend, or not in Suspend state

bit 24 **USBWKUP:** USB Activity Status bit
1 = Connect, disconnect, or other activity on USB detected since last cleared
0 = No activity detected on USB

Note: This bit should be cleared just prior to entering sleep, but it should be checked that no activity has already occurred on USB before actually entering sleep.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **Reserved:** Read as '1'

bit 14-10 **Unimplemented:** Read as '0'

bit 9 **USBIDOVEN:** USB ID Override Enable bit
1 = Enable use of USBIDVAL bit
0 = Disable use of USBIDVAL and instead use the PHY value

bit 8 **USBIDVAL:** USB ID Value bit
1 = ID override value is 1
0 = ID override value is 0

bit 7 **PHYIDEN:** PHY ID Monitoring Enable bit
1 = Enable monitoring of the ID bit from the USB PHY
0 = Disable monitoring of the ID bit from the USB PHY

bit 6 **VBUSMONEN:** VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in VBUS Valid range (between 4.4V and 4.75V)
0 = Disable monitoring for VBUS in VBUS Valid range

bit 5 **ASVALMONEN:** A-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for A-device (between 0.8V and 2.0V)
0 = Disable monitoring for VBUS in Session Valid range for A-device

bit 4 **BSVALMONEN:** B-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for B-device (between 0.8V and 4.0V)
0 = Disable monitoring for VBUS in Session Valid range for B-device

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER (CONTINUED)

bit 3 **SENDMONEN:** Session End VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session End range (between 0.2V and 0.8V)
0 = Disable monitoring for VBUS in Session End range

bit 2 **USBIE:** USB General Interrupt Enable bit
1 = Enables general interrupt from USB module
0 = Disables general interrupt from USB module

bit 1 **USBRIE:** USB Resume Interrupt Enable bit
1 = Enable remote resume from suspend Interrupt
0 = Disable interrupt to a Remote Devices USB resume signaling

bit 0 **USBWKUPEN:** USB Activity Detection Interrupt Enable bit
1 = Enable interrupt for detection of activity on USB bus in Sleep mode
0 = Disable interrupt for detection of activity on USB bus in Sleep mode

21.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 21-1: SPI/I^2S MODULE BLOCK DIAGRAM

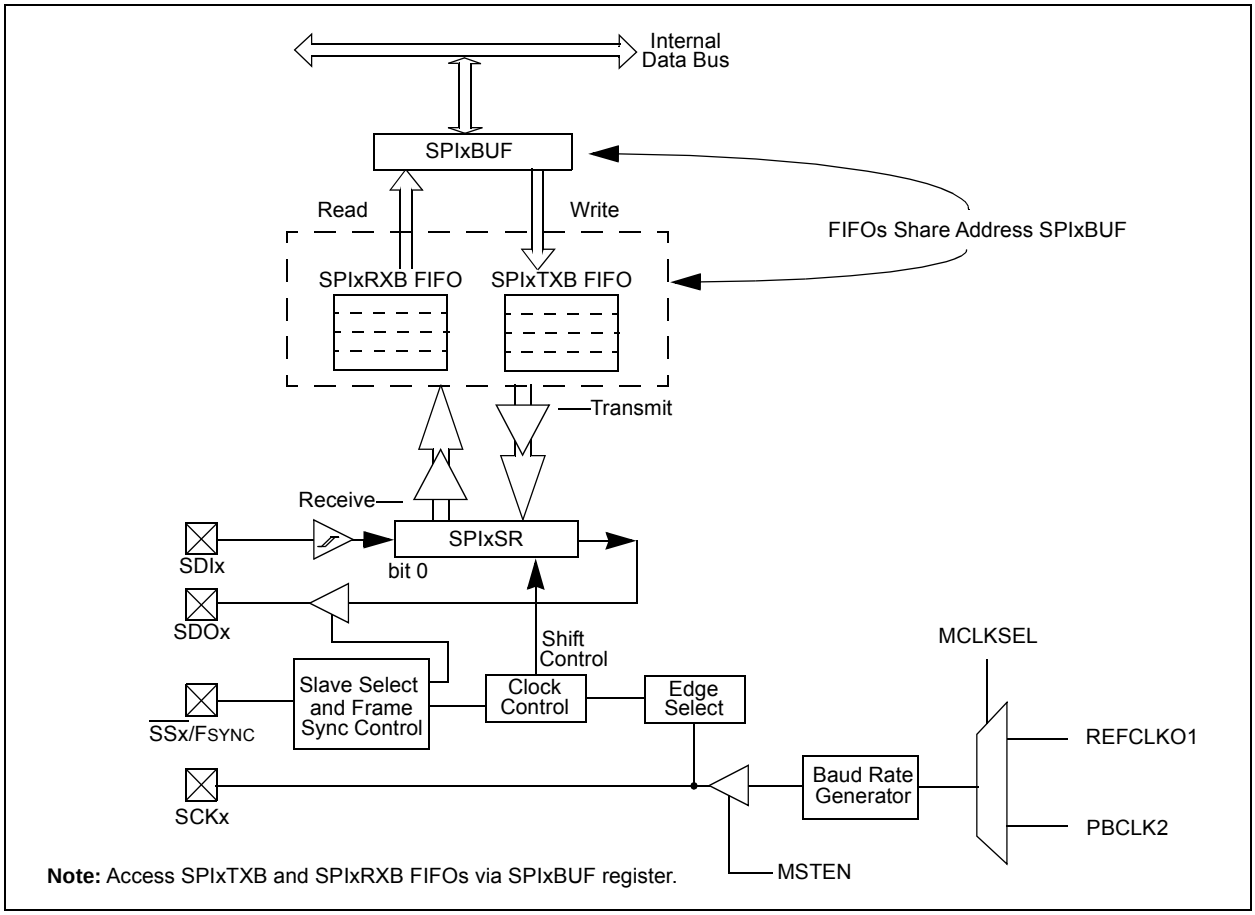


FIGURE 27-2: FORMAT OF BD_CTRL

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
23-16	—	SA_FETCH_EN	—	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
15-8	BD_BUFLEN<15:8>							
7-0	BD_BUFLEN<7:0>							

bit 31 **DESC_EN**: Descriptor Enable
1 = The descriptor is owned by hardware. After processing the BD, hardware resets this bit to '0'.
0 = The descriptor is owned by software

bit 30 **Unimplemented:** Must be written as '0'

bit 29-27 **CRY_MODE<2:0>:** Crypto Mode
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = CEK operation
010 = KEK operation
001 = Preboot authentication
000 = Normal operation

bit 22 **SA_FETCH_EN:** Fetch Security Association From External Memory
1 = Fetch SA from the SA pointer. This bit needs to be set to '1' for every new packet.
0 = Use current fetched SA or the internal SA

bit 21-20 **Unimplemented:** Must be written as '0'

bit 19 **LAST_BD:** Last Buffer Descriptors
1 = Last Buffer Descriptor in the chain
0 = More Buffer Descriptors in the chain
After the last BD, the CEBDADDR goes to the base address in CEBDPADDR.

bit 18 **LIFM:** Last In Frame
In case of Receive Packets (from H/W-> Host), this field is filled by the Hardware to indicate whether the packet goes across multiple buffer descriptors. In case of transmit packets (from Host -> H/W), this field indicates whether this BD is the last in the frame.

bit 17 **PKT_INT_EN:** Packet Interrupt Enable
Generate an interrupt after processing the current buffer descriptor, if it is the end of the packet.

bit 16 **CBD_INT_EN:** CBD Interrupt Enable
Generate an interrupt after processing the current buffer descriptor.

bit 15-0 **BD_BUFLEN<15:0>:** Buffer Descriptor Length
This field contains the length of the buffer and is updated with the actual length filled by the receiver.

NOTES:

REGISTER 35-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current
10 = 10 times base current
01 = Base current level
00 = 1000 times base current(4)

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<2:0> bits must be set to '1110' to select the C2OUT pin.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 44-20) in **Section 44.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

REGISTER 38-30: DDRPHYDLLCTRL: DDR PHY TRIM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	r-x	r-x
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DDRDLLTRIM<7:0>							

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-10 **Unimplemented:** Read as '0'

bit 9-8 **Reserved:** Write as '0'

bit 7-0 **DDRDLLTRIM<7:0>:** Trim Setting bits

These bits control the Trim settings for adjusting the output time of the bank address and control signals with respect to data signals (DQ/DQS). The recommended value is 0x1.

REGISTER 38-31: DDRPHYCLKDLY: DDR CLOCK DELTA DELAY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0	R-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	SCLUBPASS(1)	SCLLBPASS(1)	—	CLKDLYDELTA<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0

bit 5 **SCLUBPASS:** Self Calibration Logic Upper Data Byte Status bit (1)

1 = Self calibration logic for upper data byte is passed

0 = Self calibration logic for upper data byte is failed

bit 4 **SCLLBPASS:** Self Calibration Logic Lower Data Byte Status bit(1)

1 = Self calibration logic for lower data byte is passed

0 = Self calibration logic for lower data byte is failed

bit 3 **Unimplemented:** Read as '0'

REGISTER 39-1: SDHCBLKCON: SDHC BLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<15:8>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<7:0>(1)							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	BSIZE<9:8>(2)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BSIZE<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **BCOUNT<31:0>:** Blocks Count for Current Transfer bits(1)

These bits represent the number of blocks. The software sets this value between 1 and 65,535 blocks and the SDHC decrements the count after each block transfer and stops when the count reaches zero.
0xFFFF = 65,535 blocks
0x0002 = 2 blocks
0x0001 = 1 block
0x0000 = Stop count Blocks Count for Current Transfer bits

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **BSIZE<9:0>:** Transfer Block Size bits(2)

These bits specify the block size of the data transfer for CMD17, CMD18, CMD24, CMD25, and CMD53.
0x200 = 512 bytes
0x1FF = 511 bytes
•
•
•
0x002 = 2 bytes
0x001 = 1 byte
0x000 = No data transfer

Note 1: These bits are only used when the BCEN bit (SDHCMODE<1>) is set to '1' and is valid only for multiple block transfers. The BCOUNT<15:0> bits need not be set if the BSIZE bit (SDHCMODE<5>) is set to '0'.

2: These bits can only be accessed when no transactions are in progress. Read operations during transfers will return an invalid value and write operations to these bits will be ignored.

TABLE 40-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits															All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
02A8	DSGPR27	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02AC	DSGPR28	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02B0	DSGPR29	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02B4	DSGPR30	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02B8	DSGPR31	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02BC	DSGPR32	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice.

REGISTER 41-9: CFGCON: CONFIGURATION CONTROL REGISTER (CONTINUED)

bit 7 **IOANCPEN:** I/O Analog Charge Pump Enable bit
1 = Charge pumps are enabled
0 = Charge pumps are disabled

Note 1: For proper analog operation at VDD is less than 2.5V, the AICPMPEN bit (ADCCON1<12>) must be = 1 and the IOANCPEN bit must be set to '1'; however, the charge pumps will consume additional current. These bits should not be set if VDD is greater than 2.5V.

2: ADC throughput rate performance is reduced as defined in the table below if ADCCON1<AICPMPEN> = 1 and CFGCON<IOANCPEN> = 1.

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **ECCCON<1:0>:** Flash ECC Configuration bits
11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 3 **JTAGEN:** JTAG Port Enable bit(2)
1 = Enable the JTAG port
0 = Disable the JTAG port

bit 2 **TROEN:** Trace Output Enable bit
1 = Enable trace outputs and start trace clock (trace probe must be present)
0 = Disable trace outputs and stop trace clock

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG
1 = 2-wire JTAG protocol uses TDO
0 = 2-wire JTAG protocol does not use TDO

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: The JTAGEN bit is only available at run-time when the JTAGEN (DEVCFG0<2>) fuse bit is set at start-up.

FIGURE 44-5: EXTERNAL RESET TIMING CHARACTERISTICS

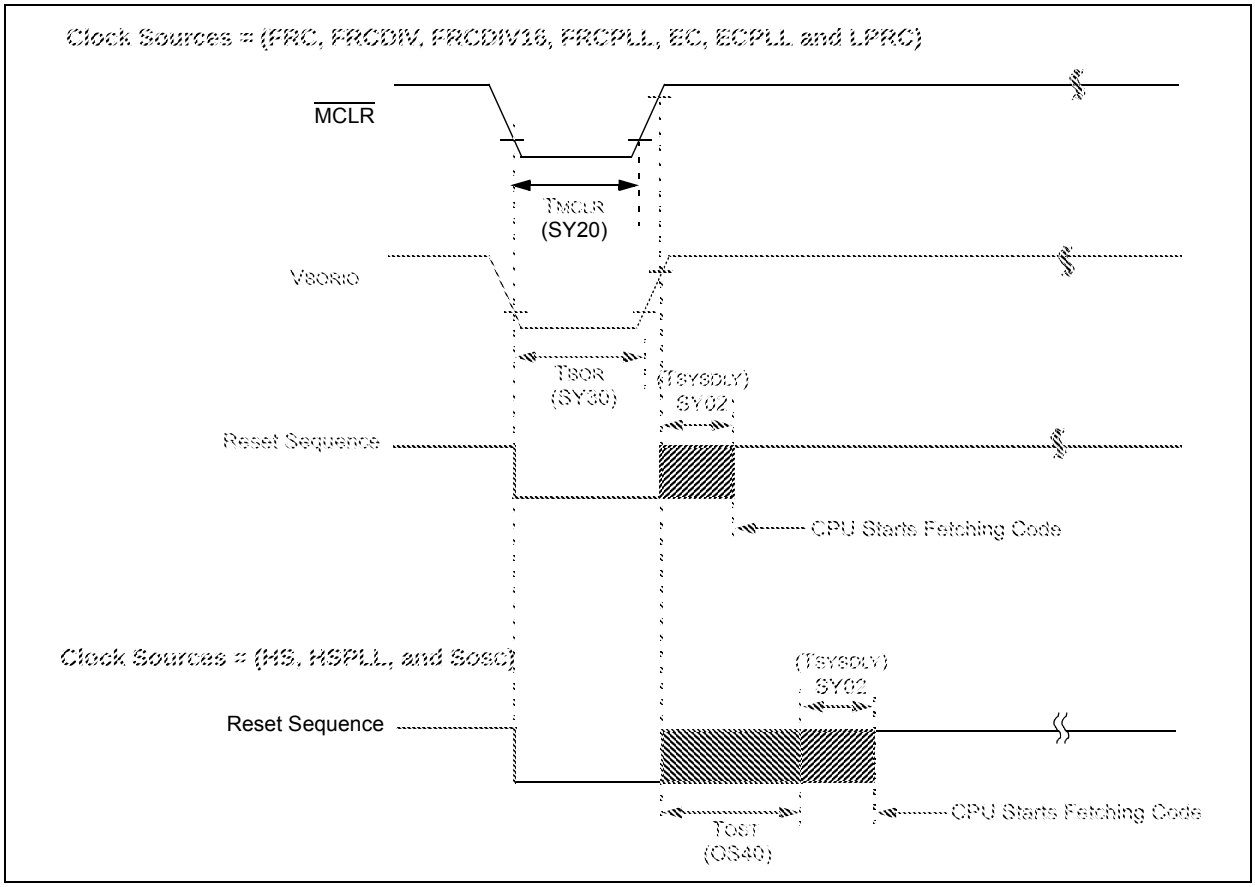


TABLE 44-31: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	µs	—
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	1 µs + 8 SYSCLK cycles	—	—	—
SY20	TMCLR	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	—
SY30	TBOR	BOR Pulse Width (low)	—	1	—	µs	—

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Characterized by design but not tested.

NOTES: