Microchip Technology - PIC32MZ1025DAB169T-I/HF Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1025dab169t-i-hf

TABLE 4-6: INITIATORS TO TARGETS ACCESS ASSOCIATION (CONTINUED)

Target Number	Initiator ID	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Name	CPU	DMA Read	DMA Write	USB	Ethernet Read	Ethernet Write	CAN1	CAN2	SQI1	Flash Controller	Crypto	GLCD	GPU	SDHC
18	2D Graphics Processing Unit	X													
19	Secure Digital Host Controller	X													
20	DDR2 PHY Control Register Interface	X													
21	DDR2 Control Register Interface	X													
22	**Peripheral Set 6:** RTCC DSCTRL	X													
23	External Memory via EBI and EBI Module	X	X	X	X	X	X	X	X	X		X			X

Note 1: The GLCD and GPU are directly connected to the DDR2 SDRAM Controller to use DDR2 SDRAM for frame buffers. Arbitration control is done through the DDR2 SDRAM Controller arbitration engine. Refer to **Section 55. "DDR2 SDRAM Controller"** (DS60001321) in the "PIC32 Family Reference Manual" for additional information.

TABLE 4-23: SYSTEM BUS TARGET PROTECTION GROUP 13 REGISTER MAP

Virtual Address (BF91_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8420	SBT13ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8424	SBT13ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8428	SBT13ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8430	SBT13ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8438	SBT13ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8440	SBT13REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8450	SBT13RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8458	SBT13WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8460	SBT13REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8470	SBT13RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8478	SBT13WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

REGISTER 5-4: NVMDATAx: FLASH DATA REGISTER (x = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATA<31:0>:** Flash Data bits
Word Program: Writes NVMDATA0 to the target Flash address defined in NVMADDR
Quad Word Program: Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the Least Significant Instruction Word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits
The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

Register 9-1: PRESTAT: Prefetch Module Status Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
	—	—	—	—	PFMDED	PFMSEC	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PFMSECCNT<7:0>							

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Write '0'; ignore read

bit 27 **PFMDED:** Flash Double-bit Error Detected (DED) Status bit
This bit is set in hardware and can only be cleared (i.e., set to '0') in software.
1 = A DED error has occurred
0 = A DED error has not occurred

bit 26 **PFMSEC:** Flash Single-bit Error Corrected (SEC) Status bit
1 = A SEC error occurred when PFMSECCNT<7:0> was equal to zero
0 = A SEC error has not occurred

bit 25-8 **Unimplemented:** Write '0'; ignore read

bit 7-0 **PFMSECCNT<7:0>:** Flash SEC Count bits
11111111 - 00000000 = SEC count

TABLE 12-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD9	RPD9R	RPD9R<3:0>	0000 = No Connect 0001 = U3RTS 0010 = U4TX 0011 = Reserved 0100 = U6TX 0101 = SS1 0110 = Reserved 0111 = SS3 1000 = SS4 1001 = SS5 1010 = SDO6 1011 = OC5 1100 = OC8 1101 = Reserved 1110 = C1OUT 1111 = REFCLKO3
RPB8	RPB8R	RPB8R<3:0>	
RPB15	RPB15R	RPB15R<3:0>	
RPD4	RPD4R	RPD4R<3:0>	
RPB0	RPB0R	RPB0R<3:0>	
RPE3	RPE3R	RPE3R<3:0>	
RPB7	RPB7R	RPB7R<3:0>	
RPF12	RPF12R	RPF12R<3:0>	
RPD12	RPD12R	RPD12R<3:0>	
RPF8	RPF8R	RPF8R<3:0>	
RPC3	RPC3R	RPC3R<3:0>	
RPE9	RPE9R	RPE9R<3:0>	
RPG9	RPG9R	RPG9R<3:0>	0000 = No Connect 0001 = U1RTS 0010 = U2TX 0011 = U5RTS 0100 = U6TX 0101 = Reserved 0110 = SS2 0111 = Reserved 1000 = SDO4 1001 = Reserved 1010 = SDO6 1011 = OC2 1100 = OC1 1101 = OC9 1110 = Reserved 1111 = C2TX
RPD0	RPD0R	RPD0R<3:0>	
RPB6	RPB6R	RPB6R<3:0>	
RPD5	RPD5R	RPD5R<3:0>	
RPB2	RPB2R	RPB2R<3:0>	
RPF3	RPF3R	RPF3R<3:0>	
RPC2	RPC2R	RPC2R<3:0>	
RPE8	RPE8R	RPE8R<3:0>	
RPF2	RPF2R	RPF2R<3:0>	

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C10	TMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0C20	PR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0E00	T8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0E10	TMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0E20	PR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
1000	T9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
1010	TMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
1020	PR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 20-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(2)

11111111 = Alarm will trigger 256 times
•
•
•
00000000 = Alarm will trigger one time
The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note:	This register is reset only on a Power-on Reset (POR).

REGISTER 22-26: SQI1XCON4: SQI XIP CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT2SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD3<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD2<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD1<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT2SCHECK:** Flash Initialization 2 Command Status Check bit
1 = Check the status after executing the INIT2 commands
0 = Do not check the status

bit 27-26 **INIT2COUNT<1:0>:** Flash Initialization 2 Command Count bits
11 = INIT2CMD1, INIT2CMD2, and INIT2CMD3 are sent
10 = INIT2CMD1 and INIT2CMD2 are sent, but INIT2CMD3 is still pending
01 = INIT2CMD1 is sent, but INIT2CMD2 and INIT2CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT2TYPE<1:0>:** Flash Initialization 2 Command Type bits
11 = Reserved
10 = INIT2 commands are sent in Quad Lane mode
01 = INIT2 commands are sent in Dual Lane mode
00 = INIT2 commands are sent in Single Lane mode

bit 24-16 **INIT2CMD3<7:0>:** Flash Initialization Command 3 bits
Third command of the Flash initialization.

bit 15-8 **INIT2CMD2<7:0>:** Flash Initialization Command 2 bits
Second command of the Flash initialization.

bit 7-0 **INIT2CMD1<7:0>:** Flash Initialization Command 1 bits
First command of the Flash initialization.

Note: Some Flash devices require write enable and sector unprotect commands before write/read operations and this register is useful in working with those Flash types (XIP mode only)

27.1 Crypto Engine Control Registers

TABLE 27-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>				START	ACTIVE	0000
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRLRLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 31-12: ETHRXWM: ETHERNET CONTROLLER RECEIVE WATERMARKS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFWM<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXEWM<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RXFWM<7:0>:** Receive Full Watermark bits

The software controlled RX Buffer Full Watermark Pointer is compared against the RX BUFCNT to determine the full watermark condition for the FWMARK interrupt and for enabling Flow Control when automatic Flow Control is enabled. The Full Watermark Pointer should always be greater than the Empty Watermark Pointer.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXEWM<7:0>:** Receive Empty Watermark bits

The software controlled RX Buffer Empty Watermark Pointer is compared against the RX BUFCNT to determine the empty watermark condition for the EWMARK interrupt and for disabling Flow Control when automatic Flow Control is enabled. The Empty Watermark Pointer should always be less than the Full Watermark Pointer.

Note: This register is only used for RX operations.

REGISTER 31-33: EMAC1MADR: ETHERNET CONTROLLER MAC MII MANAGEMENT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	—	—	—	PHYADDR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	REGADDR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **PHYADDR<4:0>:** MII Management PHY Address bits

This field represents the 5-bit PHY Address field of Management cycles. Up to 31 PHYs can be addressed (0 is reserved).

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **REGADDR<4:0>:** MII Management Register Address bits

This field represents the 5-bit Register Address field of Management cycles. Up to 32 registers can be accessed.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 36-9: GLCDLxMODE: GRAPHICS LCD CONTROLLER LAYER 'x' MODE REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	LAYEREN	DISABIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALPHA<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DESTBLEND<3:0>				SRCBLEND<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	COLORMODE<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **LAYEREN:** Layer Enable bit
1 = Layer is enabled
0 = Layer is not enabled

bit 30 **DISABIFIL:** Disable Bilinear Filtering bit
1 = Bilinear filtering is enabled
0 = Bilinear filtering is not enabled

bit 29 **FORCEALPHA:** Force Alpha with Global Alpha bit
1 = Force alpha with global alpha is enabled
0 = Force alpha with global alpha is not enabled

bit 28 **MULALPHA:** Premultiply Image Alpha bit
1 = Premultiply image alpha is enabled
0 = Premultiply image alpha is not enabled

bit 27-24 **Unimplemented:** Read as '0'

bit 23-16 **ALPHA<7:0>:** Layer Alpha bits
These bits contain the Layer Alpha value ranging from 0 to 0xFF.

bit 15-12 **DESTBLEND<3:0>:** Destinary Blending Function bits
1111 = Reserved
1110 = Reserved
1101 = Blend inverted destination
1100 = Reserved
1011 = Reserved
1010 = Blend alpha destination
1001 = Reserved
1000 = Reserved
0111 = Blend inverted source and inverted global
0110 = Blend inverted global
0101 = Blend inverted source
0100 = Blend alpha source and alpha global
0011 = Blend alpha global
0010 = Blend alpha source
0001 = Blend white
0000 = Blend black

REGISTER 36-14: GLCDLxRES: GRAPHICS LCD CONTROLLER LAYER 'x' RESOLUTION REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESX<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **RESX<10:0>:** X Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the X dimension.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **RESY<10:0>:** Y Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the Y dimension.

REGISTER 38-24: DDRSCLSTART: DDL SELF CALIBRATION LOGIC START REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	U-0	W-0	U-0	R/W-0
	—	—	SCL PHCAL	SCL START	—	SCLEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	SCLUB PASS(1)	SCLLB PASS(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Write as '0'

bit 29 **SCLPHCAL:** Start Phase Self-calibration Logic bit
- 1 = Phase calibration is enabled
- 0 = Phase calibration is disabled

bit 28 **SCLSTART:** Start Self Calibration Logic bit
- 1 = Start self calibration
- 0 = Do not start self calibration

bit 27 **Unimplemented:** Write as '0'

bit 26 **SCLEN:** Self Calibration Logic Enable bit
- 1 = Enable dynamic self calibration logic
- 0 = Disable dynamic self calibration logic

Note: Enabling dynamic self calibration may impact performance.

bit 25-2 **Unimplemented:** Write as '0'

bit 1 **SCLUBPASS:** Self Calibration Logic Upper Data Byte Status bit(1)
- 1 = Self calibration logic for upper data byte passed
- 0 = Self calibration logic for upper data byte failed

bit 0 **SCLLBPASS:** Self Calibration Logic Lower Data Byte Status bit(1)
- 1 = Self calibration logic for lower data byte passed
- 0 = Self calibration logic for lower data byte failed

Note 1: This bit is set by hardware when the SCL process has passed and is complete.

39.0 SECURE DIGITAL HOST CONTROLLER (SDHC)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 57. "Secure Digital Host Controller (SDHC)"** (DS60001334), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The SDHC module uses a 32-bit System Bus master and slave interface to connect the Host system and standard card interface on the device side.

The core has a built-in DMA controller so that data can be automatically transferred between system memory and the SD/SDIO/eMMC card without intervention from the CPU.

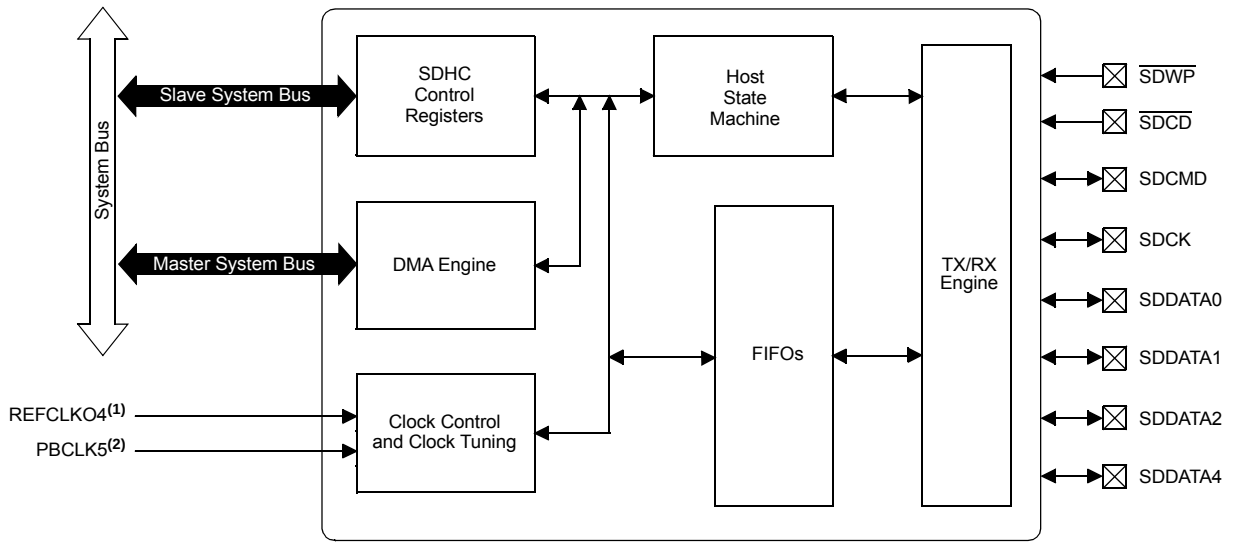
The SDHC module includes the following features:

- SD Association specification compliance:
  - SD Host Controller Simplified Specification, version 2.00
  - Physical Layer Simplified Specification, version 2.00
  - SDIO Simplified Specification, version 2.00
- eMMC Standard: JESD84-A441
- Default and High-Speed modes of operation
- 1-bit or 4-bit data transfers
- Built-in clock divider
- PIO and ADMA modes of data transfer
- 3.3V operation
- Interrupt support
- Stop at block gap

A block diagram of the SDHC module is provided in Figure 39-1.

Note: Transmit and receive buffer addresses in ADMA mode should be word-aligned. When multiple descriptors are used to transfer a single block, all but the last descriptor should have a transfer size in multiples of four.

FIGURE 39-1: SECURE DIGITAL HOST CONTROLLER (SDHC) BLOCK DIAGRAM



Note 1: When configuring the REFCLKO4 clock source, a value of '0' for the ROTRIM<8:0> bits must be selected. REFCLKO4 must be turned on before SDHC Special Function Registers (SFR) access.

2: This clock source is only used for SDHC Special Function Register (SFR) access.

REGISTER 39-3: SDHCMODE: SDHC MODE REGISTER (CONTINUED)

bit 4 **DTXDSEL:** Data Transfer Direction Select bit
1 = Read (card to SDHC)
0 = Write (SDHC to card)

bit 3-2 **ACEN<1:0>:** Auto CMD12 Enable bits
Auto CMD12 is used to stop multiple-block read/write operations.
11 = Reserved
10 = Reserved
01 = Auto CMD12 is enabled
00 = Auto CMD 12 is disabled

bit 1 **BCEN:** Block Count Enable Bit
1 = Block count is enabled
0 = Block count is disabled

bit 0 **DMAEN:** DMA Enable bit
1 = DMA (ADMA) is used to transfer data
0 = CPU is used to transfer data

Note 1: Refer to bits 45-40 of the command format in the *"SD Host Controller Simplified Specification"* (version 2.00).

2: If these bits are set to '1', the SDHC will check the index field in the response to see if it has the same value as the CIDX<5:0> bits, if not, it will be reported as a command index error.

3: If these bits are set to '1', the SDHC will check the CRC field in the response and reports a command CRC error upon a CRC error detection.

REGISTER 39-4: SDHCRESPx: SDHC RESPONSE REGISTER 'x' ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RESP<31:0>:** Response bits

These bits indicate the bit positions of Responses [31:0] defined in the *"SD Host Controller Simplified Specification* (version 2.00). Refer to Table 39-2 for full bit definitions.

TABLE 39-2: RESPONSE BIT DEFINITION FOR EACH RESPONSE TYPE

Response Type (see Note 1)	Response Meaning	Response Register
R1, R1b (normal response)	Card status	SDHCRESP0<31:0>
R1b (Auto CMD12 response)	Card status for Auto CMD12	SDHCRESP3<31:0>
R2 (CID, CSD register)	CID or CSD register	SDHCRESP0<31:0> SDHCRESP1<31:0> SDHCRESP2<31:0> SDHCRESP3<31:0>
R3 (OCR register)	OCR register for memory	SDHCRESP0<31:0>
R4 (OCR register)	OCR register for I/O, etc.	SDHCRESP0<31:0>
R5, R5b	SDIO response	SDHCRESP0<31:0>
R6 (published RCA response)	New published RCA<31:16>, etc.	SDHCRESP0<31:0>

Note 1: For additional information, refer to the "*SD Host Controller Simplified Specification"* (version 2.00), the "*Physical Layer Simplified Specification"* (version 2.00), and the *"SDIO Simplified Specification"* (version 2.00). These documents are available for download by visiting the SD Association web site at: http://www.sdcard.org/downloads/pls/simplified_specs/archive/index.html

42.0 INSTRUCTION SET

The PIC32MZ Graphics (DA) Family family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32MZ DA device family *does not* support the following features:

- Core extend instructions
- Coprocessor 2 instructions

Note:	Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

TABLE 44-57: SD HOST CONTROLLER DEFAULT MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD20	tSDCK	Clock Frequency	—	—	25	MHz	—
SD21	tDUTY	Duty Cycle	—	50	—	%	—
SD22	tHIGH	Clock High Time	10	—	—	ns	—
SD23	tLOW	Clock Low Time	10	—	—	ns	—
SD24	tRISE	Clock Rise Time	—	10	—	ns	—
SD25	tFALL	Clock Fall Time	—	10	—	ns	—
SD26	tSETUP	Input Setup Time	5	—	—	ns	—
SD27	tHOLD	Input Hold Time	5	—	—	ns	—

TABLE 44-58: SD HOST CONTROLLER HIGH-SPEED MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD30	tSDCK	Clock Frequency	—	—	50	MHz	—
SD31	tDUTY	Duty Cycle	—	50	—	%	—
SD32	tHIGH	Clock High Time	7	—	—	ns	—
SD33	tLOW	Clock Low Time	7	—	—	ns	—
SD34	tRISE	Clock Rise Time	—	3	—	ns	—
SD35	tFALL	Clock Fall Time	—	3	—	ns	—
SD36	tSETUP	Input Setup Time	6	—	—	ns	—
SD37	tHOLD	Input Hold Time	2	—	—	ns	—

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
25.0 "Parallel Master Port (PMP)"	The All Resets value for bits 15:0 of the PMSTAT register in the Parallel Master Port Register Map was updated (see Table 25-1).
26.0 "External Bus Interface (EBI)"	The All Resets values were updated in the EBI Register Map (see Table 26-2).
29.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	The All Resets values for the ADCCON1 and ADCxTIME registers were updated and the Virtual Addresses for the ADCxCFG, ADCSYSCFGx, and ADCDATAx registers were updated in the ADC Register Map (see Table 29-1).
34.0 "High/Low-Voltage Detect (HLVD)"	The chapter was renamed and the introduction was updated. The HLVDCON register was updated (see Table 34-1 and Register 34-1). High/Low-Voltage Detect (HLVD) Module Block Diagram was updated (see Figure 34-1)
36.0 "Graphics LCD (GLCD) Controller"	The Graphics LCD Controller Register Map was updated (see Table 36-1). These registers were updated: • **Register 36-2: "GLCDCLKCON: Graphics LCD Controller Clock Control Register"** • **Register 36-4: "GLCDRES: Graphics LCD Controller Resolution Register"** • **Register 36-5: "GLCDFPORCH: Graphics LCD Controller Front Porch Register"** • **Register 36-6: "GLCDBLANKING: Graphics LCD Controller Blanking Register"** • **Register 36-7: "GLCDBPORCH: Graphics LCD Controller Back Porch Register"** • **Register 36-8: "GLCDCURSOR: Graphics LCD Controller Cursor Register"** • **Register 36-10: "GLCDLxstart: graphics lcd controller layer 'x' start register ('x' = 0-2)"** • **Register 36-11: "GLCDLxsize: graphics lcd controller layer 'x' size register ('x' = 0-2)"** • **Register 36-14: "GLCDLxres: graphics lcd controller layer 'x' resolution register ('x' = 0-2)"**
37.0 "2-D Graphics Processing Unit (GPU)"	The introduction was updated.
39.0 "Secure Digital Host Controller (SDHC)"	The SDHC block diagram was updated (see Figure 39-1). The SDHC Register Map was updated (see Table 39-1). The bit values for the CDSLVL bit in the SDHCSTAT1 register were updated (see Register 39-6). The SDHCCAP register was updated (see Register 39-13).
40.0 "Power-Saving Features"	**40.2.3 "Deep Sleep Mode"** was updated. References to High-Voltage Detect were removed in the PMD Register Summary (Table 40-2) and the PMD Bits and Locations (Table 40-3).
41.0 "Special Features"	The CFGCON2 register was updated (see Table 41-3 and Register 41-12).