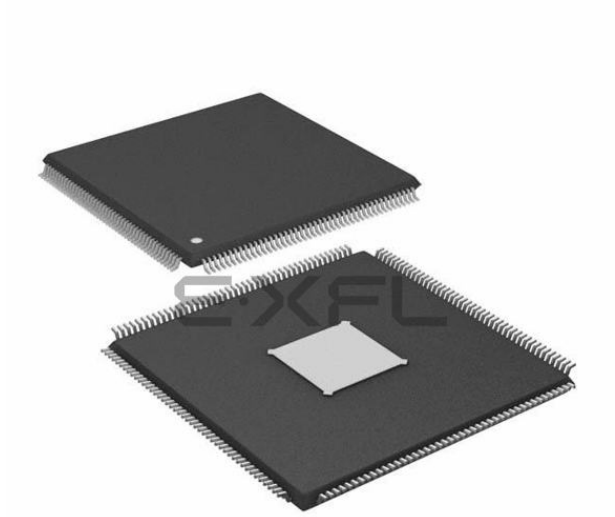
Microchip Technology - PIC32MZ1025DAB176T-I/2J Datasheet



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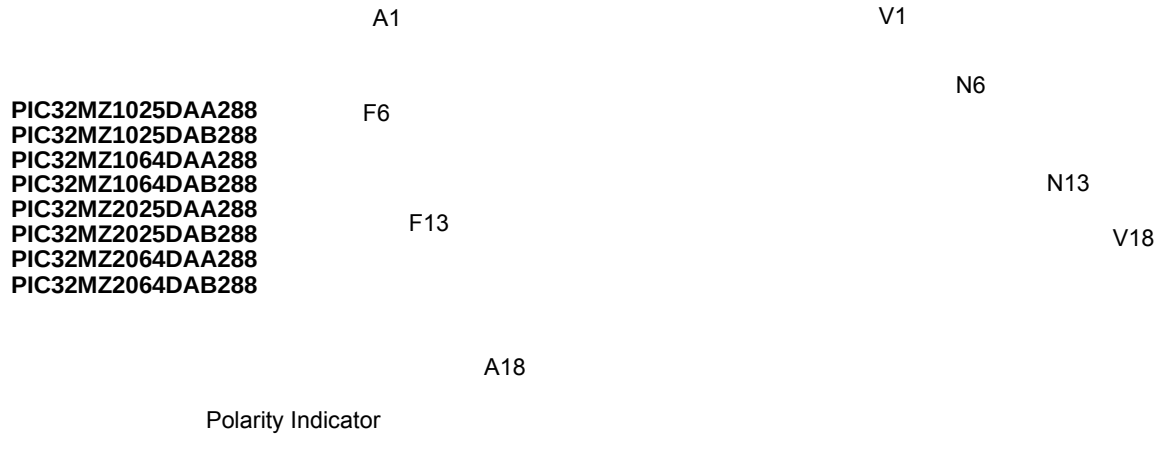
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1025dab176t-i-2j

TABLE 7: PIN NAMES FOR 288-PIN DEVICES (CONTINUED)

288-PIN LFBGA (BOTTOM VIEW)



PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288

Ball/Pin Number	Full Pin Name
V3	DDRA15
V4	VDDCORE
V5	RTCC/RPD0/RD0
V6	SCK4/RD10
V7	GD6/EBIA11/RPF0/PMA11/RF0
V8	GD21/EBIA23/RH15
V9	GD3/EBIA8/RPG0/PMA8/RG0
V10	EBID2/PMD2/RE2
V11	ERXDV/ECRSDV/RH13
V12	ERXD3/RH9
V13	ETXD2/RH0
V14	ETXD0/RJ8
V15	ETXERR/RJ0
V16	ETXEN/RPD6/RD6
V17	GD1/EBID14/PMD14/RA4
V18	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.

5: This pin is a No Connect when DDR is not connected in the system.

6: These pins are restricted to input functions only.

1.0 DEVICE OVERVIEW

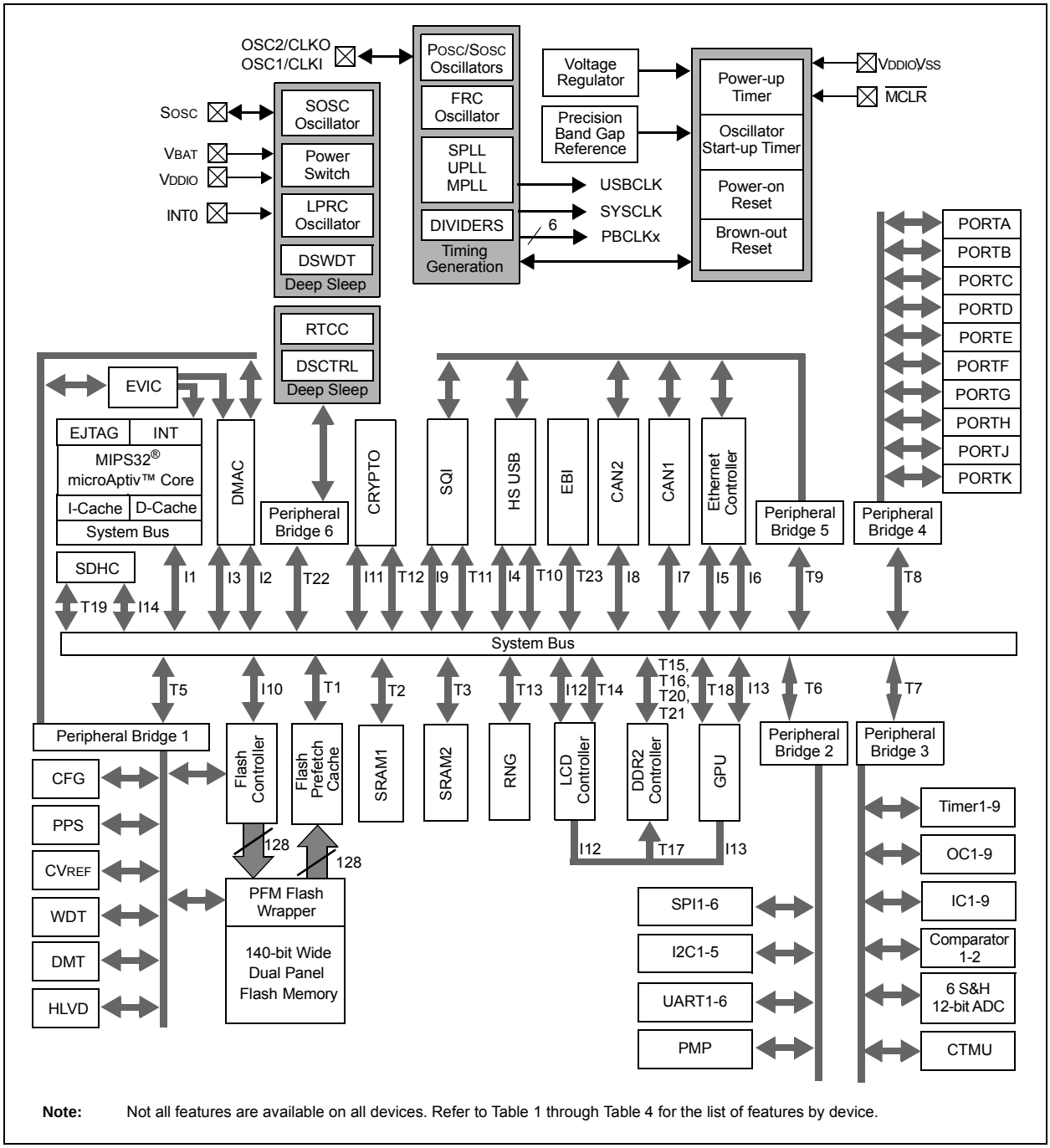
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This data sheet contains device-specific information for the PIC32MZ DA family of devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ DA family of devices.

Table 1-1 through Table 1-24 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 5 through Table 7).

FIGURE 1-1: PIC32MZ DA FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to Table 1 through Table 4 for the list of features by device.

TABLE 1-22: DDR2 SDRAM CONTROLLER PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
DDR2 SDRAM Controller						
DDRCK	DDR Internal to the Package	DDR Internal to the Package	K2	O	SSTL	Differential Clocks
$\overline{\text{DDRCK}}$			K1	O	SSTL	
DDRCKE			L2	O	SSTL	Clock Enable
$\overline{\text{DDRCS0}}$			N2	O	SSTL	Chip Select 0
$\overline{\text{DDRRAS}}$			M1	O	SSTL	Row Address Strobe
$\overline{\text{DDRCAS}}$			P2	O	SSTL	Column Address Strobe
$\overline{\text{DDRWE}}$			L1	O	SSTL	Write Enable Strobe
DDRLDM			G3	O	SSTL	Lower Data Byte Mask
DDRUDM			A3	O	SSTL	Upper Data Byte Mask
DDRODT			N1	O	SSTL	On-Die Termination
DDRLDQS			E1	I/O	SSTL	Lower Data Byte Qualifier Strobes (Differential)
$\overline{\text{DDRLDQS}}$			E2	I/O	SSTL	
DDRUDQS			B2	I/O	SSTL	Upper Data Byte Qualifier Strobes (Differential)
$\overline{\text{DDRUDQS}}$			A2	I/O	SSTL	
DDRBA0			M2	O	SSTL	Bank Address Select 0
DDRBA1			M3	O	SSTL	Bank Address Select 1
DDRBA2			U4	O	SSTL	Bank Address Select 2
DDRA0			R1	O	SSTL	DDR2 Address Bus
DDRA1			L3	O	SSTL	
DDRA2			N3	O	SSTL	
DDRA3			R2	O	SSTL	
DDRA4			P3	O	SSTL	
DDRA5			T1	O	SSTL	
DDRA6			U1	O	SSTL	
DDRA7			T2	O	SSTL	
DDRA8			U2	O	SSTL	
DDRA9			R3	O	SSTL	
DDRA10			P1	O	SSTL	
DDRA11			V2	O	SSTL	
DDRA12			T3	O	SSTL	
DDRA13			U3	O	SSTL	
DDRA14			T4	O	SSTL	
DDRA15			V3	O	SSTL	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select; SSTL = Stub Series Terminated Logic

TABLE 4-8: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS (CONTINUED)

Target Protection Number	Target Description (see Note 5)	SBTxREGy Register (see Note 7)							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
14	DSCTRL RTCC	SBT14REG0	R	0x1F8C0000	R	4 KB	—	0	SBT14RD0	R/W(1)	SBT14WR0	R/W(1)
		SBT14REG1	R/W	R/W	R/W	R/W	—	3	SBT14RD1	R/W(1)	SBT14WR1	R/W(1)
15	USB	SBT15REG0	R	0x1F8E0000	R	4 KB	—	0	SBT15RD0	R/W(1)	SBT15WR0	R/W(1)
	Crypto		R	0x1F8E5000	R	4 KB	—	0		R/W(1)		R/W(1)
	RNG		R	0x1F8E6000	R	4 KB	—	0		R/W(1)		R/W(1)
	SDHC		R	0x1F8EC000	R	4 KB	—	0		R/W(1)		R/W(1)
16	External Memory via DDR2 and DDR2 Targets 3 and 4	SBT16REG0	R	0x08000000	R	R(4)	—	0	SBT16RD0	R/W(1)	SBT16WR0	R/W(1)
		SBT16REG1	R/W	R/W	R/W	R/W	—	3	SBT16RD1	R/W(1)	SBT16WR1	R/W(1)
		SBT16REG2	R/W	R/W	R/W	R/W	1	2	SBT16RD2	R/W(1)	SBT16WR2	R/W(1)
		SBT16REG3	R/W	R/W	R/W	R/W	1	2	SBT16RD3	R/W(1)	SBT16WR3	R/W(1)
		SBT16REG4	R/W	R/W	R/W	R/W	1	2	SBT16RD4	R/W(1)	SBT16WR4	R/W(1)

Legend: R = Read; R/W = Read/Write; ‘x’ in a register name = 0-13; ‘y’ in a register name = 0-8.

Note 1: Reset values for these bits are ‘0’, ‘1’, ‘1’, ‘1’, respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Map (Figure 4-1) for specific device memory sizes and start addresses.

5: See Table 4-2 for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

7: The ‘x' in the SBTxREGy, SBTxRDy, and SBTxWRy registers represents the target protection number and not the actual target number (e.g., for SQI ‘x’ = 13 and not 11, whereas 11 is the actual target number).

TABLE 4-10: SYSTEM BUS TARGET PROTECTION GROUP 0 (T0PGV0 - T0PGV3) REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8020	SBT0ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8024	SBT0ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8028	SBT0ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8030	SBT0ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8038	SBT0ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8040	SBT0REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8050	SBT0RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8058	SBT0WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8060	SBT0REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8070	SBT0RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8078	SBT0WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7) (CONTINUED)

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **TXMAXP<10:0>:** Maximum TX Payload per transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

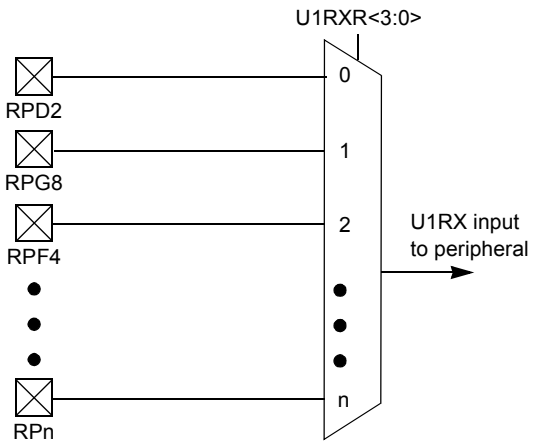
TXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-1, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-1.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 12-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect 0001 = U3TX 0010 = $\overline{\text{U4RTS}}$ 0011 = Reserved 0100 = Reserved 0101 = SDO1 0110 = SDO2 0111 = SDO3 1000 = Reserved 1001 = SDO5 1010 = $\overline{\text{SS6}}$ 1011 = OC3 1100 = OC6 1101 = REFCLKO4 1110 = C2OUT 1111 = C1TX
RPG8	RPG8R	RPG8R<3:0>	
RPF4	RPF4R	RPF4R<3:0>	
RPF1	RPF1R	RPF1R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPB5	RPB5R	RPB5R<3:0>	
RPC1	RPC1R	RPC1R<3:0>	
RPD14	RPD14R	RPD14R<3:0>	
RPG1	RPG1R	RPG1R<3:0>	
RPA14	RPA14R	RPA14R<3:0>	
RPD6	RPD6R	RPD6R<3:0>	
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect 0001 = U1TX 0010 = $\overline{\text{U2RTS}}$ 0011 = U5TX 0100 = $\overline{\text{U6RTS}}$ 0101 = SDO1 0110 = SDO2 0111 = SDO3 1000 = SDO4 1001 = SDO5 1010 = Reserved 1011 = OC4 1100 = OC7 1101 = Reserved 1110 = Reserved 1111 = REFCLKO1
RPG7	RPG7R	RPG7R<3:0>	
RPF5	RPF5R	RPF5R<3:0>	
RPD11	RPD11R	RPD11R<3:0>	
RPF0	RPF0R	RPF0R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPE5	RPE5R	RPE5R<3:0>	
RPB3	RPB3R	RPB3R<3:0>	
RPC4	RPC4R	RPC4R<3:0>	
RPG0	RPG0R	RPG0R<3:0>	
RPA15	RPA15R	RPA15R<3:0>	
RPD7	RPD7R	RPD7R<3:0>	

NOTES:

REGISTER 25-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits(1)

1111 = Wait of 16 TPB
•
•
•
0001 = Wait of 2 TPB
0000 = Wait of 1 TPB (default)

bit 1-0 **WAITE<1:0>:** Data Hold After Read/Write Strobe Wait States bits(1)

11 = Wait of 4 TPB
10 = Wait of 3 TPB
01 = Wait of 2 TPB
00 = Wait of 1 TPB (default)

For Read operations:
11 = Wait of 3 TPB
10 = Wait of 2 TPB
01 = Wait of 1 TPB
00 = Wait of 0 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

REGISTER 29-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

bit 5-6 **Unimplemented:** Read as '0'

bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

REGISTER 30-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN15	MSEL15<1:0>		FSEL15<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN14	MSEL14<1:0>		FSEL14<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN13	MSEL13<1:0>		FSEL13<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN12	MSEL12<1:0>		FSEL12<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN15:** Filter 15 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL14<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 31-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HTEN	MPEN	—	NOTPM	PMMODE<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **HTEN:** Enable Hash Table Filtering bit
1 = Enable Hash Table Filtering
0 = Disable Hash Table Filtering

bit 14 **MPEN:** Magic Packet™ Enable bit
1 = Enable Magic Packet Filtering
0 = Disable Magic Packet Filtering

bit 13 **Unimplemented:** Read as '0'

bit 12 **NOTPM:** Pattern Match Inversion bit
1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
0 = The Pattern Match Checksum must match for a successful Pattern Match to occur
This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 **PMMODE<3:0>:** Pattern Match Mode bits
1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)**(1,3)**
1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)**(1,1)**
0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)**(1)**
0000 = Pattern Match is disabled; pattern match is always unsuccessful

Note 1: XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

REGISTER 36-7: GLCDBPORCH: GRAPHICS LCD CONTROLLER BACK PORCH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BPORCHX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BPORCHX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BPORCHY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BPORCHY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **BPORCHX<10:0>:** X Dimension Back Porch Lines bits
These bits specify the front porch X dimension lines.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **BPORCHY<10:0>:** Y Dimension Back Porch Pixel Clocks bits
These bits specify the front porch Y dimension pixel clocks.

REGISTER 36-8: GLCDCURSOR: GRAPHICS LCD CONTROLLER CURSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CURSORX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CURSORX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CURSORY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CURSORY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **CURSORX<10:0>:** Cursor X Dimension Position bits
These bits specify the X dimension position of the cursor

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **CURSORY<10:0>:** Cursor Y Dimension Position bits
These bits specify the Y dimension position of the cursor

NOTES:

TABLE 39-1: SDHC SFR SUMMARY (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C054	SDHC AESTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	ALMERR	AERRST<1:0>		0000
C058	SDHC AADDR	31:16	ADDR<31:16>																0000
		15:0	ADDR<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

REGISTER 39-13: SDHCCAP: SDHC CAPABILITIES REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1, HS
	—	—	—	—	—	—	—	VOLT3V3
23:16	R-x, HS	U-0	R-x, HS	U-0	R-x, HS	U-0	R-0, HS	R-0, HS
	SRESUME	—	HISPEED	—	ADMA2	—	MBLEN<1:0>	
15:8	U-0	U-0	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS
	—	—	BASECLK<5:0>					
7:0	R-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	TOCLKU	—	TOCLKFREQ<5:0>					

Legend:		HS = Hardware settable	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **VOLT3V3:** 3.3V Voltage Support bit
1 = Voltage of 3.3V is supported

bit 23 **SRESUME:** Suspend/Resume Support bit
1 = Suspend/resume is supported
0 = Suspend/resume is not supported

bit 22 **Unimplemented:** Read as '0'

bit 21 **HISPEED:** High-speed Support bit
1 = High speed is supported
0 = High speed is not supported

bit 20 **Unimplemented:** Read as '0'

bit 19 **ADMA2:** ADMA2 Support bit
1 = ADMA2 is supported
0 = ADMA2 is not supported

bit 18 **Unimplemented:** Read as '0'

bit 17-16 **MBLEN<1:0>:** Maximum Block Length bits
11 = Reserved
10 = 2048
01 = 1024
00 = 512

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **BASECLK<5:0>:** Base Clock Frequency for SDCLK bits
111111 = 63 MHz
111110 = 62 MHz
111101 = 61 MHz
.
.
.
000010 = 2 MHz
000001 = 1 MHz
000000 = Reserved

bit 7 **TOCLKU:** Time-out Clock Unit bit
1 = Time-out clock unit is in kHz
0 = Time-out clock unit is in MHz

bit 6 **Unimplemented:** Read as '0'

REGISTER 41-1: DEVSIGN0/ADEVSIGN0: DEVICE SIGNATURE WORD 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30-0 **Reserved:** Write as '1'

Note: The DEVSIGN1 through DEVSIGN3 and ADEVSIGN1 through ADEVSIGN3 registers are used for Quad Word programming operation when programming the DEVSIGN0/ADESIGN0 registers, and do not contain any valid information.

REGISTER 41-2: DEVCP0/ADEVCP0: DEVICE CODE-PROTECT 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	r-1	r-1	r-1	r-1
	—	—	—	CP	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection is disabled
0 = Protection is enabled

bit 27-0 **Reserved:** Write as '1'

Note: The DEVCP1 through DEVCP3 and ADEVCP1 through ADEVCP3 registers are used for Quad Word programming operation when programming the DEVCP0/ADEVCP0 registers, and do not contain any valid information.

TABLE 44-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20	VOH	**Output High Voltage** I/O Pins 4x Sink Driver Pins - RA0-RA3, RA9, RA10, RA14, RA15 RB0, RB4, RB6, RB7, RB10, RB11, RB12, RB14 RC12-RC15 RD6, RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8, RF12 RG15 RH0, RH1, RH4-RH14 RJ0-RJ2, RJ8, RJ9, RJ11	2.4	—	—	V	$I_{OH} \geq$ -10 mA, V_{DDIO} = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins - RA4, RA5 RB2, RB3, RB5, RB8, RB9, RB13, RB14, RB15 RC1-RC4 RD0-RD3, RD9, RD10, RD12, RD13 RE0-RE7 RF0, RF1, RF4, RF5, RF13 RG0, RG1, RG6, RG7, RG8, RG9 RH2, RH3, RH7, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	2.4	—	—	V	$I_{OH} \geq$ -15 mA, V_{DDIO} = 3.3V
		Output High Voltage I/O Pins: 12x Source Driver Pins - RA6, RA7 RD4, RD5 RG12-RG14	2.4	—	—	V	$I_{OH} \geq$ -20 mA, V_{DDIO} = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
25.0 "Parallel Master Port (PMP)"	The All Resets value for bits 15:0 of the PMSTAT register in the Parallel Master Port Register Map was updated (see Table 25-1).
26.0 "External Bus Interface (EBI)"	The All Resets values were updated in the EBI Register Map (see Table 26-2).
29.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	The All Resets values for the ADCCON1 and ADCxTIME registers were updated and the Virtual Addresses for the ADCxCFG, ADCSYSCFGx, and ADCDATAx registers were updated in the ADC Register Map (see Table 29-1).
34.0 "High/Low-Voltage Detect (HLVD)"	The chapter was renamed and the introduction was updated. The HLVDCON register was updated (see Table 34-1 and Register 34-1). High/Low-Voltage Detect (HLVD) Module Block Diagram was updated (see Figure 34-1)
36.0 "Graphics LCD (GLCD) Controller"	The Graphics LCD Controller Register Map was updated (see Table 36-1). These registers were updated: • **Register 36-2: "GLCDCLKCON: Graphics LCD Controller Clock Control Register"** • **Register 36-4: "GLCDRES: Graphics LCD Controller Resolution Register"** • **Register 36-5: "GLCDFPORCH: Graphics LCD Controller Front Porch Register"** • **Register 36-6: "GLCDBLANKING: Graphics LCD Controller Blanking Register"** • **Register 36-7: "GLCDBPORCH: Graphics LCD Controller Back Porch Register"** • **Register 36-8: "GLCDCURSOR: Graphics LCD Controller Cursor Register"** • **Register 36-10: "GLCDLxstart: graphics lcd controller layer 'x' start register ('x' = 0-2)"** • **Register 36-11: "GLCDLxsize: graphics lcd controller layer 'x' size register ('x' = 0-2)"** • **Register 36-14: "GLCDLxres: graphics lcd controller layer 'x' resolution register ('x' = 0-2)"**
37.0 "2-D Graphics Processing Unit (GPU)"	The introduction was updated.
39.0 "Secure Digital Host Controller (SDHC)"	The SDHC block diagram was updated (see Figure 39-1). The SDHC Register Map was updated (see Table 39-1). The bit values for the CDSLVL bit in the SDHCSTAT1 register were updated (see Register 39-6). The SDHCCAP register was updated (see Register 39-13).
40.0 "Power-Saving Features"	**40.2.3 "Deep Sleep Mode"** was updated. References to High-Voltage Detect were removed in the PMD Register Summary (Table 40-2) and the PMD Bits and Locations (Table 40-3).
41.0 "Special Features"	The CFGCON2 register was updated (see Table 41-3 and Register 41-12).