Microchip Technology - PIC32MZ1025DAH169-I/6J Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1025dah169-i-6j

TABLE 4-4: BOOT FLASH 2 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC6_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF3C	ABF2DEVCFG4	31:0	**Note:** See Table 41-2 for the bit descriptions.																xxxx
FF40	ABF2DEVCFG3	31:0																	xxxx
FF44	ABF2DEVCFG2	31:0																	xxxx
FF48	ABF2DEVCFG1	31:0																	xxxx
FF4C	ABF2DEVCFG0	31:0																	xxxx
FF50	ABF2DEVCP3	31:0																	xxxx
FF54	ABF2DEVCP2	31:0																	xxxx
FF58	ABF2DEVCP1	31:0																	xxxx
FF5C	ABF2DEVCP0	31:0																	xxxx
FF60	ABF2DEVSIGN3	31:0																	xxxx
FF64	ABF2DEVSIGN2	31:0																	xxxx
FF68	ABF2DEVSIGN1	31:0																	xxxx
FF6C	ABF2DEVSIGN0	31:0																	xxxx
FF70	ABF2SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	ABF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF78	ABF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF7C	ABF2SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFBC	BF2DEVCFG4	31:0	**Note:** See Table 41-1 for the bit descriptions.																xxxx
FFC0	BF2DEVCFG3	31:0																	xxxx
FFC4	BF2DEVCFG2	31:0																	xxxx
FFC8	BF2DEVCFG1	31:0																	xxxx
FFCC	BF2DEVCFG0	31:0																	xxxx
FFD0	BF2DEVCP3	31:0																	xxxx
FFD4	BF2DEVCP2	31:0																	xxxx
FFD8	BF2DEVCP1	31:0																	xxxx
FFDC	BF2DEVCP0	31:0																	xxxx
FFE0	BF2DEVSIGN3	31:0																	xxxx
FFE4	BF2DEVSIGN2	31:0																	xxxx
FFE8	BF2DEVSIGN1	31:0																	xxxx
FFEC	BF2DEVSIGN0	31:0																	xxxx
FFF0	BF2SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	BF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF8	BF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFFC	BF2SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F4	OFF045	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05FC	OFF047	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0600	OFF048	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0604	OFF049	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0608	OFF059	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
060C	OFF051	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0610	OFF052	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0614	OFF053	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0618	OFF054	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
061C	OFF055	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0620	OFF056	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0624	OFF057	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0628	OFF058	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
062C	OFF059	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is only available on devices with a Crypto module.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER (CONTINUED)

bit 3 **SENDMONEN:** Session End VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session End range (between 0.2V and 0.8V)
0 = Disable monitoring for VBUS in Session End range

bit 2 **USBIE:** USB General Interrupt Enable bit
1 = Enables general interrupt from USB module
0 = Disables general interrupt from USB module

bit 1 **USBRIE:** USB Resume Interrupt Enable bit
1 = Enable remote resume from suspend Interrupt
0 = Disable interrupt to a Remote Devices USB resume signaling

bit 0 **USBWKUPEN:** USB Activity Detection Interrupt Enable bit
1 = Enable interrupt for detection of activity on USB bus in Sleep mode
0 = Disable interrupt for detection of activity on USB bus in Sleep mode

REGISTER 17-1: DMTCON: DEADMAN TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Deadman Timer Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is disabled

bit 13-0 **Unimplemented:** Read as ‘0’

Note 1: This bit only has control when FDMTEN (DEVCFG1<3>) = 0.

REGISTER 17-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP1<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-8 **STEP1<7:0>:** Preclear Enable bits
01000000 = Enables the Deadman Timer Preclear (Step 1)
All other write patterns = Set BAD1 flag.
These bits are cleared when a DMT reset event occurs. STEP1<7:0> is also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 22-1: SQI1XCON1: SQI XIP CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	SDRCMD	DDRDATA	DDRDUMMY	DDRMODE	DDRADDR	DDRCMD(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DUMMYBYTES<2:0>			ADDRBYTES<2:0>			READOPCODE<7:6>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	READOPCODE<5:0>						TYPEDATA<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TYPEDUMMY<1:0>		TYPEMODE<1:0>		TYPEADDR<1:0>		TYPECMD<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **SDRCMD:** SQI Command in SDR Mode bit
1 = SQI command is in SDR mode and SQI data is in DDR mode
0 = SQI command is in DDR mode and SQI data is in DDR mode

bit 28 **DDRDATA:** SQI Data DDR Mode bit
1 = SQI data bytes are transferred in DDR mode
0 = SQI data bytes are transferred in SDR mode

bit 27 **DDRDUMMY:** SQI Dummy DDR Mode bit
1 = SQI dummy bytes are transferred in DDR mode
0 = SQI dummy bytes are transferred in SDR mode

bit 26 **DDRMODE:** SQI DDR Mode bit
1 = SQI mode bytes are transferred in DDR mode
0 = SQI mode bytes are transferred in SDR mode

bit 25 **DDRADDR:** SQI Address Mode bit
1 = SQI address bytes are transferred in DDR mode
0 = SQI address bytes are transferred in SDR mode

bit 24 **DDRCMD:** SQI DDR Command Mode bit(1)
1 = SQI command bytes are transferred in DDR mode
0 = SQI command bytes are transferred in SDR mode

bit 23-21 **DUMMYBYTES<2:0>:** Transmit Dummy Bytes bits
111 = Transmit seven dummy bytes after the address bytes
•
•
•
011 = Transmit three dummy bytes after the address bytes
010 = Transmit two dummy bytes after the address bytes
001 = Transmit one dummy bytes after the address bytes
000 = Transmit zero dummy bytes after the address bytes

Note 1: When DDRCMD is set to '0', the SQI module will ignore the value in the SDRCMD bit.

REGISTER 27-1: CEVER: CRYPTO ENGINE REVISION, VERSION, AND ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **REVISION<7:0>:** Crypto Engine Revision bits

bit 23-16 **VERSION<7:0>:** Crypto Engine Version bits

bit 15-0 **ID<15:0>:** Crypto Engine Identification bits

REGISTER 28-1: RNGVER: RANDOM NUMBER GENERATOR VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **ID<15:0>:** Block Identification bits

bit 15-8 **VERSION<7:0>:** Block Version bits

bit 7-0 **REVISION<7:0>:** Block Revision bits

REGISTER 30-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN7	MSEL7<1:0>		FSEL7<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN6	MSEL6<1:0>		FSEL6<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN5	MSEL5<1:0>		FSEL5<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN4	MSEL4<1:0>		FSEL4<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN7:** Filter 7 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL7<1:0>:** Filter 7 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL7<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN6:** Filter 6 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL6<1:0>:** Filter 6 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL6<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)

bit 15 **FLTEN5:** Filter 17 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL5<1:0>:** Filter 5 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL5<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4:** Filter 4 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL4<1:0>:** Filter 4 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL4<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Table 31-1 and Table 31-2 show two interfaces and the associated pins that can be used with the Ethernet Controller.

TABLE 31-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXCLK	Transmit Clock
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
ETXD2	Transmit Data
ETXD3	Transmit Data
ETXERR	Transmit Error
ERXCLK	Receive Clock
ERXDV	Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXD2	Receive Data
ERXD3	Receive Data
ERXERR	Receive Error
ECRS	Carrier Sense
ECOL	Collision Indication

TABLE 31-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
EREFCLK	Reference Clock
ECRSDV	Carrier Sense – Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXERR	Receive Error

Note: Ethernet controller pins that are not used by selected interface can be used by other peripherals.

REGISTER 38-21: DDRMEMWIDTH: DDR MEMORY WIDTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	—	—	—	—	HALFRATE	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **HALFRATE:** Half-rate Mode bit

The PIC32 always operates in Half-rate mode. This bit must be set during initialization.

1 = Half-rate mode

0 = Full-rate mode

bit 2-0 **Unimplemented:** Read as '0'

REGISTER 38-27: DDRSCLCFG1: DDR SCL CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
	—	—	—	DBLREFDLY	WCASLAT<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	—	—	—	—	—	—	—	SCLCSEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12 **DBLREFDLY:** Double Reference Delay bit

Determines whether the PHY will delay an SCL operation following an acknowledge by one or two time intervals. The time interval is a function of the hardware design.

1 = SCL operation delay doubled

0 = SCL operation delay not doubled

bit 11-8 **WCASLAT<3:0>:** Write CAS Latency bits

DRAM write CAS latency in clock cycles.

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SCLCSEN:** SCL Chip Select Enable bit

1 = Run SCL on Chip Select 0

0 = Do not run SCL on Chip Select 0

REGISTER 39-2: SDHCARG: SDHC ARGUMENT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ARG<31:0>:** Command Argument bits

REGISTER 41-12: CFGPG: PERMISSION GROUP CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	GPUPG<1:0>		GLCDPG<1:0>		CRYPTPG<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCPG<1:0>		SQI1PG<1:0>		SDHCPG<1:0>		ETHPG<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>	
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	DMAPG<1:0>		—	—	CPUPG<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **GPUPG<1:0>:** 2D Graphics Processing Unit Permission Group bits
- 11 = Initiator is assigned to Permission Group 3
- 10 = Initiator is assigned to Permission Group 2
- 01 = Initiator is assigned to Permission Group 1
- 00 = Initiator is assigned to Permission Group 0

bit 27-26 **GLCDPG<1:0>:** Graphics LCD Controller Permission Group bits
Same definition as bits 29-28.

bit 25-24 **CRYPTPG<1:0>:** Crypto Engine Permission Group bits
Same definition as bits 29-28.

bit 23-22 **FCPG<1:0>:** Flash Control Permission Group bits
Same definition as bits 29-28.

bit 21-20 **SQI1PG<1:0>:** SQI Module Permission Group bits
Same definition as bits 29-28.

bit 19-18 **SDHCPG<1:0>:** Secure Digital Host Controller Permission Group bits
Same definition as bits 29-28.

bit 17-16 **ETHPG<1:0>:** Ethernet Module Permission Group bits
Same definition as bits 29-28.

bit 15-14 **CAN2PG<1:0>:** CAN2 Module Permission Group bits
Same definition as bits 29-28.

bit 13-12 **CAN1PG<1:0>:** CAN1 Module Permission Group bits
Same definition as bits 29-28.

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **USBPG<1:0>:** USB Module Permission Group bits
Same definition as bits 29-28.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DMAPG<1:0>:** DMA Module Permission Group bits
Same definition as bits 29-28.

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CPUPG<1:0>:** CPU Permission Group bits
Same definition as bits 29-28.

TABLE 44-17: DC CHARACTERISTICS: DDR2 SDRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No. (Note 1)	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DDRM12	I_{DD0}	Operating Current, One Bank Active Precharge	—	—	90	mA	**Note 2**
DDRM13	I_{DD1}	Operating Current, One Back Active-Read Precharge	—	—	100	mA	**Note 2**
DDRM14	I_{DD2}	Precharge Power-Down Current	—	—	8	mA	**Note 3**
DDRM15	I_{DD3}	Precharge Stand-by Current	—	—	45	mA	**Note 2**
DDRM16	I_{DD4}	Precharge Quiet Stand-by Current	—	—	35	mA	**Note 4**
DDRM17	I_{DD5}	Active Power-Down Current	—	—	12	mA	**Note 3**
DDRM18	I_{DD6}	Active Stand-by Current	—	—	65	mA	**Note 2**
DDRM19	I_{DD7}	Operating Burst Read Current	—	—	140	mA	**Note 2**
DDRM20	I_{DD8}	Operating Burst Write Current	—	—	165	mA	**Note 2**
DDRM21	I_{DD9}	Burst Refresh Current	—	—	95	mA	**Note 2**
DDRM22	I_{DD10}	Self-Refresh Current	—	—	6	mA	**Note 5**
DDRM23	I_{DD11}	Operating Bank Interleave Read Current	—	—	200	mA	**Note 6**

Note 1: These parameters are characterized, but not tested in manufacturing. The specifications are only valid after the memory is initialized.

2: DDRCKE is high, $\overline{\text{DDRCS0}}$ is high between valid commands. Address, control, and data bus inputs are switching.

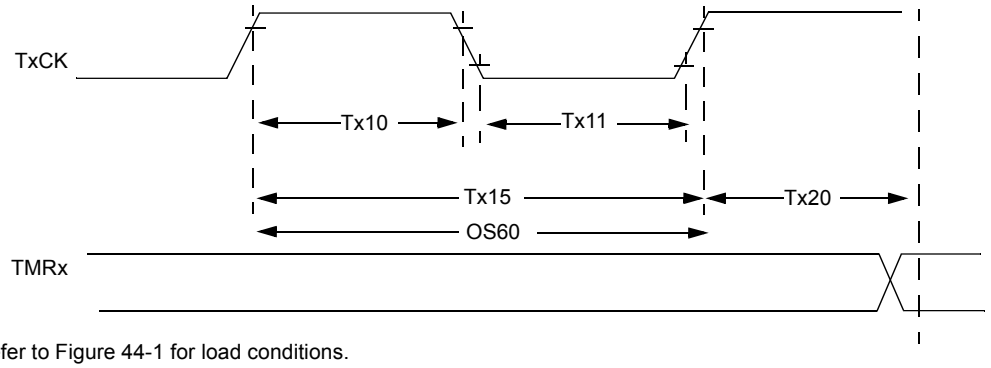
3: DDRCKE is low. Other control and address inputs are stable. Data bus inputs are floating.

4: DDRCKE is high and $\overline{\text{DDRCS0}}$ is high. Other control and address inputs are stable. Data bus inputs are floating.

5: DDRCKE is low and DDRCK/$\overline{\text{DDRCK}}$ are low. Other control and address inputs are floating. Data bus inputs are floating.

6: DDRCKE is high and $\overline{\text{DDRCS0}}$ is high between valid commands. Address bus inputs are stable. Data bus inputs are switching.

FIGURE 44-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-32: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(2)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 20 ns or 2 TPBCLK3)/N] + 30 ns	—	—	ns	V_{DDIO} > 2.7V (**Note 3**)
				[(Greater of 20 ns or 2 TPBCLK3)/N] + 50 ns	—	—	ns	V_{DDIO} < 2.7V (**Note 3**)
			Asynchronous, with prescaler	20	—	—	ns	V_{DDIO} > 2.7V
				50	—	—	ns	V_{DDIO} < 2.7V
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	50	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	—	1	TPBCLK3	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

TABLE 44-48: TEMPERATURE SENSOR SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TS10	VTS	Rate of Change	—	5	—	mV/ºC	—
TS11	TR	Resolution	-2	—	+2	ºC	—
TS12	IVTEMP	Voltage Range	0.5	—	1.5	V	—
TS13	TMIN	Minimum Temperature	—	-40	—	ºC	IVTEMP = 0.5V
TS14	TMAX	Maximum Temperature	—	160	—	ºC	IVTEMP = 1.5V

Note 1: The temperature sensor is functional at VBORIOMIN < VDDIO < VDDIOMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
44.0 "Electrical Characteristics"	The following tables were updated: • **Table 44-1: "Operating MIPS vs. Voltage"** • **Table 44-3: "Thermal Packaging Characteristics"** • **Table 44-4: "DC Temperature and Voltage Specifications"** • **Table 44-8: "DC Characteristics: Operating Current (Idd)"** • **Table 44-9: "DC Characteristics: Idle Current (Iidle)"** • **Table 44-10: "DC Characteristics: Power-Down Current (Ipd)"** • **Table 44-12: "DC Characteristics: I/O Pin Output Specifications"** • **Table 44-38: "SPIx Master Mode (CKE = 0) Timing Requirements"** • **Table 44-39: "SPIx Module Master Mode (CKE = 1) Timing Requirements"** • **Table 44-53: "USB OTG Electrical Specifications"**

Revision C (October/November 2016)

All instances of V_{DD1V8} were changed to: V_{DDR1V8} and V_{DD} were changed to V_{DDIO} throughout the data sheet.

All instances of V-Temp specifications were removed throughout the data sheet.

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology	The Operating Conditions were updated from 2.0V to 3.6V to 2.2V to 3.6V. All Device Pin Tables were updated (see Table 5 through Table 7).
1.0 "Device Overview"	Note 1 was added to the Timer1 through Timer9 and RTCC Pinout I/O Descriptions (see Table 1-7). Note 2 and the pin numbers for the Power, Ground, and Voltage Reference Pinout I/O Descriptions were updated (see Table 1-23).
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	The Recommended Minimum Connection diagram was updated (see Figure 2-1). **2.9.1.3 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations"** was added.
3.0 "CPU"	The SB bit was updated in the Configuration Register; CP0 Register 16, Select 0 (see Register 3-1).
4.0 "Memory Organization"	**4.3 "Timing Parameters"** was updated.
6.0 "Resets"	Note 1 was added to the Resets Register Map (see Table 6-1).
8.0 "Oscillator Configuration"	The DIVSPLLRDY bit was removed from the CLKSTAT register (see Table 8-2 and Register 8-8). Updated bit 5-0 center frequency values from -2% to -4% and +2% to +4% (see Register 8-2).