Microchip Technology - PIC32MZ1064DAA169T-I/HF Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1064daa169t-i-hf

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

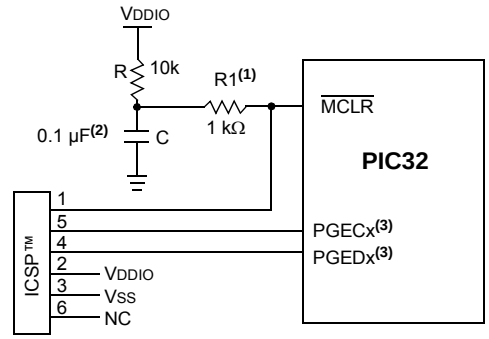
- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: 470Ω ≤ R1 ≤ 1Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.4 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For additional information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available for download from the Microchip web site, www.microchip.com:

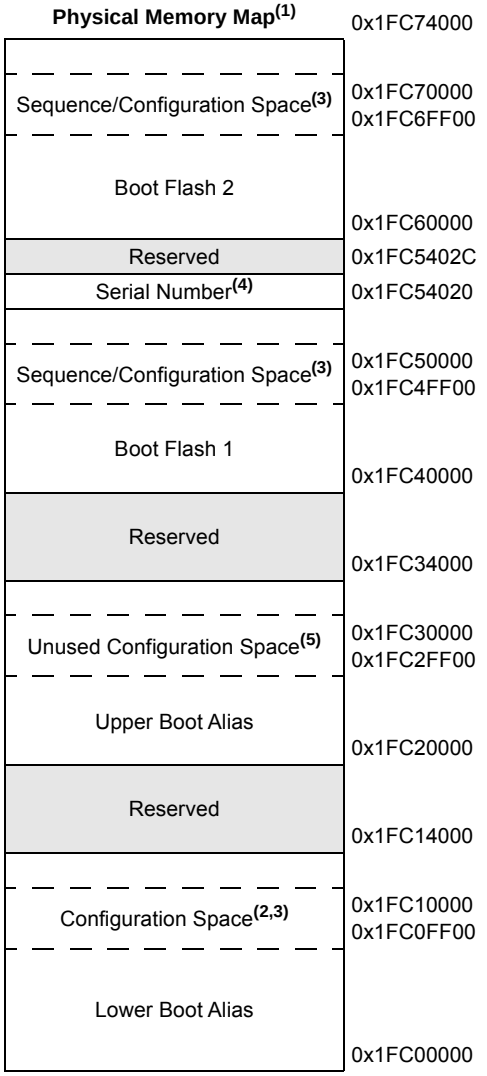
- *"Using MPLAB® ICD 3"* (poster) (DS50001765)
- *"MPLAB® ICD 3 Design Advisory"* (DS50001764)
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" (*DS50001616)
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) (DS50001749)

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer or debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

FIGURE 4-2: BOOT AND ALIAS MEMORY MAP



Note 1: Memory areas are not shown to scale.

2: Memory locations 0x1FC0FF40 through 0x1FC0FFFC are used to initialize Configuration registers (see **Section 41.0 "Special Features"**).

3: Refer to **Section 4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

4: Memory location 0x1FC54020 contains a unique device serial number (see **Section 41.0 "Special Features"**).

5: This configuration space cannot be used for executing code in the upper boot alias.

TABLE 4-2: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
System Bus(1)	0xBF8F0000	0x0000
SDHC	0xBF8E0000	0xC000
GPU		0xB000
GLCD		0xA000
DDRPHY		0x9100
DDRC		0x8000
RNG		0x6000
Crypto		0x5000
USB		0x3000
SQI1		0x2000
EBI		0x1000
Prefetch		0x0000
DSCTRL	0xBF8C0000	0x0200
RTCC		0x0000
USBCR	0xBF880000	0x4000
Ethernet		0x2000
CAN1 and CAN2		0x0000
PORTA-PORTK	0xBF860000	0x0000
CTMU	0xBF840000	0xC200
Comparator 1, 2		0xC000
ADC		0xB000
OC1-OC9		0x4000
IC1-IC9		0x2000
Timer1-Timer9		0x0000
PMP	0xBF820000	0xE000
UART1-UART6		0x2000
SPI1-SPI6		0x1000
I2C1-I2C5		0x0000
DMA	0xBF810000	0x1000
Interrupt Controller		0x0000
HLVD	0xBF800000	0x1800
PPS		0x1400
Oscillator		0x1200
CVREF		0x0E00
Deadman Timer		0x0A00
Watchdog Timer		0x0800
Flash Controller		0x0600
Configuration		0x0000

Note 1: Refer to **4.4 "System Bus Arbitration"** for important legal information.

TABLE 4-9: SYSTEM BUS VIOLATION FLAG REGISTER MAP

Virtual Address (BFxx_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8F_0510	SBFLAG0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	T0PGV0	T3PGV	T6PGV	T2PGV	T5PGV	T4PGV	T1PGV	0000
90_0510	SBFLAG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	T0PGV1	T12PGV	T11PGV	T10PGV	T9PGV	T8PGV	T7PGV	0000
91_0510	SBFLAG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T0PGV2	T15PGV	T14PGV	T13PGV	0000
92_0510	SBFLAG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	T0PGV3	T16PGV	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER (CONTINUED)

bit 6 **BFSWAP:** Boot Flash Bank Swap Control bit(3,4)
- 1 = Boot Flash Bank 2 is mapped to the lower boot region and Boot Flash Bank 1 is mapped to the upper mapped region
- 0 = Boot Flash Bank 1 is mapped to the lower boot region and Boot Flash Bank 2 is mapped to the upper mapped region

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits

These bits are only writable when WREN = 0.
- 1111 = Reserved
- •
- •
- •
- 1000 = Reserved
- 0111 = Program erase operation: erase all of program Flash memory (all pages must be unprotected, PWP<23:0> = 0x000000)
- 0110 = Upper program Flash memory erase operation: erases only the upper mapped region of program Flash (all pages in that region must be unprotected)
- 0101 = Lower program Flash memory erase operation: erases only the lower mapped region of program Flash (all pages in that region must be unprotected)
- 0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected
- 0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected
- 0010 = Quad Word (128-bit) program operation: programs the 128-bit Flash word selected by NVMADDR, if it is not write-protected
- 0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected(2)
- 0000 = No operation

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This operation results in a "no operation" (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) for information regarding ECC and Flash programming.

3: This bit can only be modified when the WREN bit = 0, the NVMKEY unlock sequence is satisfied, and the SWAPLOCK<1:0> bits (NVMCON2<7:6>) are cleared to '0'.

4: The BFSWAP value is determined by the values the user programmed Sequence Numbers in each boot panel.

REGISTER 10-10: DCHxSSA: DMA CHANNEL x SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.
Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL x DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.
Note: This must be the physical address of the destination.

REGISTER 11-5: USBIE0CSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 0) (CONTINUED)

bit 21 **SENDSTALL:** Send Stall Control bit (*Device mode*)
1 = Terminate the current transaction and transmit a STALL handshake. This bit is automatically cleared.
0 = Do not send STALL handshake.

REQPKT: IN transaction Request Control bit (*Host mode*)
1 = Request an IN transaction. This bit is cleared when the RXPKTRDY bit is set.
0 = Do not request an IN transaction

bit 20 **SETUPEND:** Early Control Transaction End Status bit (*Device mode*)
1 = A control transaction ended before the DATAEND bit has been set. An interrupt will be generated and the FIFO flushed at this time.
0 = Normal operation

This bit is cleared by writing a '1' to the SVCSETEND bit in this register.

ERROR: No Response Error Status bit (*Host mode*)
1 = Three attempts have been made to perform a transaction with no response from the peripheral. An interrupt is generated.
0 = Clear this flag. Software must write a '0' to this bit to clear it.

bit 19 **DATAEND:** End of Data Control bit (*Device mode*)
The software sets this bit when:

- Setting TXPKTRDY for the last data packet
- Clearing RXPKTRDY after unloading the last data packet
- Setting TXPKTRDY for a zero length data packet

Hardware clears this bit.

SETUPPKT: Send a SETUP token Control bit (*Host mode*)
1 = When set at the same time as the TXPKTRDY bit is set, the module sends a SETUP token instead of an OUT token for the transaction
0 = Normal OUT token operation

Setting this bit also clears the Data Toggle.

bit 18 **SENTSTALL:** STALL sent status bit (*Device mode*)
1 = STALL handshake has been transmitted
0 = Software clear of bit

RXSTALL: STALL handshake received Status bit (*Host mode*)
1 = STALL handshake was received
0 = Software clear of bit

bit 17 **TXPKTRDY:** TX Packet Ready Control bit
1 = Data packet has been loaded into the FIFO. It is cleared automatically.
0 = No data packet is ready for transmit

bit 16 **RXPKTRDY:** RX Packet Ready Status bit
1 = Data packet has been received. Interrupt is generated (when enabled) when this bit is set.
0 = No data packet has been received

This bit is cleared by setting the SVCRPR bit.

bit 15-0 **Unimplemented:** Read as '0'

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER (CONTINUED)

bit 3 **SENDMONEN:** Session End VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session End range (between 0.2V and 0.8V)
0 = Disable monitoring for VBUS in Session End range

bit 2 **USBIE:** USB General Interrupt Enable bit
1 = Enables general interrupt from USB module
0 = Disables general interrupt from USB module

bit 1 **USBRIE:** USB Resume Interrupt Enable bit
1 = Enable remote resume from suspend Interrupt
0 = Disable interrupt to a Remote Devices USB resume signaling

bit 0 **USBWKUPEN:** USB Activity Detection Interrupt Enable bit
1 = Enable interrupt for detection of activity on USB bus in Sleep mode
0 = Disable interrupt for detection of activity on USB bus in Sleep mode

TABLE 12-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1654	RPF5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF5R<3:0>				0000
1660	RPF8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF8R<3:0>				0000
1670	RPF12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG12R<3:0>				0000
1680	RPG0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1684	RPG1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
169C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG7R<3:0>				0000
16A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG8R<3:0>				0000
16A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG9R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 22-4: SQI1CON: SQI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	r-0	R/W-0
	—	—	—	—	—	—	—	SCHECK(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DDRMODE	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<7:0>							

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **Reserved:** Must be programmed as '0'

bit 24 **SCHECK:** Flash Status Check bit(1)
- 1 = Check the status of the Flash
- 0 = Do not check the status of the Flash

bit 23 **DDRMODE:** Double Data Rate Mode bit
- 1 = Set the SQI transfers to DDR mode
- 0 = Set the SQI transfers to SDR mode

bit 22 **DASSERT:** Chip Select Assert bit
- 1 = Chip Select is deasserted after transmission or reception of the specified number of bytes
- 0 = Chip Select is not deasserted after transmission or reception of the specified number of bytes

bit 21-20 **DEVSEL<1:0>:** SQI Device Select bits
- 11 = Reserved
- 10 = Reserved
- 01 = Select Device 1
- 00 = Select Device 0

bit 19-18 **LANEMODE<1:0>:** SQI Lane Mode Select bits
- 11 = Reserved
- 10 = Quad Lane mode
- 01 = Dual Lane mode
- 00 = Single Lane mode

bit 17-16 **CMDINIT<1:0>:** Command Initiation Mode Select bits

If it is Transmit, commands are initiated based on a write to the transmit register or the contents of TX buffer. If CMDINIT is Receive, commands are initiated based on reads to the read register or RX buffer availability.
- 11 = Reserved
- 10 = Receive
- 01 = Transmit
- 00 = Idle

bit 15-0 **TXRXCOUNT<15:0>:** Transmit/Receive Count bits

These bits specify the total number of bytes to transmit or received (based on CMDINIT).

Note 1: When this bit is set to '1', the SQI module uses the SQI1MEMSTAT register to control the status check command process.

REGISTER 22-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal buffer space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

REGISTER 22-21: SQI1THR: SQI THRESHOLD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	THRES<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **THRES<3:0>:** SQI Control Threshold Value bits
The SQI control threshold interrupt is asserted when the amount of space indicated by THRES<6:0> is available in the SQI control buffer.

REGISTER 22-25: SQI1XCON3: SQI XIP CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT1SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD3<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD2<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD1<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT1SCHECK:** Flash Initialization 1 Command Status Check bit
1 = Check the status after executing the INIT1 commands
0 = Do not check the status

bit 27-26 **INIT1COUNT<1:0>:** Flash Initialization 1 Command Count bits
11 = INIT1CMD1, INIT1CMD2, and INIT1CMD3 are sent
10 = INIT1CMD1 and INIT1CMD2 are sent, but INIT1CMD3 is still pending
01 = INIT1CMD1 is sent, but INIT1CMD2 and INIT1CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT1TYPE<1:0>:** Flash Initialization 1 Command Type bits
11 = Reserved
10 = INIT1 commands are sent in Quad Lane mode
01 = INIT1 commands are sent in Dual Lane mode
00 = INIT1 commands are sent in Single Lane mode

bit 24-16 **INIT1CMD3<7:0>:** Flash Initialization Command 3 bits
Third command of the Flash initialization.

bit 15-8 **INIT1CMD2<7:0>:** Flash Initialization Command 2 bits
Second command of the Flash initialization.

bit 7-0 **INIT1CMD1<7:0>:** Flash Initialization Command 1 bits
First command of the Flash initialization.

Note: Some Flash devices require write enable and sector unprotect commands before write/read operations and this register is useful in working with those Flash types (XIP mode only)

REGISTER 29-10: ADCCSS1: ADC COMMON SCAN SELECT REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CSS31:CSS0:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

Note 1: In addition to setting the appropriate bits in this register, Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSS*x* bits. Refer to the bit descriptions in the ADCTRGx registers for selecting the STRIG option.

2: If a Class 1 or Class 2 input is included in the scan by setting the CSSx bit to '1' and by setting the TRGSRCx<4:0> bits to STRIG mode ('0b11), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

REGISTER 30-4: CiVEC: CAN INTERRUPT CODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	FILHIT<4:0>				
7:0	U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	—	ICODE<6:0>(1)						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bit
11111 = Filter 31
11110 = Filter 30
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits(1)
1001000-1111111 = Reserved
1001000 = Invalid message received (IVRIF)
1000111 = CAN module mode change (MODIF)
1000110 = CAN timestamp timer (CTMRIF)
1000101 = Bus bandwidth error (SERRIF)
1000100 = Address error interrupt (SERRIF)
1000011 = Receive FIFO overflow interrupt (RBOVIF)
1000010 = Wake-up interrupt (WAKIF)
1000001 = Error Interrupt (CERRIF)
1000000 = No interrupt
0100000-0111111 = Reserved
0011111 = FIFO31 Interrupt (CiFSTAT<31> set)
0011110 = FIFO30 Interrupt (CiFSTAT<30> set)
•
•
•
0000001 = FIFO1 Interrupt (CiFSTAT<1> set)
0000000 = FIFO0 Interrupt (CiFSTAT<0> set)

Note 1: These bits are only updated for enabled interrupts.

REGISTER 31-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **PMCS<15:8>:** Pattern Match Checksum 1 bits

bit 7-0 **PMCS<7:0>:** Pattern Match Checksum 0 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 31-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PMO<15:0>:** Pattern Match Offset 1 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 36-3: GLCDBGCOLOR: GRAPHICS LCD CONTROLLER BACKGROUND COLOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RED<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALPHA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **RED<7:0>:** Color Red as Background bits
These bits specify that the color red is to be used as the background color.

bit 23-16 **GREEN<7:0>:** Color Green as Background bits
These bits specify that the color green is to be used as the background color.

bit 15-8 **BLUE<7:0>:** Color Blue as Background bits
These bits specify that the color blue is to be used as the background color.

bit 7-0 **ALPHA<7:0>:** Color Alpha as Background bits
These bits specify that the color alpha is to be used as the background color.

Note: If all of the bits in this register are set (RED, GREEN, BLUE and ALPHA), RGBA color is used as the background.

REGISTER 36-4: GLCDRES: GRAPHICS LCD CONTROLLER RESOLUTION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESX<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **RESX<10:0>:** X Dimension Pixel Resolution bits
These bits specify the pixel resolution for the X dimension.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **RESY<10:0>:** Y Dimension Pixel Resolution bits
These bits specify the pixel resolution for the Y dimension.

REGISTER 41-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitoring Selection Configuration bits

11 = Software Clock switching is enabled and clock monitoring is enabled
10 = Software Clock switching is disabled and clock monitoring is enabled
01 = Software Clock switching is enabled and clock monitoring is disabled
00 = Software Clock switching is disabled and clock monitoring is disabled

bit 13-11 **Reserved:** Write as '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit

1 = CLKO output is disabled
0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits

11 = POSC is disabled
10 = HS Oscillator mode is selected
01 = Reserved
00 = EC mode is selected (this mode must not be selected if the POSCAGC bit (DEVCFG0/ADEVCFG0<27>) is equal to '1')

bit 7 **IESO:** Internal External Switchover bit

1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **FSOSCEN:** Secondary Oscillator Enable bit

1 = Enable SOSC
0 = Disable SOSC

bit 5-3 **DMTINV<2:0>:** Deadman Timer Count Window Interval bits

111 = Window/Interval value is 127/128 counter value
110 = Window/Interval value is 63/64 counter value
101 = Window/Interval value is 31/32 counter value
100 = Window/Interval value is 15/16 counter value
011 = Window/Interval value is 7/8 counter value
010 = Window/Interval value is 3/4 counter value
001 = Window/Interval value is 1/2 counter value
000 = Window/Interval value is zero

REGISTER 41-9: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	ICACLK(1)	OCACLK(1)
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	IOLOCK(1)	PMDLOCK(1)	PGLOCK(1)	—	—	USBSSEN(1)
7:0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	U-0	R/W-1
	IOANCPEN	—	ECCCON<1:0>		JTAGEN(2)	TROEN	—	TDOEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-18 **Unimplemented:** Read as '0'

bit 17 **ICACLK:** Input Capture Alternate Clock Selection bit(1)
- 1 = Input Capture modules use an alternative Timer pair as their timebase clock
- 0 = All Input Capture modules use Timer2/3 as their timebase clock

bit 16 **OCACLK:** Output Compare Alternate Clock Selection bit(1)
- 1 = Output Compare modules use an alternative Timer pair as their timebase clock
- 0 = All Output Compare modules use Timer2/3 as their timebase clock

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)
- 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
- 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)
- 1 = Peripheral module is locked. Writes to PMD registers is not allowed.
- 0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11 **PGLOCK:** Permission Group Lock bit(1)
- 1 = Permission Group registers are locked. Writes to PG registers are not allowed.
- 0 = Permission Group registers are not locked. Writes to PG registers are allowed.

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **USBSSEN:** USB Suspend Sleep Enable bit(1)

Enables features for USB PHY clock shutdown in Sleep mode.
- 1 = USB PHY clock is shut down when Sleep mode is active
- 0 = USB PHY clock continues to run when Sleep is active

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: The JTAGEN bit is only available at run-time when the JTAGEN (DEVCFG0<2>) fuse bit is set at start-up.

44.1 DC Characteristics

TABLE 44-1: OPERATING MIPS VS. VOLTAGE

Characteristic	V_{DDIO} Range (in Volts) (Note 1)	V_{DDCORE} Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comments
				PIC32MZ DA Devices	
DC5	2.2V-3.6V	1.7V-1.9V	-40°C to +85°C	200 MHz	—

Note 1: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

TABLE 44-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DDIO} \times (I_{DD} - S\ I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = S\ (\{V_{DDIO} - V_{OH}\} \times I_{OH}) + S\ (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 44-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 169-pin LFBGA (11x11x1.4 mm)	θ_{JA}	25	—	°C/W	**1**
Package Thermal Resistance, 169-pin LFBGA (11x11x1.56 mm)	θ_{JA}	24	—	°C/W	**1,2**
Package Thermal Resistance, 176-pin LQFP (20x20x1.45 mm)	θ_{JA}	17	—	°C/W	**1**
Package Thermal Resistance, 176-pin LQFP (20x20x1.45 mm)	θ_{JA}	19	—	°C/W	**1,2**
Package Thermal Resistance, 288-pin LFBGA (15x15x1.4 mm)	θ_{JA}	22	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-$_{JA}$ (θ_{JA}) numbers are achieved by package simulations.

2: Devices with internal DDR2 SDRAM.

44.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ DA device AC characteristics and timing parameters.

FIGURE 44-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

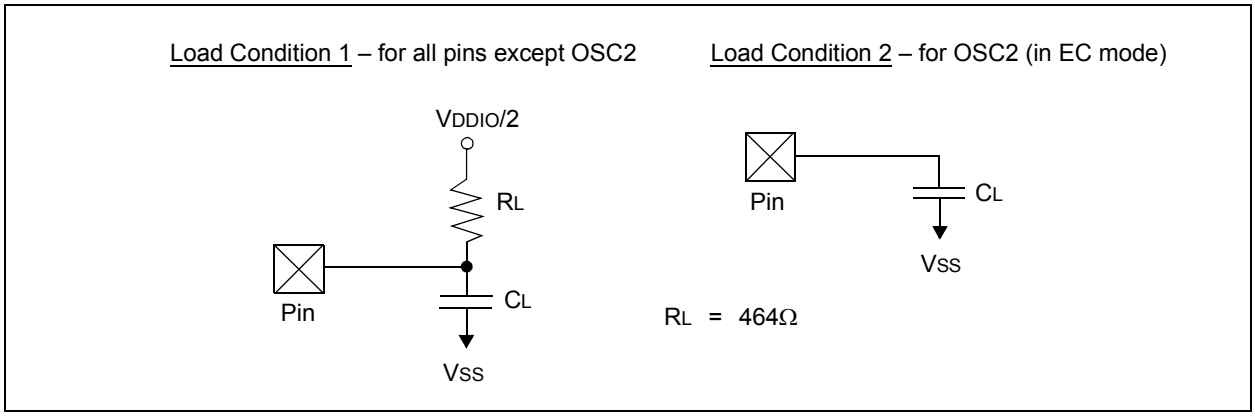


TABLE 44-22: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO56	C_L	All I/O pins	—	—	50	pF	EC mode for OSC2
DO58	C_B	SCLx, SDAx	—	—	400	pF	In I^2C mode
DO59	C_{SQI}	All SQI pins	—	—	10	pF	—

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 44-57: SD HOST CONTROLLER DEFAULT MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD20	tSDCK	Clock Frequency	—	—	25	MHz	—
SD21	tDUTY	Duty Cycle	—	50	—	%	—
SD22	tHIGH	Clock High Time	10	—	—	ns	—
SD23	tLOW	Clock Low Time	10	—	—	ns	—
SD24	tRISE	Clock Rise Time	—	10	—	ns	—
SD25	tFALL	Clock Fall Time	—	10	—	ns	—
SD26	tSETUP	Input Setup Time	5	—	—	ns	—
SD27	tHOLD	Input Hold Time	5	—	—	ns	—

TABLE 44-58: SD HOST CONTROLLER HIGH-SPEED MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD30	tSDCK	Clock Frequency	—	—	50	MHz	—
SD31	tDUTY	Duty Cycle	—	50	—	%	—
SD32	tHIGH	Clock High Time	7	—	—	ns	—
SD33	tLOW	Clock Low Time	7	—	—	ns	—
SD34	tRISE	Clock Rise Time	—	3	—	ns	—
SD35	tFALL	Clock Fall Time	—	3	—	ns	—
SD36	tSETUP	Input Setup Time	6	—	—	ns	—
SD37	tHOLD	Input Hold Time	2	—	—	ns	—