Microchip Technology - PIC32MZ1064DAB169-I/HF Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1064dab169-i-hf

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
PORTK						
RK0	K12	137	P16	I/O	ST	PORTK is a bidirectional I/O port
RK1	J11	136	R18	I/O	ST	
RK2	H11	135	R17	I/O	ST	
RK3	L13	134	R16	I/O	ST	
RK4	H10	133	P15	I/O	ST	
RK5	J10	132	R15	I/O	ST	
RK6	M13	131	T18	I/O	ST	
RK7	M12	130	T17	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-7: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Timer1 through Timer9						
T1CK	D13	161	H18	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar						
RTCC(1)	H3	79	V5	O	—	Real-Time Clock Alarm/Seconds Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: RTCC pin function in not available during VBAT operation.

TABLE 4-8: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS (CONTINUED)

Target Protection Number	Target Description (see Note 5)	SBTxREGy Register (see Note 7)							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
6	External Memory via EBI and EBI Module(6)	SBT6REG0	R	0x20000000	R	64 MB	—	0	SBT6RD0	R/W(1)	SBT6WR0	R/W(1)
		SBT6REG2	R	0x1F8EC000	R	4 KB	0	1	SBT6RD2	R/W(1)	SBT6WR2	R/W(1)
7	System Controller	SBT7REG0	R	0x1F800000	R	—	—	0	SBT7RD0	R/W(1)	SBT7WR0	R/W(1)
	Flash Controller	SBT7REG1	R/W	R/W	R/W	R/W	—	3	SBT7RD1	R/W(1)	SBT7WR1	R/W(1)
	DMT/WDT CVREF PPS Input PPS Output Interrupts DMA	SBT7REG2	R/W	R/W	R/W	R/W	0	1	SBT7RD2	R/W(1)	SBT7WR2	R/W(1)
8	SPI1-SPI6	SBT8REG0	R	0x1F820000	R	64 KB	—	0	SBT8RD0	R/W(1)	SBT8WR0	R/W(1)
	I2C1-I2C5 UART1-UART6 PMP	SBT8REG1	R/W	R/W	R/W	R/W	—	3	SBT8RD1	R/W(1)	SBT8WR1	R/W(1)
9	Timer1-Timer9	SBT9REG0	R	0x1F840000	R	64 KB	—	0	SBT9RD0	R/W(1)	SBT9WR0	R/W(1)
	IC1-IC9 OC1-OC9 ADC Comparator 1 Comparator 2	SBT9REG1	R/W	R/W	R/W	R/W	—	3	SBT9RD1	R/W(1)	SBT9WR1	R/W(1)
10	PORTA-PORTK	SBT10REG0	R	0x1F860000	R	64 KB	—	0	SBT10RD0	R/W(1)	SBT10WR0	R/W(1)
		SBT10REG1	R/W	R/W	R/W	R/W	—	3	SBT10RD1	R/W(1)	SBT10WR1	R/W(1)
11	CAN1	SBT11REG0	R	0x1F880000	R	64 KB	—	0	SBT11RD0	R/W(1)	SBT11WR0	R/W(1)
	CAN2 Ethernet	SBT11REG1	R/W	R/W	R/W	R/W	—	3	SBT11RD1	R/W(1)	SBT11WR1	R/W(1)
12	GLCD	SBT12REG0	R	0x1F8EA000	R	4 KB	—	0	SBT12RD0	R/W(1)	SBT12WR0	R/W(1)
	GPU		R	0x1F8EB000	R	4 KB	—	0		R/W(1)		R/W(1)
	DDR2PHY		R	0x1F8E9000	R	4 KB	—	0		R/W(1)		R/W(1)
	DDR2SFR		R	0x1F8E8000	R	4 KB	—	0		R/W(1)		R/W(1)
13	External Memory via SQI1 and SQI1	SBT13REG0	R	0x30000000	R	64 MB	—	0	SBT13RD0	R/W(1)	SBT13WR0	R/W(1)
		SBT13REG1	R	0x1F8E2000	R	4 KB	—	3	SBT13RD1	R/W(1)	SBT13WR1	R/W(1)

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Map (Figure 4-1) for specific device memory sizes and start addresses.

5: See Table 4-2 for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

7: The 'x' in the SBTxREGy, SBTxRDy, and SBTxWRy registers represents the target protection number and not the actual target number (e.g., for SQI 'x' = 13 and not 11, whereas 11 is the actual target number).

TABLE 4-16: SYSTEM BUS TARGET PROTECTION GROUP 6 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9820	SBT6ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9824	SBT6ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9828	SBT6ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT6ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT6ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT6REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9850	SBT6RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9858	SBT6WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9860	SBT6REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9870	SBT6RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9878	SBT6WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

REGISTER 6-1: RCON: RESET CONTROL REGISTER

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MZ DA family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MZ DA oscillator system has the following modules and features:

- Five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown with dedicated Back-up FRC (BFRC)
- Dedicated On-Chip PLL for DDR2 and USB modules
- Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility

A block diagram of the oscillator system is provided in Figure 8-1. The clock distribution is shown in Table 8-1.

REGISTER 11-2: USBCSR1: USB CONTROL STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	U-0
	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIE:EP1TXIE:** Endpoint 'n' Transmit Interrupt Enable bits
1 = Endpoint Transmit interrupt events are enabled
0 = Endpoint Transmit interrupt events are not enabled

bit 16 **EP0IE:** Endpoint 0 Interrupt Enable bit
1 = Endpoint 0 interrupt events are enabled
0 = Endpoint 0 interrupt events are not enabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7-1 **EP7RXIF:EP1RXIF:** Endpoint 'n' RX Interrupt bit
1 = Endpoint has a receive event to be serviced
0 = No interrupt event

bit 0 **Unimplemented:** Read as '0'

14.2 Timer2-Timer9 Control Registers

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0210	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0220	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0400	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0410	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0420	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0600	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0610	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0620	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0800	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0810	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0820	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF
0A00	T6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0A10	TMR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0A20	PR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0C00	T7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 18-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value 0x5743 to these bits using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The Watchdog Timer module is enabled
0 = The Watchdog Timer module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Watchdog Timer Postscaler Value in Run Mode bits
In Run mode, these bits are set to the values of the WDTPS<4:0> Configuration bits in DEVCFG1.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-1 **SLPDIV<4:0>:** Watchdog Timer Postscaler Value in Sleep Mode bits
In Sleep mode, these bits are set to the values of the SWDTPS <4:0> Configuration bits in DEVCFG4.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

Note 1: This bit only has control when FWDTEN (DEVCFG1<23>) = 0.

REGISTER 22-2: SQI1XCON2: SQI XIP CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MODECODE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-10 **DEVSEL<1:0>:** Device Select bits
- 11 = Reserved
- 10 = Reserved
- 01 = Device 1 is selected
- 00 = Device 0 is selected

bit 9-8 **MODEBYTES<1:0>:** Mode Byte Cycle Enable bits
- 11 = Three cycles
- 10 = Two cycles
- 01 = One cycle
- 00 = Zero cycles

bit 7-0 **MODECODE<7:0>:** Mode Code Value bits

These bits contain the 8-bit code value for the mode bits.

26.0 EXTERNAL BUS INTERFACE (EBI)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 47. "External Bus Interface (EBI)"**, which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

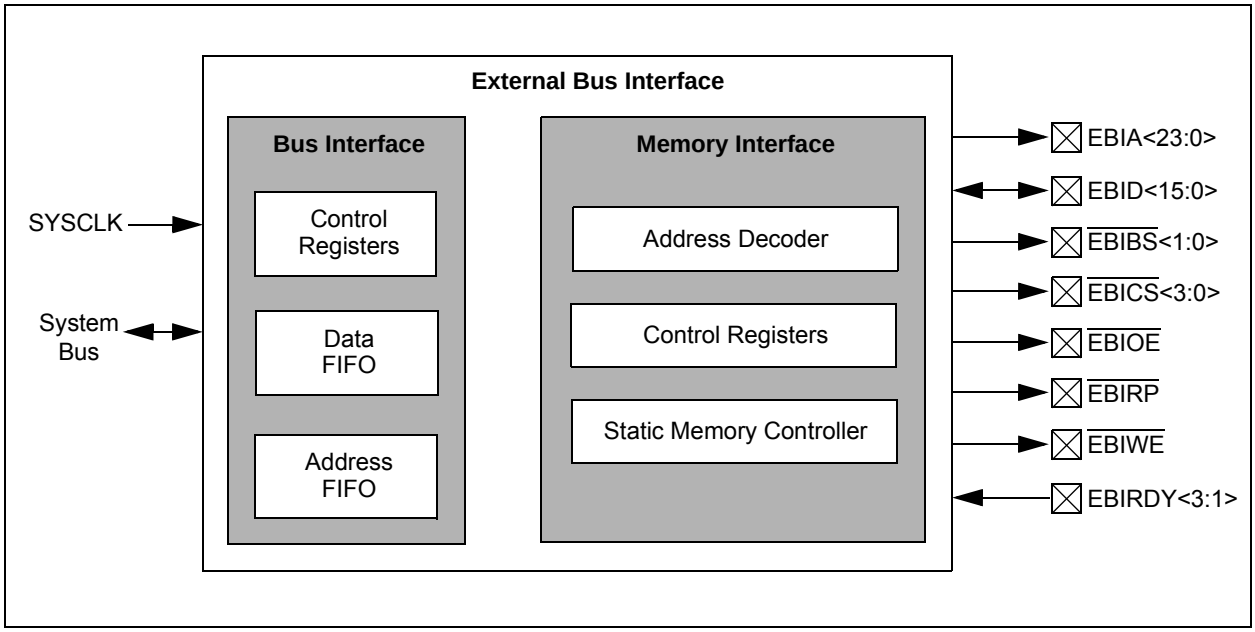
The External Bus Interface (EBI) module provides a high-speed, convenient way to interface external parallel memory devices to the PIC32MZ DA family device.

With the EBI module, it is possible to connect asynchronous SRAM and NOR Flash devices, as well as non-memory devices such as camera sensors and LCDs.

Note 1: Once the EBI module is configured, external devices will be memory mapped and can be access from KSEG2 memory space (see Figure 4-1 through Figure 4-2 in **Section 4.0 "Memory Organization"** for more information). The MMU must be enabled and the TLB must be set up to access this memory (see **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"* for more information).

2: When using the EBI module, Graphics LCD (GLCD) Controller functionality is not available, as most of the I/O between the EBI module and the GLCD is shared.

FIGURE 26-1: EBI SYSTEM BLOCK DIAGRAM



REGISTER 27-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BDPADDR<31:0>:** Current Buffer Descriptor Process Address Status bits
These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 27-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** DMA Base Address Status bits
These bits contain the base address of the DMA controller. After a reset, a fetch starts from this address.

TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
BA80	ADCDATA32	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA84	ADCDATA33	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA88	ADCDATA34	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA8C	ADCDATA35	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA90	ADCDATA36	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA94	ADCDATA37	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA98	ADCDATA38	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA9C	ADCDATA39	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAA0	ADCDATA40	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAA4	ADCDATA41	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAA8	ADCDATA42	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAAC	ADCDATA43	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 29-17: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC3<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC2<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC1<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC3<4:0>:** Trigger Source for Conversion of Analog Input AN3 Select bits
11111 = Reserved
11110 = Reserved
11101 = CTMU Event
11100 = Reserved
•
•
•
01110 = Reserved
01101 = CTMU Event
01100 = Comparator 2 (C2OUT) (1)
01011 = Comparator 1 (C1OUT) (1)
01010 = OCMP5 (1)
01001 = OCMP3 (1)
01000 = OCMP1 (1)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC2<4:0>:** Trigger Source for Conversion of Analog Input AN2 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC1<4:0>:** Trigger Source for Conversion of Analog Input AN1 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC0<4:0>:** Trigger Source for Conversion of Analog Input AN0 Select bits
See bits 28-24 for bit value definitions.

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 "Output Compare"** and Figure 32-1 in **32.0 "Comparator"** for more information.

REGISTER 29-24: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Unimplemented:** Read as '0'

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

REGISTER 30-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

TABLE 36-1: GRAPHICS LCD CONTROLLER REGISTER MAP (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0	All Resets
A054	GLCD L1START	31:16	—	—	—	—	STARTX<10:0>												0000
		15:0	—	—	—	—	STARTY<10:0>												0000
A058	GLCD L1SIZE	31:16	—	—	—	—	SIZEX<10:0>												0000
		15:0	—	—	—	—	SIZEY<10:0>												0000
A05C	GLCD L1BADDR	31:16	BASEADDR<31:16>																0000
		15:0	BASEADDR<15:0>																0000
A060	GLCD L1STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRIDE<15:0>																0000
A064	GLCD L1RES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A070	GLCD L2MODE	31:16	LAYEREN	DISA BIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>								0000
		15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>				0000
A074	GLCD L2START	31:16	—	—	—	—	STARTX<10:0>												0000
		15:0	—	—	—	—	STARTY<10:0>												0000
A078	GLCD L2SIZE	31:16	—	—	—	—	SIZEX<10:0>												0000
		15:0	—	—	—	—	SIZEY<10:0>												0000
A07C	GLCD L2BADDR	31:16	BASEADDR<31:16>																0000
		15:0	BASEADDR<15:0>																0000
A080	GLCD L2STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRIDE<15:0>																0000
A084	GLCDL2RES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A0F8	GLCDINT	31:16	IRQCON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HSYNCINT	VSYNCINT	0001
A0FC	GLCDSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LROW	—	VSYNC	HSYNC	DE	ACTIVE	0000
A400 through A7FC	GLCDCLUTx ('x' = 0-255)	31:16	—	—	—	—	—	—	—	—	RED<7:0>								0000
		15:0	GREEN<7:0>								BLUE<7:0>								0000
A800 through A9FC	GLCD CURDATAx ('x' = 0-127)	31:16	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				0000
		15:0	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				0000
AA00 through AA40	GLCD CURLUTx ('x' = 0-15)	31:16	—	—	—	—	—	—	—	—	RED<7:0>								0000
		15:0	GREEN<7:0>								BLUE<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: For the PIXELxy bits, x = 0-31 and y = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

REGISTER 36-12: GLCDLxBADDR: GRAPHICS LCD CONTROLLER LAYER 'x' BASE ADDRESS REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Base Address of the Framebuffer bits
These bits specify the base address of the framebuffer.

REGISTER 36-13: GLCDLxSTRIDE: GRAPHICS LCD CONTROLLER LAYER 'x' STRIDE REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRIDE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRIDE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **STRIDE<15:0>:** Layer Stride bits
These bits specify the distance from line to line in bytes.

REGISTER 39-4: SDHCRESPx: SDHC RESPONSE REGISTER 'x' ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RESP<31:0>:** Response bits

These bits indicate the bit positions of Responses [31:0] defined in the *"SD Host Controller Simplified Specification* (version 2.00). Refer to Table 39-2 for full bit definitions.

TABLE 39-2: RESPONSE BIT DEFINITION FOR EACH RESPONSE TYPE

Response Type (see Note 1)	Response Meaning	Response Register
R1, R1b (normal response)	Card status	SDHCRESP0<31:0>
R1b (Auto CMD12 response)	Card status for Auto CMD12	SDHCRESP3<31:0>
R2 (CID, CSD register)	CID or CSD register	SDHCRESP0<31:0> SDHCRESP1<31:0> SDHCRESP2<31:0> SDHCRESP3<31:0>
R3 (OCR register)	OCR register for memory	SDHCRESP0<31:0>
R4 (OCR register)	OCR register for I/O, etc.	SDHCRESP0<31:0>
R5, R5b	SDIO response	SDHCRESP0<31:0>
R6 (published RCA response)	New published RCA<31:16>, etc.	SDHCRESP0<31:0>

Note 1: For additional information, refer to the "*SD Host Controller Simplified Specification"* (version 2.00), the "*Physical Layer Simplified Specification"* (version 2.00), and the *"SDIO Simplified Specification"* (version 2.00). These documents are available for download by visiting the SD Association web site at: http://www.sdcard.org/downloads/pls/simplified_specs/archive/index.html

40.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MZ DA devices include two features to prevent alterations to enabled or disabled peripherals:

- Control Register Lock Sequence
- Configuration Bit Select Lock

40.4.1.1 Control Register Lock

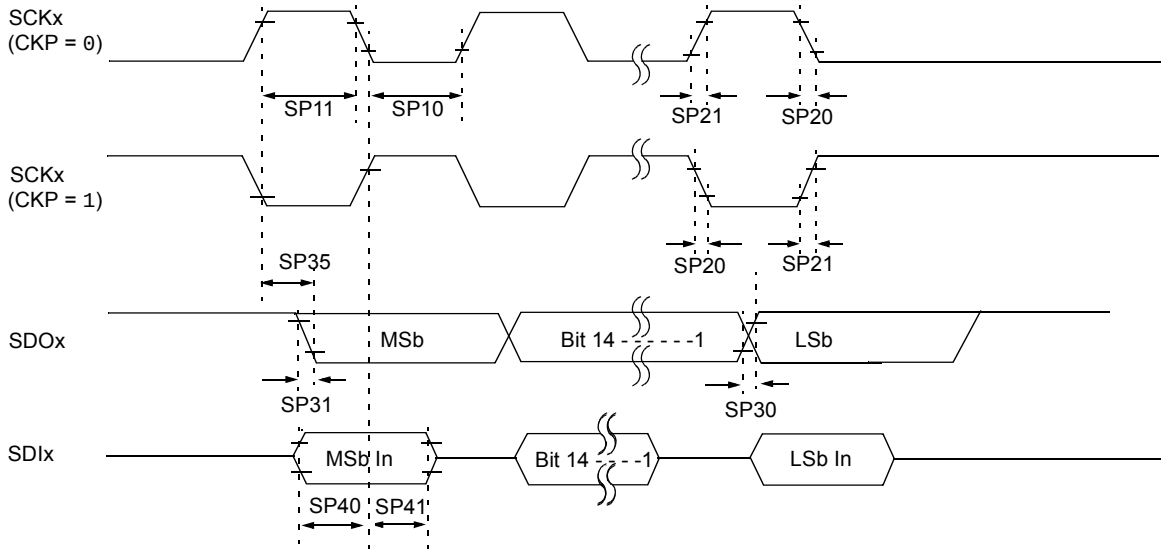
Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting the PMDLOCK bit prevents writes to the control registers and clearing the PMDLOCK bit allows writes.

To set or clear the PMDLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

40.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If the PMDLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

FIGURE 44-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.