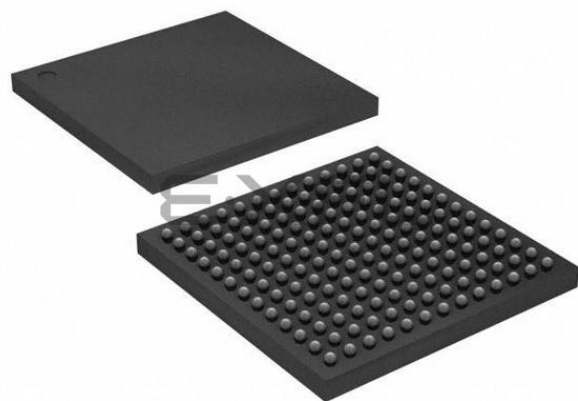




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1064dab169t-i-hf

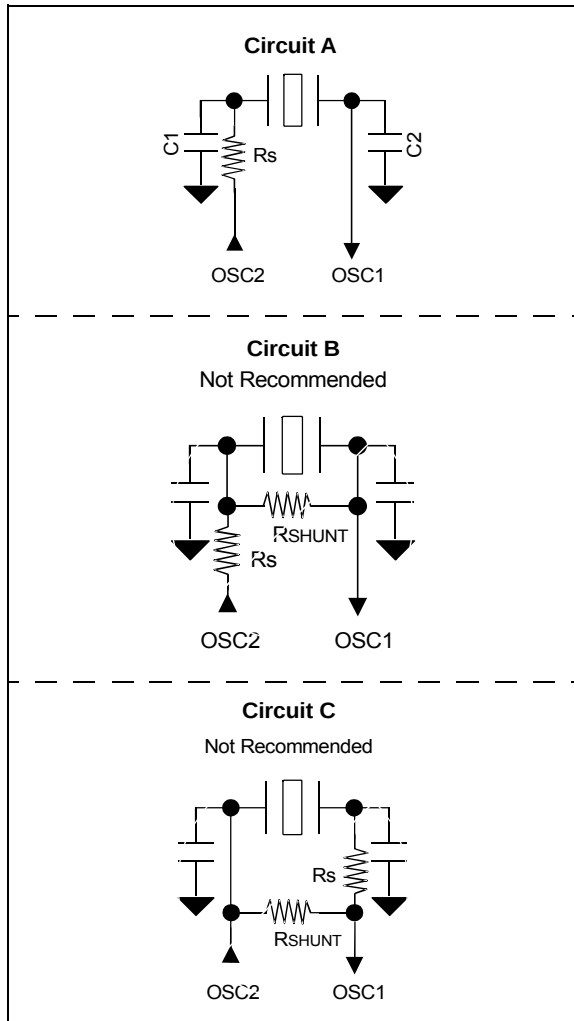
PIC32MZ Graphics (DA) Family

TABLE 7: PIN NAMES FOR 288-PIN DEVICES (CONTINUED)

288-PIN LFBGA (BOTTOM VIEW)			
		A1	V1
			N6
PIC32MZ1025DAA288 PIC32MZ1025DAB288 PIC32MZ1064DAA288 PIC32MZ1064DAB288 PIC32MZ2025DAA288 PIC32MZ2025DAB288 PIC32MZ2064DAA288 PIC32MZ2064DAB288		F6	N13
		F13	V18
		A18	
Polarity Indicator			
Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
N15	EBIA4/AN36/PMA4/RH7	T5	No Connect
N16	SDWP/EBIRP/RH2	T6	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3
N17	EBIA0/PMA0/RJ15	T7	GD16/EBID8/RPF5/SCL5/PMD8/RF5
N18	GD8/EBID11/PMD11/RJ14	T8	GD4/EBIA9/RPG1/PMA9/RG1
P1	DDRA10	T9	EBID3/RPE3/PMD3/RE3
P2	DDRCAS	T10	ERXD2/RH6
P3	DDRA4	T11	ECOL/RH10
P4	RPF8/SCL3/RF8	T12	ETXD3/RH1
P15	GD13/EBIA18/RK4	T13	ETXD1/RJ9
P16	GD23/EBIA16/RK0	T14	No Connect
P17	EBIRDY2/AN37/RH11	T15	ETXCLK/RPD7/RD7
P18	AN35/RH3	T16	RPA14/SCL1/RA14
R1	DDRA0	T17	GD19/EBIA21/RK7
R2	DDRA3	T18	GD15/EBIA20/RK6
R3	DDRA9	U1	DDRA6
R4	VSS1V8	U2	DDRA8
R5	MCLR	U3	DDRA13
R6	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2	U4	DDRBA2
R7	Vss	U5	GD7/EBIA12/RPD12/PMA12/RD12
R8	Vss	U6	GD2/EBID15/RPD9/PMD15/RD9
R9	VDDIO	U7	GD5/EBIA10/RPF1/PMA10/RF1
R10	VDDIO	U8	ERXERR/RPF3/RF3
R11	VDDCORE	U9	GD17/EBID9/RPF4/SDA5/PMD9/RF4
R12	VDDIO	U10	ERXD1/RH5
R13	VDDIO	U11	ECRS/RH12
R14	VDDIO	U12	ERXD0/RH8
R15	GD14/EBIA19/RK5	U13	ERXCLK/ERECLK/RJ11
R16	GD12/EBIA17/RK3	U14	EMDIO/RJ1
R17	EBIA3/AN11/PMA3/RK2	U15	EMDC/RPD11/RD11
R18	EBIA1/AN38/PMA1/RK1	U16	RPA15/SDA1/RA15
T1	DDRA5	U17	EBIRDY1/SDA2/RA3
T2	DDRA7	U18	SCL2/RA2
T3	DDRA12	V1	No Connect
T4	DDRA14	V2	DDRA11

- Note** 1: The RPN pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and 12.4 “Peripheral Pin Select (PPS)” for restrictions.
- 2: Every I/O port pin (RAX-RKx) can be used as a change notification pin (CNAx-CNKx). See 12.0 “I/O Ports” for more information.
- 3: Shaded pins are 5V tolerant.
- 4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.
- 5: This pin is a No Connect when DDR is not connected in the system.
- 6: These pins are restricted to input functions only.

FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS



Note: For recommended resistor values versus crystal/frequency, Refer to the "PIC32MK GP/MC Family Silicon Errata and Data Sheet Clarification" (DS80000737), which is available for download from the Microchip web site (www.microchip.com).

2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to VSS through a 1k to 10k resistor and configuring the pin as an input.

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The MIPS architecture defines that the result of a multiply or divide operation be placed in one of four pairs of HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFL0) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFL0 instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

The MDU also implements various shift instructions operating on the HI/LO register and multiply instructions as defined in the DSP ASE. The MDU supports all of the data types required for this purpose and includes three extra HI/LO registers as defined by the ASE.

Table 3-2 lists the latencies and repeat rates for the DSP multiply and dot-product operations. The approximate latencies and repeat rates are listed in terms of pipeline clocks.

TABLE 3-2: DSP-RELATED LATENCIES AND REPEAT RATES

Op code	Latency	Repeat Rate
Multiply and dot-product without saturation after accumulation	5	1
Multiply and dot-product with saturation after accumulation	5	1
Multiply without accumulation	5	1

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation and cache protocols, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as cache size and set associativity, and the presence of options like microMIPS, is also available by accessing the CP0 registers, listed in Table 3-3.

TABLE 3-3: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0	Index	Index into the TLB array (microAptiv MPU only).
1	Random	Randomly generated index into the TLB array (microAptiv MPU only).
2	EntryLo0	Low-order portion of the TLB entry for even-numbered virtual pages (microAptiv MPU only).
3	EntryLo1	Low-order portion of the TLB entry for odd-numbered virtual pages (microAptiv MPU only).
4	Context/ UserLocal	Pointer to the page table entry in memory (microAptiv MPU only). User information that can be written by privileged software and read via the RDHWR instruction.
5	PageMask/ PageGrain	PageMask controls the variable page sizes in TLB entries. PageGrain enables support of 1 KB pages in the TLB (microAptiv MPU only).
6	Wired	Controls the number of fixed (i.e., wired) TLB entries (microAptiv MPU only).
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-privileged mode.
8	BadVAddr	Reports the address for the most recent address-related exception.
9	Count	Processor cycle count.
10	EntryHi	High-order portion of the TLB entry (microAptiv MPU only).
11	Compare	Core timer interrupt control.

PIC32MZ Graphics (DA) Family

FIGURE 4-1: PIC32MZ DA FAMILY MEMORY MAP

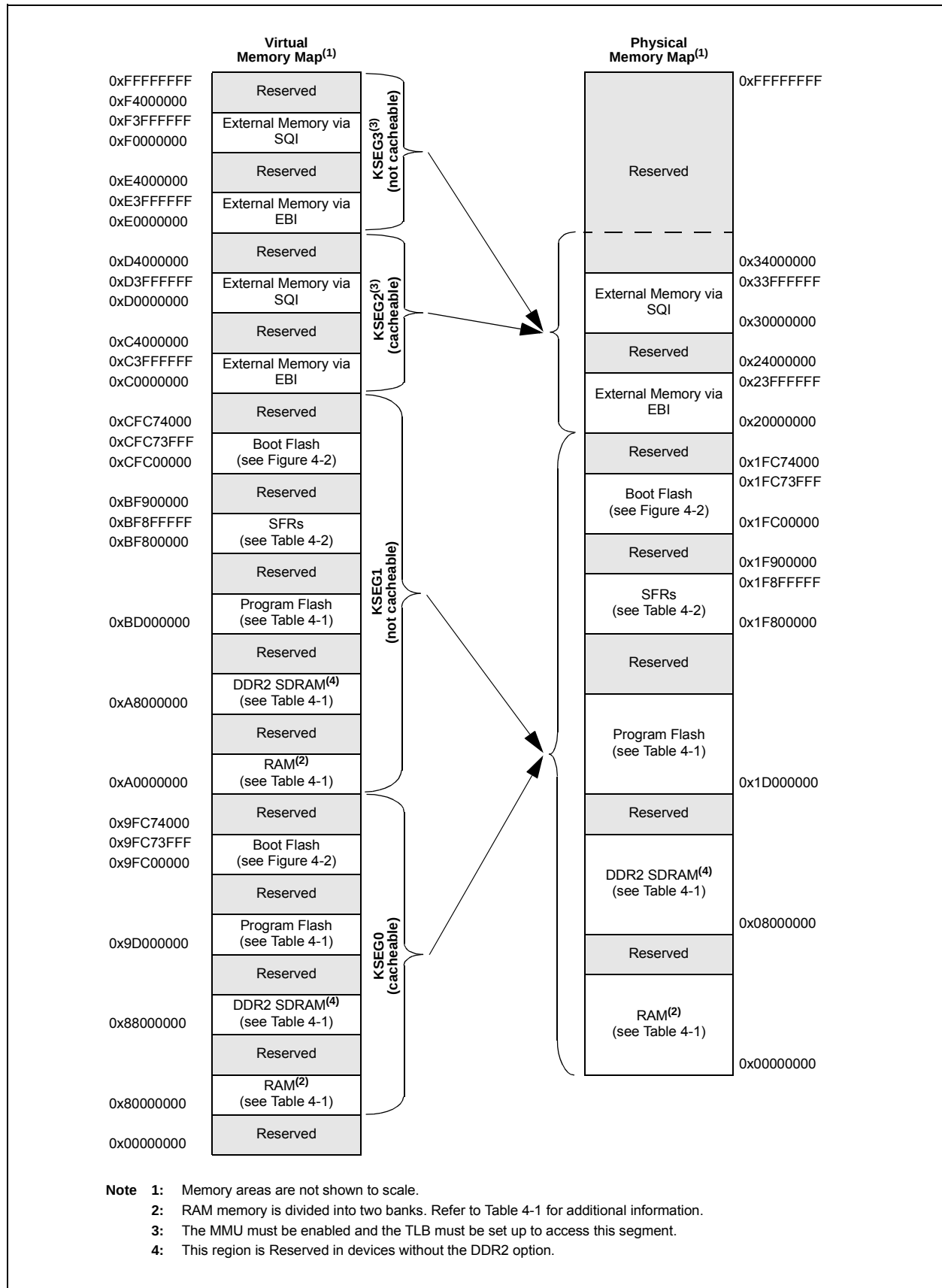


TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Digital Filter 1	_ADC_DF1_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes
ADC Digital Filter 2	_ADC_DF2_VECTOR	53	OFF053<17:1>	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
ADC Digital Filter 3	_ADC_DF3_VECTOR	54	OFF054<17:1>	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
ADC Digital Filter 4	_ADC_DF4_VECTOR	55	OFF055<17:1>	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes
ADC Digital Filter 5	_ADC_DF5_VECTOR	56	OFF056<17:1>	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
ADC Digital Filter 6	_ADC_DF6_VECTOR	57	OFF057<17:1>	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
ADC Fault	_ADC_FAULT_VECTOR	58	OFF058<17:1>	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	Yes
ADC Data 0	_ADC_DATA0_VECTOR	59	OFF059<17:1>	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
ADC Data 1	_ADC_DATA1_VECTOR	60	OFF060<17:1>	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
ADC Data 2	_ADC_DATA2_VECTOR	61	OFF061<17:1>	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
ADC Data 3	_ADC_DATA3_VECTOR	62	OFF062<17:1>	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	Yes
ADC Data 4	_ADC_DATA4_VECTOR	63	OFF063<17:1>	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	Yes
ADC Data 5	_ADC_DATA5_VECTOR	64	OFF064<17:1>	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	Yes
ADC Data 6	_ADC_DATA6_VECTOR	65	OFF065<17:1>	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
ADC Data 7	_ADC_DATA7_VECTOR	66	OFF066<17:1>	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
ADC Data 8	_ADC_DATA8_VECTOR	67	OFF067<17:1>	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
ADC Data 9	_ADC_DATA9_VECTOR	68	OFF068<17:1>	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
ADC Data 10	_ADC_DATA10_VECTOR	69	OFF069<17:1>	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
ADC Data 11	_ADC_DATA11_VECTOR	70	OFF070<17:1>	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
ADC Data 12	_ADC_DATA12_VECTOR	71	OFF071<17:1>	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
ADC Data 13	_ADC_DATA13_VECTOR	72	OFF072<17:1>	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
ADC Data 14	_ADC_DATA14_VECTOR	73	OFF073<17:1>	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
ADC Data 15	_ADC_DATA15_VECTOR	74	OFF074<17:1>	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	Yes
ADC Data 16	_ADC_DATA16_VECTOR	75	OFF075<17:1>	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	Yes
ADC Data 17	_ADC_DATA17_VECTOR	76	OFF076<17:1>	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	Yes
ADC Data 18	_ADC_DATA18_VECTOR	77	OFF077<17:1>	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	Yes
ADC Data 19	_ADC_DATA19_VECTOR	78	OFF078<17:1>	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
ADC Data 20	_ADC_DATA20_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
ADC Data 21	_ADC_DATA21_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes

- Note 1:** Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.
- Note 2:** Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
DMA Channel 5	_DMA5_VECTOR	139	OFF139<17:1>	IFS4<11>	IEC4<11>	IPC34<28:26>	IPC34<25:24>	No
DMA Channel 6	_DMA6_VECTOR	140	OFF140<17:1>	IFS4<12>	IEC4<12>	IPC35<4:2>	IPC35<1:0>	No
DMA Channel 7	_DMA7_VECTOR	141	OFF141<17:1>	IFS4<13>	IEC4<13>	IPC35<12:10>	IPC35<9:8>	No
SPI2 Fault	_SPI2_FAULT_VECTOR	142	OFF142<17:1>	IFS4<14>	IEC4<14>	IPC35<20:18>	IPC35<17:16>	Yes
SPI2 Receive Done	_SPI2_RX_VECTOR	143	OFF143<17:1>	IFS4<15>	IEC4<15>	IPC35<28:26>	IPC35<25:24>	Yes
SPI2 Transfer Done	_SPI2_TX_VECTOR	144	OFF144<17:1>	IFS4<16>	IEC4<16>	IPC36<4:2>	IPC36<1:0>	Yes
UART2 Fault	_UART2_FAULT_VECTOR	145	OFF145<17:1>	IFS4<17>	IEC4<17>	IPC36<12:10>	IPC36<9:8>	Yes
UART2 Receive Done	_UART2_RX_VECTOR	146	OFF146<17:1>	IFS4<18>	IEC4<18>	IPC36<20:18>	IPC36<17:16>	Yes
UART2 Transfer Done	_UART2_TX_VECTOR	147	OFF147<17:1>	IFS4<19>	IEC4<19>	IPC36<28:26>	IPC36<25:24>	Yes
I2C2 Bus Collision Event	_I2C2_BUS_VECTOR	148	OFF148<17:1>	IFS4<20>	IEC4<20>	IPC37<4:2>	IPC37<1:0>	Yes
I2C2 Slave Event	_I2C2_SLAVE_VECTOR	149	OFF149<17:1>	IFS4<21>	IEC4<21>	IPC37<12:10>	IPC37<9:8>	Yes
I2C2 Master Event	_I2C2_MASTER_VECTOR	150	OFF150<17:1>	IFS4<22>	IEC4<22>	IPC37<20:18>	IPC37<17:16>	Yes
Control Area Network 1	_CAN1_VECTOR	151	OFF151<17:1>	IFS4<23>	IEC4<23>	IPC37<28:26>	IPC37<25:24>	Yes
Control Area Network 2	_CAN2_VECTOR	152	OFF152<17:1>	IFS4<24>	IEC4<24>	IPC38<4:2>	IPC38<1:0>	Yes
Ethernet Interrupt	_ETHERNET_VECTOR	153	OFF153<17:1>	IFS4<25>	IEC4<25>	IPC38<12:10>	IPC38<9:8>	Yes
SPI3 Fault	_SPI3_FAULT_VECTOR	154	OFF154<17:1>	IFS4<26>	IEC4<26>	IPC38<20:18>	IPC38<17:16>	Yes
SPI3 Receive Done	_SPI3_RX_VECTOR	155	OFF155<17:1>	IFS4<27>	IEC4<27>	IPC38<28:26>	IPC38<25:24>	Yes
SPI3 Transfer Done	_SPI3_TX_VECTOR	156	OFF156<17:1>	IFS4<28>	IEC4<28>	IPC39<4:2>	IPC39<1:0>	Yes
UART3 Fault	_UART3_FAULT_VECTOR	157	OFF157<17:1>	IFS4<29>	IEC4<29>	IPC39<12:10>	IPC39<9:8>	Yes
UART3 Receive Done	_UART3_RX_VECTOR	158	OFF158<17:1>	IFS4<30>	IEC4<30>	IPC39<20:18>	IPC39<17:16>	Yes
UART3 Transfer Done	_UART3_TX_VECTOR	159	OFF159<17:1>	IFS4<31>	IEC4<31>	IPC39<28:26>	IPC39<25:24>	Yes
I2C3 Bus Collision Event	_I2C3_BUS_VECTOR	160	OFF160<17:1>	IFS5<0>	IEC5<0>	IPC40<4:2>	IPC40<1:0>	Yes
I2C3 Slave Event	_I2C3_SLAVE_VECTOR	161	OFF161<17:1>	IFS5<1>	IEC5<1>	IPC40<12:10>	IPC40<9:8>	Yes
I2C3 Master Event	_I2C3_MASTER_VECTOR	162	OFF162<17:1>	IFS5<2>	IEC5<2>	IPC40<20:18>	IPC40<17:16>	Yes
SPI4 Fault	_SPI4_FAULT_VECTOR	163	OFF163<17:1>	IFS5<3>	IEC5<3>	IPC40<28:26>	IPC40<25:24>	Yes
SPI4 Receive Done	_SPI4_RX_VECTOR	164	OFF164<17:1>	IFS5<4>	IEC5<4>	IPC41<4:2>	IPC41<1:0>	Yes
SPI4 Transfer Done	_SPI4_TX_VECTOR	165	OFF165<17:1>	IFS5<5>	IEC5<5>	IPC41<12:10>	IPC41<9:8>	Yes
Real Time Clock	_RTCC_VECTOR	166	OFF166<17:1>	IFS5<6>	IEC5<6>	IPC41<20:18>	IPC41<17:16>	No
Flash Control Event	_FLASH_CONTROL_VECTOR	167	OFF167<17:1>	IFS5<7>	IEC5<7>	IPC41<28:26>	IPC41<25:24>	No

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

Note 2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
06C8	OFF098	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06CC	OFF099	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06D0	OFF100	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06D4	OFF101	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06D8	OFF102	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06DC	OFF103	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06E0	OFF104	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06E4	OFF105	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06E8	OFF106	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06EC	OFF107	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06F4	OFF109	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06F8	OFF110	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
06FC	OFF111	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0700	OFF112	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0704	OFF113	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0708	OFF114	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
070C	OFF115	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0710	OFF116	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0714	OFF117	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.
- 2: This bit is only available on devices with a Crypto module.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
11A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
11B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
11C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
11D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
11E0	DCH2CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	—	0000
11F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1210	DCH2SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
1220	DCH2DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
1230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 “CLR, SET, and INV Registers” for more information.

PIC32MZ Graphics (DA) Family

REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF**: Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
0 = No interrupt is pending
- bit 4 **CHDHIF**: Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending
- bit 3 **CHBCIF**: Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending
- bit 2 **CHCCIF**: Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending
- bit 1 **CHTAIF**: Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending
- bit 0 **CHERIF**: Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected
 Either the source or the destination address is invalid.
0 = No interrupt is pending

PIC32MZ Graphics (DA) Family

REGISTER 11-19: USBExRXA: USB ENDPOINT 'x' RECEIVE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXHUBPRT<6:0>							
23:16	R/W-0 MULTTRAN	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXHUBADD<6:0>							
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFADDR<6:0>							

Legend:	HC = Hardware Cleared	HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-24 **RXHUBPRT<6:0>:** RX Hub Port bits (*Host mode*)

When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, this field records the port number of that USB 2.0 hub.

bit 23 **MULTTRAN:** RX Hub Multiple Translators bit (*Host mode*)

1 = The USB 2.0 hub has multiple transaction translators

0 = The USB 2.0 hub has a single transaction translator

bit 22-16 **RXHUBADD<6:0>:** RX Hub Address bits (*Host mode*)

When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, these bits record the address of the USB 2.0 hub.

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **RXFADDR<6:0>:** RX Functional Address bits (*Host mode*)

Specifies the address for the target function that is to be accessed through the associated endpoint. It needs to be defined for each RX endpoint that is used.

PIC32MZ Graphics (DA) Family

TABLE 12-1: INPUT PIN SELECTION

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPN Pin Selection
INT3	INT3R	INT3R<3:0>	0000 = RPD2 0001 = RPG8 0010 = RPF4 0011 = Reserved 0100 = RPF1 0101 = RPB9 0110 = RPB10 0111 = RPC14 1000 = RPB5 1001 = Reserved 1010 = RPC1 1011 = RPD14 1100 = RPG1 1101 = RPA14 1110 = RPD6 1111 = Reserved
T2CK	T2CKR	T2CKR<3:0>	
T6CK	T6CKR	T6CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
IC7	IC7R	IC7R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
U2CTS	U2CTSR	U2CTSR<3:0>	
U5RX	U5RXR	U5RXR<3:0>	
U6CTS	U6CTSR	U6CTSR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
SDI3	SDI3R	SDI3R<3:0>	
SDI5	SDI5R	SDI5R<3:0>	
SS6	SS6R	SS6R<3:0>	
REFCLKI1	REFCLKI1R	REFCLKI1R<3:0>	
INT4	INT4R	INT4R<3:0>	0000 = RPD3 0001 = RPG7 0010 = RPF5 0011 = RPD11 0100 = RPF0 0101 = RPB1 0110 = RPE5 0111 = RPC13 1000 = RPB3 1001 = Reserved 1010 = RPC4 1011 = Reserved 1100 = RPG0 1101 = RPA15 1110 = RPD7 1111 = Reserved
T5CK	T5CKR	T5CKR<3:0>	
T7CK	T7CKR	T7CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
IC8	IC8R	IC8R<3:0>	
U3RX	U3RXR	U3RXR<3:0>	
U4CTS	U4CTSR	U4CTSR<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
SDI4	SDI4R	SDI4R<3:0>	
C1RX	C1RXR	C1RXR<3:0>	
REFCLKI4	REFCLKI4R	REFCLKI4R<3:0>	

PIC32MZ Graphics (DA) Family

REGISTER 22-4: SQI1CON: SQI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	r-0 —	R/W-0 SCHECK ⁽¹⁾
23:16	R/W-0 DDRMODE	R/W-0 DASSERT	R/W-0 DEVSEL<1:0>	R/W-0 DEVSEL<1:0>	R/W-0 LANEMODE<1:0>	R/W-0 LANEMODE<1:0>	R/W-0 CMDINIT<1:0>	R/W-0 CMDINIT<1:0>
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<7:0>							

Legend:

R = Readable bit

-n = Value at POR

r = Reserved

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **Reserved:** Must be programmed as '0'

bit 24 **SCHECK:** Flash Status Check bit⁽¹⁾

1 = Check the status of the Flash

0 = Do not check the status of the Flash

bit 23 **DDRMODE:** Double Data Rate Mode bit

1 = Set the SQI transfers to DDR mode

0 = Set the SQI transfers to SDR mode

bit 22 **DASSERT:** Chip Select Assert bit

1 = Chip Select is deasserted after transmission or reception of the specified number of bytes

0 = Chip Select is not deasserted after transmission or reception of the specified number of bytes

bit 21-20 **DEVSEL<1:0>:** SQI Device Select bits

11 = Reserved

10 = Reserved

01 = Select Device 1

00 = Select Device 0

bit 19-18 **LANEMODE<1:0>:** SQI Lane Mode Select bits

11 = Reserved

10 = Quad Lane mode

01 = Dual Lane mode

00 = Single Lane mode

bit 17-16 **CMDINIT<1:0>:** Command Initiation Mode Select bits

If it is Transmit, commands are initiated based on a write to the transmit register or the contents of TX buffer. If CMDINIT is Receive, commands are initiated based on reads to the read register or RX buffer availability.

11 = Reserved

10 = Receive

01 = Transmit

00 = Idle

bit 15-0 **TXRXCOUNT<15:0>:** Transmit/Receive Count bits

These bits specify the total number of bytes to transmit or received (based on CMDINIT).

Note 1: When this bit is set to '1', the SQI module uses the SQI1MEMSTAT register to control the status check command process.

PIC32MZ Graphics (DA) Family

REGISTER 26-1: EBICSx: EXTERNAL BUS INTERFACE CHIP SELECT REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **CSADDR<15:0>**: Base Address for Device bits

Address in physical memory, which will select the external device.

bit 15-0 **Unimplemented**: Read as '0'

PIC32MZ Graphics (DA) Family

REGISTER 27-5: CESTAT: CRYPTO ENGINE STATUS REGISTER (CONTINUED)

bit 16 **ACTIVE:** Buffer Descriptor Processor Status bit

1 = BDP is active

0 = BDP is idle

bit 15-0 **BDCTRL<15:0>:** Descriptor Control Word Status bits

These bits contain the current descriptor control word.

28.0 RANDOM NUMBER GENERATOR (RNG)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. “Crypto Engine (CE) and Random Number Generator (RNG)”** (DS60001246), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Random Number Generator (RNG) core implements a thermal noise-based, True Random Number Generator (TRNG) and a cryptographically secure Pseudo-Random Number Generator (PRNG).

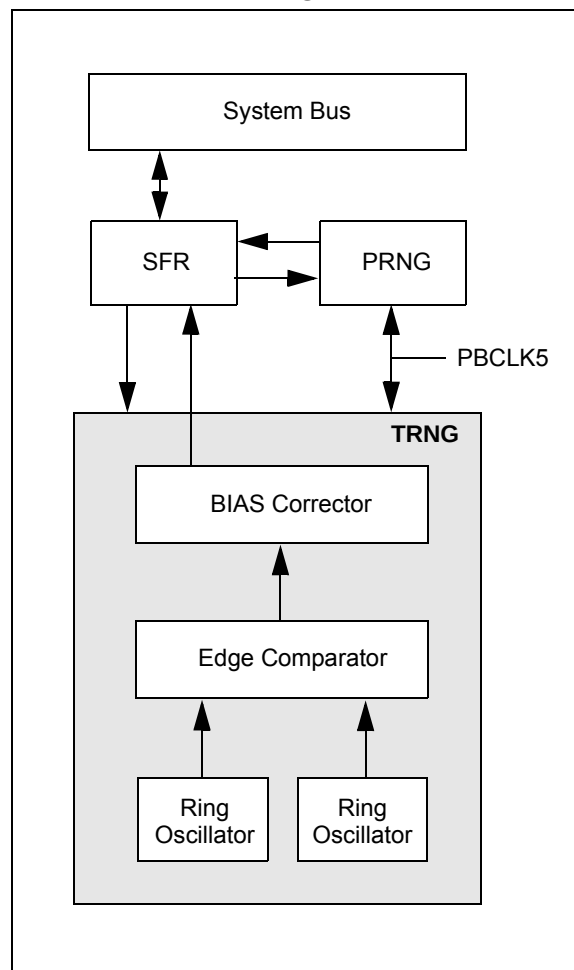
The TRNG uses multiple ring oscillators and the inherent thermal noise of integrated circuits to generate true random numbers that can initialize the PRNG.

The PRNG is a flexible LSFR, which is capable of manifesting a maximal length LFSR of up to 64-bits.

The following are some of the key features of the Random Number Generator:

- TRNG:
 - Up to 25 Mbps of random bits
 - Multi-Ring Oscillator based design
 - Built-in Bias Corrector
- PRNG:
 - LSFR-based
 - Up to 64-bit polynomial length
 - Programmable polynomial
 - TRNG can be seed value

FIGURE 28-1: RANDOM NUMBER GENERATOR BLOCK DIAGRAM



PIC32MZ Graphics (DA) Family

REGISTER 30-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-22 **Unimplemented:** Read as '0'
- bit 21 **TXBO:** Transmitter in Error State Bus OFF ($TERRCNT \geq 256$)
- bit 20 **TXBP:** Transmitter in Error State Bus Passive ($TERRCNT \geq 128$)
- bit 19 **RXBP:** Receiver in Error State Bus Passive ($RERRCNT \geq 128$)
- bit 18 **TXWARN:** Transmitter in Error State Warning ($128 > TERRCNT \geq 96$)
- bit 17 **RXWARN:** Receiver in Error State Warning ($128 > RERRCNT \geq 96$)
- bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning
- bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter
- bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 30-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-0 **FIFOIP<31:0>:** FIFO Interrupt Pending bits
- 1 = One or more enabled FIFO interrupts are pending
- 0 = No FIFO interrupts are pending

PIC32MZ Graphics (DA) Family

REGISTER 31-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSE:** Transmit BVCI Bus Error Interrupt bit⁽²⁾

1 = BVCI Bus Error has occurred

0 = BVCI Bus Error has not occurred

This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 13 **RXBUSE:** Receive BVCI Bus Error Interrupt bit⁽²⁾

1 = BVCI Bus Error has occurred

0 = BVCI Bus Error has not occurred

This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARK:** Empty Watermark Interrupt bit⁽²⁾

1 = Empty Watermark pointer reached

0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.

bit 8 **FWMARK:** Full Watermark Interrupt bit⁽²⁾

1 = Full Watermark pointer reached

0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

Note 1: This bit is only used for TX operations.

Note 2: This bit is are only used for RX operations.

Note: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

PIC32MZ Graphics (DA) Family

REGISTER 36-1: GLCDMODE: GRAPHICS LCD CONTROLLER MODE REGISTER (CONTINUED)

- bit 19 **FORCEBLANK:** Force Output to Blank bit
 1 = Forces output to blank
 0 = No effect
- bit 18-10 **Unimplemented:** Read as '0'
- bit 9 **YUVOUTPUT:** YUV Output Enable bit
 1 = YUV is enabled
 0 = RGB is enabled
- bit 8 **FORMATCLK:** Formatting Clock Divide Enable bit
 1 = Formatting clock is not divided
 0 = Formatting clock is divided
- bit 7-5 **RGBSEQ<2:0>:** RGB Sequential Modes bit
 111 = BT.656
 110 = YUYV
 101 = Reserved
 100 = Reserved
 011 = Reserved
 010 = Reserved
 001 = Reserved
 000 = Parallel RGB (RGB888, RGB666, RGB332)
- bit 4-0 **Unimplemented:** Read as '0'

PIC32MZ Graphics (DA) Family

REGISTER 38-13: DDRDLYCFG0: DDR DELAY CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RMWDLY<3:0>				R2WDLY<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2WCSDLY<3:0>				W2WDLY<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	R2RCSDLY<3:0>				R2RDLY<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2RCSDLY<3:0>				W2RDLY<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **RMWDLY<3:0>**: Read-Modify-Write Delay bits

These bits specify the minimum number of clocks required between the read and write commands issued for a read-modify-write operation.

bit 27-24 **R2WDLY<3:0>**: Read-to-Write Delay bits

These bits specify the minimum number of clocks required between a read command and write command. Commands may be to the same or different Chip Selects.

bit 23-20 **W2WCSDLY<3:0>**: Write-to-Write Chip Select Delay bits

These bits specify the minimum number of clocks required between two write commands to different Chip Selects.

bit 19-16 **W2WDLY<3:0>**: Write-to-Write Delay bits

These bits specify the minimum number of clocks required between two write commands to the same Chip Select.

bit 15-12 **R2RCSDLY<3:0>**: Read-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between two read commands to different Chip Selects.

bit 11-8 **R2RDLY<3:0>**: Read-to-Read Delay bits

These bits specify the minimum number of clocks required between two read commands to the same Chip Select.

bit 7-4 **W2RCSDLY<3:0>**: Write-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between a write command and a read command to different Chip Selects.

bit 3-0 **W2RDLY<3:0>**: Write-to-Read Delay bits

These bits specify the minimum number of clocks required between a write command and a read command to the same Chip Select.

PIC32MZ Graphics (DA) Family

REGISTER 39-5: SDHCDATA: SDHC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DATA<31:0>**: Buffer Data bits

These bits are used to access bits 31 through 0 of the internal data buffer.