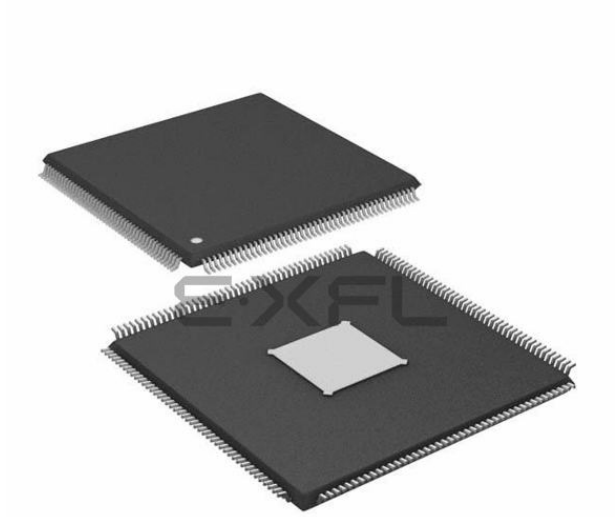
Microchip Technology - PIC32MZ1064DAB176-I/2J Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

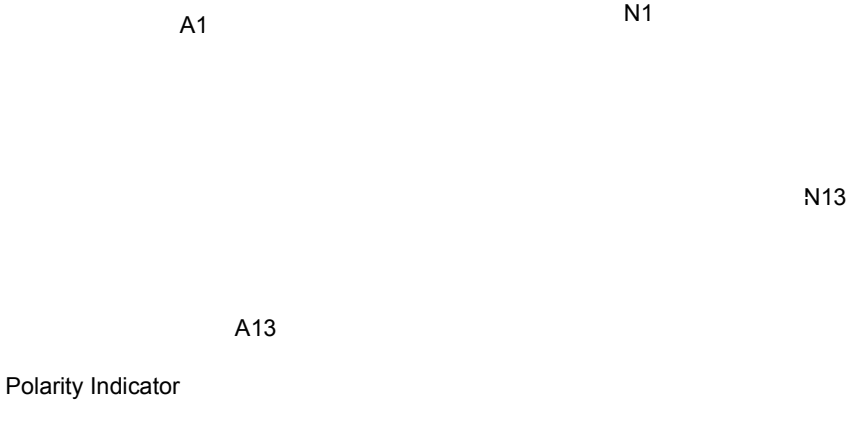
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1064dab176-i-2j

TABLE 5: PIN NAMES FOR 169-PIN DEVICES (CONTINUED)

169-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA169
PIC32MZ1025DAB169
PIC32MZ1064DAA169
PIC32MZ1064DAB169
PIC32MZ2025DAA169
PIC32MZ2025DAB169
PIC32MZ2064DAA169
PIC32MZ2064DAB169
PIC32MZ1025DAG169
PIC32MZ1025DAH169
PIC32MZ1064DAG169
PIC32MZ1064DAH169
PIC32MZ2025DAG169
PIC32MZ2025DAH169
PIC32MZ2064DAG169
PIC32MZ2064DAH169



Ball/Pin Number	Full Pin Name
E9	AN22/RPD14/RD14
E10	AN29/SCK3/RB14
E11	TCK/AN24/RA1
E12	OSC1/CLKI/RC12
E13	OSC2/CLKO/RC15
F1	SDCMD/SQICS0/RPD4/RD4
F2	SQICS1/RPD5/RD5
F3	EBIA6/RPE5/PMA6/RE5
F4	DDRVREF(5)
F5	VSS
F6	EBID6/AN16/PMD6/RE6
F7	AN48/CTPLS/RB13
F8	GD18/EBIBS1/RJ10
F9	GD9/EBIBS0/RJ12
F10	EBIRDY3/AN32/RJ2
F11	AN33/SCK6/RD15
F12	HSYNC/EBICS1/RJ5
F13	VSYNC/EBICS0/RJ4
G1	SCK1/RD1
G2	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2
G3	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3
G4	VSS1V8
G5	VSS
G6	VSS
G7	VSS
G8	VSS
G9	VDDIO
G10	GD8/EBID11/PMD11/RJ14
G11	GCLK/EBICS2/RJ6
G12	GD0/EBID13/PMD13/RJ13
G13	GEN/EBICS3/RJ7
H1	GD2/EBID15/RPD9/PMD15/RD9

Ball/Pin Number	Full Pin Name
H2	SCK4/RD10
H3	RTCC/RPD0/RD0
H4	VSS1V8
H5	VDDR1V8(4)
H6	VDDR1V8(4)
H7	VSS
H8	VSS
H9	VDDIO
H10	GD13/EBIA18/RK4
H11	EBIA3/AN11/PMA3/RK2
H12	$\overline{\text{SDWP}}$/EBIRP/RH2
H13	EBIA0/PMA0/RJ15
J1	GD7/EBIA12/RPD12/PMA12/RD12
J2	GD22/EBIA13/PMA13/RD13
J3	RPF8/SCL3/RF8
J4	VSS1V8
J5	VDDR1V8(4)
J6	VDDR1V8(4)
J7	VSS
J8	VSS
J9	VDDIO
J10	GD14/EBIA19/RK5
J11	EBIA1/AN38/PMA1/RK1
J12	EBIA4/AN36/PMA4/RH7
J13	AN35/RH3
K1	$\overline{\text{MCLR}}$
K2	GD16/EBID8/RPF5/SCL5/PMD8/RF5
K3	GD5/EBIA10/RPF1/PMA10/RF1
K4	VSS1V8
K5	VDDR1V8(4)
K6	VDDR1V8(4)
K7	Vss

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 2 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
5: This pin is a No Connect in devices without DDR.
6: These pins are restricted to input functions only.

3.0 CPU

Note 1: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2: MIPS32® microAptiv™ Microprocessor Core resources are available at: http://www.imgtec.com.

The MIPS32 microAptiv Microprocessor Core is the heart of the PIC32MZ DA family device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

3.1 Features

PIC32MZ DA family processor core key features:

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2):
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
  - Virtual memory support
- microMIPS compatible instruction set:
  - Improves code size density over MIPS32, while maintaining MIPS32 performance.
  - Supports all MIPS32 instructions (except branch-likely instructions)
  - Fifteen additional 32-bit instructions and 39 16-bit instructions corresponding to commonly-used MIPS32 instructions
  - Stack pointer implicit in instruction
  - MIPS32 assembly and ABI compatible
- MMU with Translation Lookaside Buffer (TLB) mechanism:
  - 32 dual-entry fully associative Joint TLB
  - 4-entry fully associative Instruction TLB
  - 4-entry fully associative Data TLB
  - 4 KB pages
- Separate L1 data and instruction caches:
  - 32 KB 4-way Instruction Cache (I-Cache)
  - 32 KB 4-way Data Cache (D-Cache)
- Autonomous Multiply/Divide Unit (MDU):
  - Maximum issue rate of one 32x32 multiply per clock
  - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
  - Support for single stepping
  - Virtual instruction and data address/value breakpoints
  - Hardware breakpoint supports both address match and address range triggering.
  - Eight instruction and four data complex breakpoints
- iFlowtrace® version 2.0 support:
  - Real-time instruction program counter
  - Special events trace capability
  - Two performance counters with 34 user-selectable countable events
  - Disabled if the processor enters Debug mode
- Four Watch registers:
  - Instruction, Data Read, Data Write options
  - Address match masking options
- DSP ASE Extension:
  - Native fractional format data type operations
  - Register Single Instruction Multiple Data (SIMD) operations (add, subtract, multiply, shift)
  - GPR-based shift
  - Bit manipulation
  - Compare-Pick
  - DSP Control Access
  - Indexed-Load
  - Branch
  - Multiplication of complex operands
  - Variable bit insertion and extraction
  - Virtual circular buffers
  - Arithmetic saturation and overflow handling
  - Zero-cycle overhead saturation and rounding operations

TABLE 4-19: SYSTEM BUS TARGET PROTECTION GROUP 9 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT9ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT9ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT9ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT9ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT9ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT9REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT9RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT9WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT9REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT9RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT9WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MZ DA family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MZ DA oscillator system has the following modules and features:

- Five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown with dedicated Back-up FRC (BFRC)
- Dedicated On-Chip PLL for DDR2 and USB modules
- Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility

A block diagram of the oscillator system is provided in Figure 8-1. The clock distribution is shown in Table 8-1.

REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—					PLLIDIV<2:0>		
7:0	R/W-y	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	PLLICLK	—	—	—	—	PLLRANGE<2:0>		

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits

111 = Reserved
110 = Reserved
101 = PLL Divide by 32
100 = PLL Divide by 16
011 = PLL Divide by 8
010 = PLL Divide by 4
001 = PLL Divide by 2
000 = Reserved

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits

1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

The default setting is specified by the FPLLMULT<6:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

bit 15-11 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER (CONTINUED)

bit 4 **CHAEN:** Channel Automatic Enable bit
1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit
1 = An event has been detected
0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
11 = Channel has priority 3 (highest)
10 = Channel has priority 2
01 = Channel has priority 1
00 = Channel has priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3340	USB DPBFD	31:16	—	—	—	—	—	—	—	—	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—	0000
		15:0	—	—	—	—	—	—	—	—	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—	0000
3344	USB TMCON1	31:16	THHSRTN<15:0>																05E6
		15:0	TUCH<15:0>																4074
3348	USB TMCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THSBT<3:0>				0000
3360	USB LPMR1	31:16	—	—	LPM ERRIE	LPM RESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE	—	—	—	LPMNAK(1)	LPMEN<1:0>		LPMRES	LPMXMT	0000
														__(2)	__(2)	__(2)			0000
		15:0	ENDPOINT<3:0>				—	—	—	RMTWAK	HIRD<3:0>				LNKSTATE<3:0>				0000
3364	USB LMPR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	LPMFADDR<6:0>							—	—	LPMERR(1)	LPMRES	LPMNC	LPMACK	LPMNY	LPMST	0000
													__(2)						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note
1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 11-2: USB REGISTER MAP 2

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	USB CRCON	31:16	—	—	—	—	—	USBIF	USBRF	USBWKUP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	USB IDOVEN	USB IDVAL	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R-0	R/W-0
	AUTOCLR	ISO AUTORQ	DMAREQEN	DISNYET PIDERR	DMAREQMD	— DATATWEN	— DATATGGL	INCOMPRX
23:16	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0, HC	R-0, HS	R/W-0, HS	R-0, HS, HC	R/W-0, HS
	CLRDT	SENTSTALL RXSTALL	SENDSTALL REQPKT	FLUSH	DATAERR DERRNAKT	OVERRUN ERROR	FIFOFULL	RXPKTRDY
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					RXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXMAXP<7:0>							

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AUTOCLR:** RXPKTRDY Automatic Clear Control bit

1 = RXPKTRDY will be automatically cleared when a packet of RXMAXP bytes has been unloaded from the RX FIFO. When packets of less than the maximum packet size are unloaded, RXPKTRDY will have to be cleared manually. When using a DMA to unload the RX FIFO, data is read from the RX FIFO in 4-byte chunks regardless of the RXMAXP.

0 = No automatic clearing of RXPKTRDY

This bit should not be set for high-bandwidth Isochronous endpoints.

bit 30 **ISO:** Isochronous Endpoint Control bit (*Device mode*)

1 = Enable the RX endpoint for Isochronous transfers

0 = Enable the RX endpoint for Bulk/Interrupt transfers

AUTORQ: Automatic Packet Request Control bit (*Host mode*)

1 = REQPKT will be automatically set when RXPKTRDY bit is cleared.

0 = No automatic packet request

This bit is automatically cleared when a short packet is received.

bit 29 **DMAREQEN:** DMA Request Enable Control bit

1 = Enable DMA requests for the RX endpoint.

0 = Disable DMA requests for the RX endpoint.

bit 28 **DISNYET:** Disable NYET Handshakes Control/PID Error Status bit (*Device mode*)

1 = In Bulk/Interrupt transactions, disables the sending of NYET handshakes. All successfully received RX packets are ACKed including at the point at which the FIFO becomes full.

0 = Normal operation.

In Bulk/Interrupt transactions, this bit only has any effect in Hi-Speed mode, in which mode it should be set for all Interrupt endpoints.

PIDERR: PID Error Status bit (*Host mode*)

1 = In ISO transactions, this indicates a PID error in the received packet.

0 = No error

bit 27 **DMAREQMD:** DMA Request Mode Selection bit

1 = DMA Request Mode 1

0 = DMA Request Mode 0

TABLE 12-10: PORTH REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0700	ANSELH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ANSH11	—	—	—	ANSH7	—	—	ANSH4	ANSH3	—	—	—	0898
0710	TRISH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISH15	TRISH14	TRISH13	TRISH12	TRISH11	TRISH10	TRISH9	TRISH8	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	FFFF
0720	PORTH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RH15	RH14	RH13	RH12	RH11	RH10	RH9	RH8	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	xxxx
0730	LATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATH15	LATH14	LATH13	LATH12	LATH11	LATH10	LATH9	LATH8	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	xxxx
0740	ODCH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCH15	ODCH14	ODCH13	ODCH12	ODCH11	ODCH10	ODCH9	ODCH8	ODCH7	ODCH6	ODCH5	ODCH4	ODCH3	ODCH2	ODCH1	ODCH0	0000
0750	CNPUH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUH15	CNPUH14	CNPUH13	CNPUH12	CNPUH11	CNPUH10	CNPUH9	CNPUH8	CNPUH7	CNPUH6	CNPUH5	CNPUH4	CNPUH3	CNPUH2	CNPUH1	CNPUH0	0000
0760	CNPDH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDH15	CNPDH14	CNPDH13	CNPDH12	CNPDH11	CNPDH10	CNPDH9	CNPDH8	CNPDH7	CNPDH6	CNPDH5	CNPDH4	CNPDH3	CNPDH2	CNPDH1	CNPDH0	0000
0770	CNCONH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0780	CNENH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEH15	CNIEH14	CNIEH13	CNIEH12	CNIEH11	CNIEH10	CNIEH9	CNIEH8	CNIEH7	CNIEH6	CNIEH5	CNIEH4	CNIEH3	CNIEH2	CNIEH1	CNIEH0	0000
0790	CNSTATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATH15	CN STATH14	CN STATH13	CN STATH12	CN STATH11	CN STATH10	CN STATH9	CN STATH8	CN STATH7	CN STATH6	CN STATH5	CN STATH4	CN STATH3	CN STATH2	CN STATH1	CN STATH0	0000
07A0	CNNEH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEH15	CNNEH14	CNNEH13	CNNEH12	CNNEH11	CNNEH10	CNNEH9	CNNEH8	CNNEH7	CNNEH6	CNNEH5	CNNEH4	CNNEH3	CNNEH2	CNNEH1	CNNEH0	0000
07B0	CNFH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFH15	CNFH14	CNFH13	CNFH12	CNFH11	CNFH10	CNFH9	CNFH8	CNFH7	CNFH6	CNFH5	CNFH4	CNFH3	CNFH2	CNFH1	CNFH0	0000
07C0	SRCON0H	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1H15	SR1H14	SR1H13	SR1H12	SR1H11	SR1H10	SR1H9	SR1H8	SR1H7	SR1H6	SR1H5	SR1H4	SR1H3	SR1H2	SR1H1	SR1H0	0000
07D0	SRCON1H	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0H15	SR0H14	SR0H13	SR0H12	SR0H11	SR0H10	SR0H9	SR0H8	SR0H7	SR0H6	SR0H5	SR0H4	SR0H3	SR0H2	SR0H1	SR0H0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

15.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

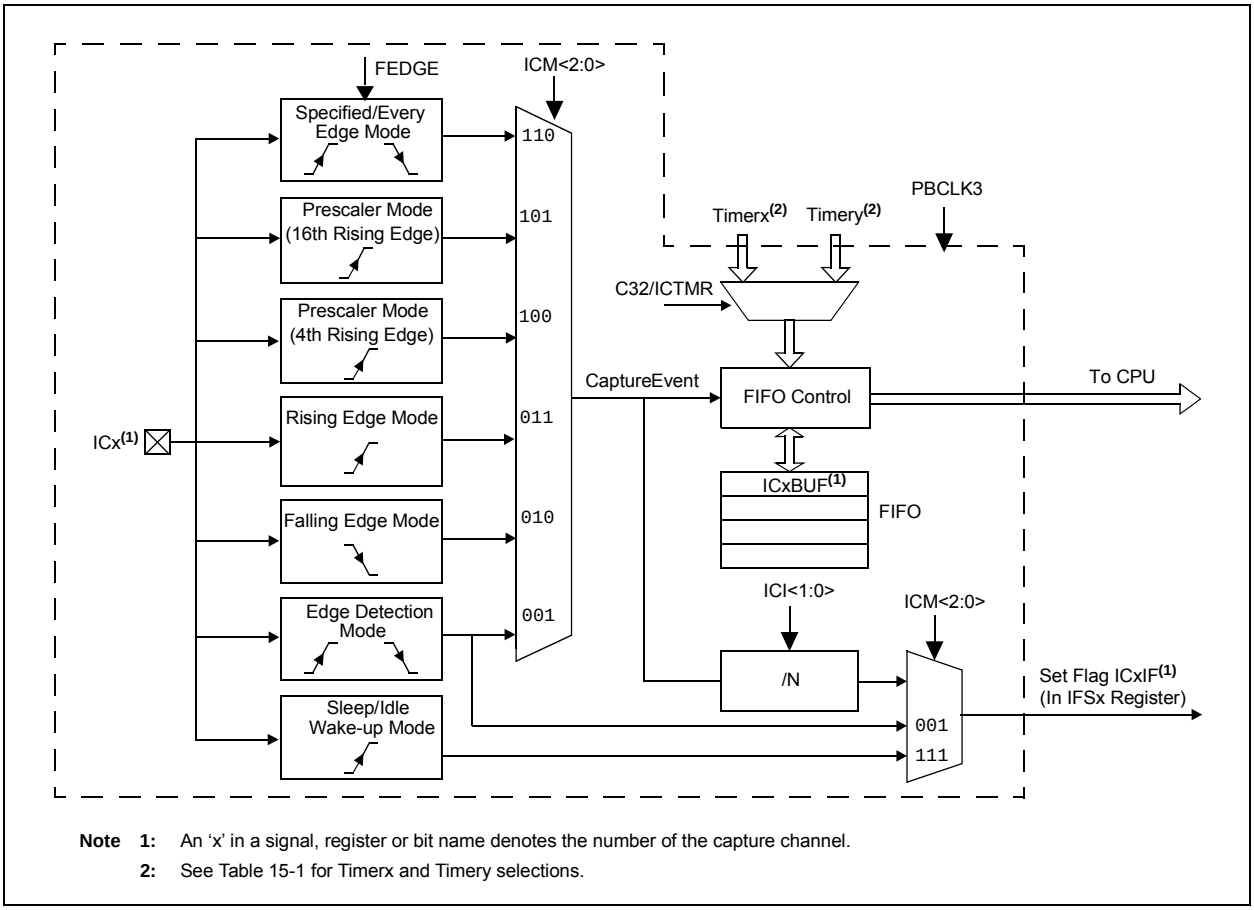
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 15-1 for Timerx and Timery selections.

20.1 RTCC Control Registers

TABLE 20-1: RTCC REGISTER MAP

Virtual Address (BF8C_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	RTCCLKSEL<1:0>		RTCOUTSEL<1:0>		RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0010	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0020	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0030	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0040	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0050	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 23-2: I2CxSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HS, HC	R-0, HS, HC	R/C-0, HS, HC	U-0	U-0	R/C-0, HS	R-0, HS, HC	R-0, HS, HC
	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS, SC	R/C-0, HS, SC	R-0, HS, HC	R/C-0, HS, HC	R/C-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF

Legend:	HS = Hardware Set	HC = Hardware Cleared	SC = Software Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I²C Slave mode only)
1 = I²C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

FIGURE 27-6: FORMAT OF BD_DSTADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_DSTADDR<31:24>							
23-16	BD_DSTADDR<23:16>							
15-8	BD_DSTADDR<15:8>							
7-0	BD_DSTADDR<7:0>							

bit 31-0 **BD_DSTADDR:** Buffer Destination Address
The destination address of the buffer that needs to be passed through the PE-CRDMA for encryption or authentication. This address must be on a 32-bit boundary.

FIGURE 27-7: FORMAT OF BD_NXTADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_NXTADDR<31:24>							
23-16	BD_NXTADDR<23:16>							
15-8	BD_NXTADDR<15:8>							
7-0	BD_NXTADDR<7:0>							

bit 31-0 **BD_NXTADDR:** Next BD Pointer Address Has Next Buffer Descriptor
The next buffer can be a next segment of the previous buffer or a new packet.

FIGURE 27-8: FORMAT OF BD_UPDPTR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_UPDADDR<31:24>							
23-16	BD_UPDADDR<23:16>							
15-8	BD_UPDADDR<15:8>							
7-0	BD_UPDADDR<7:0>							

bit 31-0 **BD_UPDADDR:** UPD Address Location
The update address has the location where the CRDMA results are posted. The updated results are the ICV values, key output values as needed.

TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
BA34	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA38	ADCDATA14	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA3C	ADCDATA15	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA40	ADCDATA16	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA44	ADCDATA17	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA48	ADCDATA18	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA4C	ADCDATA19	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA50	ADCDATA20	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA54	ADCDATA21	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA58	ADCDATA22	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA5C	ADCDATA23	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA60	ADCDATA24	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA64	ADCDATA25	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA68	ADCDATA26	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA6C	ADCDATA27	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA70	ADCDATA28	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA74	ADCDATA29	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA78	ADCDATA30	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA7C	ADCDATA31	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 29-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 4 **SIGN2:** AN2 Signed Data Mode bit
1 = AN2 is using Signed Data mode
0 = AN2 is using Unsigned Data mode

bit 3 **DIFF1:** AN1 Mode bit
1 = AN1 is using Differential mode
0 = AN1 is using Single-ended mode

bit 2 **SIGN1:** AN1 Signed Data Mode bit
1 = AN1 is using Signed Data mode
0 = AN1 is using Unsigned Data mode

bit 1 **DIFF0:** AN0 Mode bit
1 = AN0 is using Differential mode
0 = AN0 is using Single-ended mode

bit 0 **SIGN0:** AN0 Signed Data Mode bit
1 = AN0 is using Signed Data mode
0 = AN0 is using Unsigned Data mode

REGISTER 30-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	TXNFULLIF(1)	TXHALFIF	TXEMPTYIF(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
	—	—	—	—	RXOVFLIF	RXFULLIF(1)	RXHALFIF(1)	RXNEMPTYIF(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a Transmit Buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a Receive Buffer)
Unused, reads '0'

Note 1: This bit is read-only and reflects the status of the FIFO.

REGISTER 38-16: DDRDLYCFG3: DDR DELAY CONFIGURATION REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	FAWTDLY<5:0>					
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RAS2RASSBNKDLY<5:0>					
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RAS2PCHRGDLY<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-16 **FAWTDLY<5:0>:** Four Activate Window Time Delay bits
These bits specify the minimum number of clocks within which only four banks may be opened.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RAS2RASSBNKDLY<5:0>:** RAS-to-RAS Same Bank Delay bits
These bits specify the minimum number of clocks required between RAS commands to the same bank.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RAS2PCHRGDLY<4:0>:** RAS-to-Precharge Delay bits
These bits specify the minimum number of clocks required from a RAS command to a Precharge command to the same bank.

REGISTER 38-29: DDRPHYDLLR: DDR PHY DLL RECALIBRATE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	DLYSTVAL<3:0>				—	DISRECALIB	RECALIBCNT<17:16>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RECALIBCNT<15:8>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RECALIBCNT<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **DLYSTVAL<3:0>:** Delay Start Value bits
Start value of the digital DLL master delay line. Recommended value is '0011'.

bit 27 **Unimplemented:** Read as '0'

bit 26 **DISRECALIB:** Disable Recalibration bit
1 = Do not recalibrate the digital DLL after the first time
0 = Recalibrate the digital DLL in accordance with the value of the RECALIBCNT<17:0> bits

bit 25-8 **RECALIBCNT<17:0>:** Recalibration Count bits
Determines the period of recalibration of the digital DLL in units of (256 * PHY clock cycles).

bit 7-0 **Unimplemented:** Read as '0'

41.2 Registers

TABLE 41-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FFBC	DEVCFG4	31:16	—	—	—	SWDTPS<4;0>					—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFC0	DEVCFG3	31:16	—	—	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN	—	—	—	—	EXTDDRSIZE<3:0>				xxxx
		15:0	USERID<15:0>																xxxx
FFC4	DEVCFG2	31:16	—	UPLLFSEL	—	FDSEN	DSWDTEN	DSWDTOSC	DSWDTPS<4:0>					DSBOREN	VBATBOREN	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
FFC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
FFCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	POSCAGC	—	POSCTYPE<1:0>		—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>		—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
FFD0	DEVCP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD4	DEVCP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD8	DEVCP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFDC	DEVCP0	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE0	DEVSIGN3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE4	DEVSIGN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE8	DEVSIGN1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFEC	DEVSIGN0	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.