Microchip Technology - PIC32MZ1064DAG169-I/6J Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1064dag169-i-6j

TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
External Bus Interface						
EBIA0	H13	142	N17	O	—	External Bus Interface Address Bus
EBIA1	J11	136	R18	O	—	
EBIA2	C5	33	B9	O	—	
EBIA3	H11	135	R17	O	—	
EBIA4	J12	139	N15	O	—	
EBIA5	A11	174	B18	O	—	
EBIA6	F3	69	K3	O	—	
EBIA7	B12	173	E16	O	—	
EBIA8	N2	96	V9	O	—	
EBIA9	M2	95	T8	O	—	
EBIA10	K3	90	U7	O	—	
EBIA11	L1	91	V7	O	—	
EBIA12	J1	80	U5	O	—	
EBIA13	J2	81	N4	O	—	
EBIA14	G2	74	R6	O	—	
EBIA15	G3	75	T6	O	—	
EBIA16	K12	137	P16	O	—	
EBIA17	L13	134	R16	O	—	
EBIA18	H10	133	P15	O	—	
EBIA19	J10	132	R15	O	—	
EBIA20	M13	131	T18	O	—	
EBIA21	M12	130	T17	O	—	
EBIA22	E8	151	K17	O	—	
EBIA23	L2	92	V8	O	—	
EBID0	C4	40	B7	I/O	ST	External Bus Interface Data I/O Bus
EBID1	A4	40	D8	I/O	ST	
EBID2	N3	36	V10	I/O	ST	
EBID3	M3	99	T9	I/O	ST	
EBID4	B3	98	B6	I/O	ST	
EBID5	B7	43	A12	I/O	ST	
EBID6	F6	17	C11	I/O	ST	
EBID7	C7	23	B11	I/O	ST	
EBID8	K2	24	T7	I/O	ST	
EBID9	L3	89	U9	I/O	ST	
EBID10	A9	97	A15	I/O	ST	
EBID11	G10	10	N18	I/O	ST	
EBID12	A8	143	C13	I/O	ST	
EBID13	G12	14	M16	I/O	ST	
EBID14	L11	144	V17	I/O	ST	
EBID15	H1	127	U6	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-22: DDR2 SDRAM CONTROLLER PINOUT I/O DESCRIPTIONS

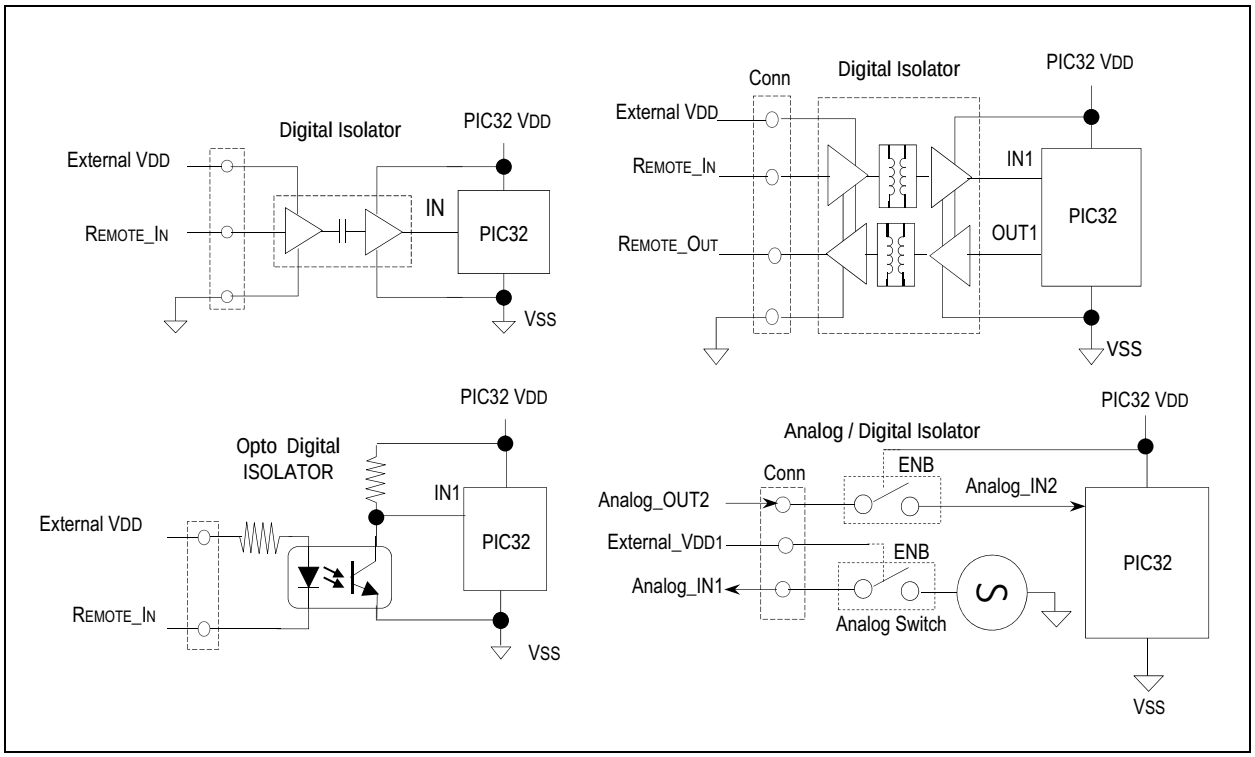
Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
DDR2 SDRAM Controller						
DDRCK	DDR Internal to the Package	DDR Internal to the Package	K2	O	SSTL	Differential Clocks
$\overline{\text{DDRCK}}$			K1	O	SSTL	
DDRCKE			L2	O	SSTL	Clock Enable
$\overline{\text{DDRCS0}}$			N2	O	SSTL	Chip Select 0
$\overline{\text{DDRRAS}}$			M1	O	SSTL	Row Address Strobe
$\overline{\text{DDRCAS}}$			P2	O	SSTL	Column Address Strobe
$\overline{\text{DDRWE}}$			L1	O	SSTL	Write Enable Strobe
DDRLDM			G3	O	SSTL	Lower Data Byte Mask
DDRUDM			A3	O	SSTL	Upper Data Byte Mask
DDRODT			N1	O	SSTL	On-Die Termination
DDRLDQS			E1	I/O	SSTL	Lower Data Byte Qualifier Strobes (Differential)
$\overline{\text{DDRLDQS}}$			E2	I/O	SSTL	
DDRUDQS			B2	I/O	SSTL	Upper Data Byte Qualifier Strobes (Differential)
$\overline{\text{DDRUDQS}}$			A2	I/O	SSTL	
DDRBA0			M2	O	SSTL	Bank Address Select 0
DDRBA1			M3	O	SSTL	Bank Address Select 1
DDRBA2			U4	O	SSTL	Bank Address Select 2
DDRA0			R1	O	SSTL	DDR2 Address Bus
DDRA1			L3	O	SSTL	
DDRA2			N3	O	SSTL	
DDRA3			R2	O	SSTL	
DDRA4			P3	O	SSTL	
DDRA5			T1	O	SSTL	
DDRA6			U1	O	SSTL	
DDRA7			T2	O	SSTL	
DDRA8			U2	O	SSTL	
DDRA9			R3	O	SSTL	
DDRA10			P1	O	SSTL	
DDRA11			V2	O	SSTL	
DDRA12			T3	O	SSTL	
DDRA13			U3	O	SSTL	
DDRA14			T4	O	SSTL	
DDRA15			V3	O	SSTL	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select; SSTL = Stub Series Terminated Logic

TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION

Example Digital/Analog Signal Isolation Circuits	Inductive Coupling	Capacitive Coupling	Opto Coupling	Analog/Digital Switch
ADuM7241 / 40 ARZ (1 Mbps)	X	—	—	—
ADuM7241 / 40 CRZ (25 Mbps)	X	—	—	—
ISO721	—	X	—	—
LTV-829S (2 Channel)	—	—	X	—
LTV-849S (4 Channel)	—	—	X	—
FSA266 / NC7WB66	—	—	—	X

FIGURE 2-6: EXAMPLE DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS



NOTES:

REGISTER 4-1: BFxSEQ3/ABFxSEQ3: BOOT FLASH 'x' SEQUENCE WORD 0 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<7:0>							
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSEQ<15:0>:** Boot Flash Complement Sequence Number bits

bit 15-0 **TSEQ<15:0>:** Boot Flash True Sequence Number bits

Note: The BFxSEQ0 through BFxSEQ2 and ABFxSEQ0 through ABFxSEQ2 registers are used for Quad Word programming operation when programming the BFxSEQ3/ABFxSEQ3 registers, and do not contain any valid information.

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	PFSWAP	BFSWAP	—	—	NVMOP<3:0>				0000
0610	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
0620	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
0630	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
0640	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
0650	NVMDATA2	31:16	NVMDATA2<31:0>																0000
		15:0																	0000
0660	NVMDATA3	31:16	NVMDATA3<31:0>																0000
		15:0																	0000
0670	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
0680	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
0690	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LBWPULOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPULOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF
06A0	NVMCON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00xx
		15:0	—	—	—	—	—	—	—	—	SWAPLOCK<1:0>		—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0, HS	U-0	RW-0, HC	R/W-0, HC	U-0	U-0
	—	—	HVD1V8R	—	BCFGERR	BCFGFAIL	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1, HS	R/W-1, HS
	—	—	—	—	—	—	VBPOR	VBAT
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
	—	—	—	—	—	DPSLP(1)	CMR	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR(1)	POR(1)

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **HVD1V8R:** V_{DDR1V8} (DDR2) High Voltage Detect Flag bit
1 = A high voltage condition on the V_{DDR1V8} voltage has occurred
0 = A high voltage condition on the V_{DDR1V8} voltage has not occurred

bit **Unimplemented:** Read as '0'

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit
1 = An error occurred during a read of the primary configuration registers
0 = No error occurred during a read of the primary configuration registers

bit 26 **BCFGFAIL:** Primary/Secondary Configuration Registers Error Flag bit
1 = An error occurred during a read of the primary and alternate configuration registers
0 = No error occurred during a read of the primary and alternate configuration registers

bit 25-18 **Unimplemented:** Read as '0'

bit 17 **VBPOR:** VBPOR Mode Flag bit
1 = A V_{BAT} domain POR has occurred
0 = A V_{BAT} domain POR has not occurred

bit 16 **VBAT:** VBAT Mode Flag bit
1 = A POR exit from V_{BAT} has occurred (a true POR must be established with the valid V_{BAT} voltage on the V_{BAT} pin)
0 = A POR exit from V_{BAT} has not occurred

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **DPSLP:** Deep Sleep Mode Flag bit(1)
1 = Deep Sleep mode has occurred
0 = Deep Sleep mode has not occurred

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **DMTO:** Deadman Timer Time-out Flag bit
1 = A DMT time-out has occurred
0 = A DMT time-out has not occurred

Note 1: User software must clear this bit to view the next detection.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
External Interrupt 4	_EXTERNAL_4_VECTOR	23	OFF023<17:1>	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	No
Timer5	_TIMER_5_VECTOR	24	OFF024<17:1>	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	No
Input Capture 5 Error	_INPUT_CAPTURE_5_ERROR_VECTOR	25	OFF025<17:1>	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	Yes
Input Capture 5	_INPUT_CAPTURE_5_VECTOR	26	OFF026<17:1>	IFS0<26>	IEC0<26>	IPC6<20:18>	IPC6<17:16>	Yes
Output Compare 5	_OUTPUT_COMPARE_5_VECTOR	27	OFF027<17:1>	IFS0<27>	IEC0<27>	IPC6<28:26>	IPC6<25:24>	No
Timer6	_TIMER_6_VECTOR	28	OFF028<17:1>	IFS0<28>	IEC0<28>	IPC7<4:2>	IPC7<1:0>	No
Input Capture 6 Error	_INPUT_CAPTURE_6_ERROR_VECTOR	29	OFF029<17:1>	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	Yes
Input Capture 6	_INPUT_CAPTURE_6_VECTOR	30	OFF030<17:1>	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	Yes
Output Compare 6	_OUTPUT_COMPARE_6_VECTOR	31	OFF031<17:1>	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
Timer7	_TIMER_7_VECTOR	32	OFF032<17:1>	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
Input Capture 7 Error	_INPUT_CAPTURE_7_ERROR_VECTOR	33	OFF033<17:1>	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	Yes
Input Capture 7	_INPUT_CAPTURE_7_VECTOR	34	OFF034<17:1>	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	Yes
Output Compare 7	_OUTPUT_COMPARE_7_VECTOR	35	OFF035<17:1>	IFS1<3>	IEC1<3>	IPC8<28:26>	IPC8<25:24>	No
Timer8	_TIMER_8_VECTOR	36	OFF036<17:1>	IFS1<4>	IEC1<4>	IPC9<4:2>	IPC9<1:0>	No
Input Capture 8 Error	_INPUT_CAPTURE_8_ERROR_VECTOR	37	OFF037<17:1>	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
Input Capture 8	_INPUT_CAPTURE_8_VECTOR	38	OFF038<17:1>	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
Output Compare 8	_OUTPUT_COMPARE_8_VECTOR	39	OFF039<17:1>	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	No
Timer9	_TIMER_9_VECTOR	40	OFF040<17:1>	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	No
Input Capture 9 Error	_INPUT_CAPTURE_9_ERROR_VECTOR	41	OFF041<17:1>	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
Input Capture 9	_INPUT_CAPTURE_9_VECTOR	42	OFF042<17:1>	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
Output Compare 9	_OUTPUT_COMPARE_9_VECTOR	43	OFF043<17:1>	IFS1<11>	IEC1<11>	IPC10<28:26>	IPC10<25:24>	No
ADC Global Interrupt	_ADC_VECTOR	44	OFF044<17:1>	IFS1<12>	IEC1<12>	IPC11<4:2>	IPC11<1:0>	Yes
ADC FIFO Interrupt	_ADC_FIFO_VECTOR	45	OFF045<17:1>	IFS1<13>	IEC1<13>	IPC11<12:10>	IPC11<9:8>	Yes
ADC Digital Comparator 1	_ADC_DC1_VECTOR	46	OFF046<17:1>	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
ADC Digital Comparator 2	_ADC_DC2_VECTOR	47	OFF047<17:1>	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	Yes
ADC Digital Comparator 3	_ADC_DC3_VECTOR	48	OFF048<17:1>	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
ADC Digital Comparator 4	_ADC_DC4_VECTOR	49	OFF049<17:1>	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes
ADC Digital Comparator 5	_ADC_DC5_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
ADC Digital Comparator 6	_ADC_DC6_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
067C	OFF079	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0680	OFF080	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0684	OFF081	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0688	OFF082	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
068C	OFF083	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0690	OFF084	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0694	OFF085	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0698	OFF086	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
069C	OFF087	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A0	OFF088	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A4	OFF089	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A8	OFF090	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06AC	OFF091	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B0	OFF092	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B4	OFF093	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B8	OFF094	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06BC	OFF095	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06C0	OFF096	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06C4	OFF097	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is only available on devices with a Crypto module.

TABLE 8-1: SYSTEM AND PERIPHERAL CLOCK DISTRIBUTION

Peripheral		Clock Source																
	FRC	LPRC	SOSC	SYSCLK	USBCLK	MPLL	PBCLK1(1)	PBCLK2	PBCLK3	PBCLK4	PBCLK5	PBCLK6	PBCLK7	REFCLKO1	REFCLKO2	REFCLKO3	REFCLKO4	REFOCLK5
CPU													X					
WDT		X		X			X(3)											
DMT				X			X(3)						X					
GLCD				X(3)														X(6)
GPU				X														
DDR2C				X(3)		X												
SDHC											X(3)						X	
Flash	X(2)			X(2)							X(2)							
ADC	X			X					X(3)							X		
Comparator									X(3)									
CTMU									X(3)									
Crypto											X(3)							
RNG											X(3)							
USB					X						X(3)							
USBCR(7)											X(3)							
CAN											X(3)							
Ethernet											X(3)							
PMP								X(3)										
I^2C								X(3)										
UART								X(3)										
RTCC		X	X									X(3)						
EBI				X														
SQI											X(3)				X			
SPI								X						X				
Timers		X	X(4)						X									
Output Compare									X									
Input Capture									X									
Ports										X(3)								
DMA				X														
Interrupts				X														
Prefetch				X														
OSC2 Pin							X(5)											
DSCTRL(8)				X								X						
HLVD							X(3)											

Note 1: PBCLK1 is used by system modules and cannot be turned off.

2: SYSCLK/PBCLK5 is used to fetch data from/to the Flash Controller, while the FRC clock is used for programming.

3: Special Function Register (SFR) access only.

4: Timer1 only.

5: PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.

6: REFCLKO5 (divided version of SPLL clock) is used for the Pixel Clock.

7: USBCR is the Clock/Reset Control block for the USB.

8: DSCTRL is the Deep Sleep Control Block.

18.1 Watchdog Timer Control Registers

TABLE 18-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	WDTCON(1)	31:16	WDTCLRKEY<15:0>																0000
		15:0	ON	—	—	RUNDIV<4:0>					—	—	SLPDIV<4:0>					WDTWINEN	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 26-3: EBISMTx: EXTERNAL BUS INTERFACE STATIC MEMORY TIMING REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>	
23:16	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	PAGEMODE	TPRC<3:0>(1)				TBTA<2:0>(1)		
15:8	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
	TWP<5:0>(1)						TWR<1:0>(1)	
7:0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
	TAS<1:0>(1)		TRC<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **RDYMODE:** Data Ready Device Select bit
The device associated with register set 'x' is a data-ready device, and will use the EBIRDYx pin.
1 = EBIRDYx input is used
0 = EBIRDYx input is not used

bit 25-24 **PAGESIZE<1:0>:** Page Size for Page Mode Device bits
11 = 32-word page
10 = 16-word page
01 = 8-word page
00 = 4-word page

bit 23 **PAGEMODE:** Memory Device Page Mode Support bit
1 = Device supports Page mode
0 = Device does not support Page mode

bit 22-19 **TPRC<3:0>:** Page Mode Read Cycle Time bits(1)
Read cycle time is TPRC + 1 clock cycle.

bit 18-16 **TBTA<2:0>:** Data Bus Turnaround Time bits(1)
Clock cycles (0-7) for static memory between read-to-write, write-to-read, and read-to-read when Chip Select changes.

bit 15-10 **TWP<5:0>:** Write Pulse Width bits(1)
Write pulse width is TWP + 1 clock cycle.

bit 9-8 **TWR<1:0>:** Write Address/Data Hold Time bits(1)
Number of clock cycles to hold address or data on the bus.

bit 7-6 **TAS<1:0>:** Write Address Setup Time bits(1)
Clock cycles for address setup time. A value of '0' is only valid in the case of SSRAM.

bit 5-0 **TRC<5:0>:** Read Cycle Time bits(1)
Read cycle time is TRC + 1 clock cycle.

Note 1: Refer to **Section 47. "External Bus Interface (EBI)"** in the *"PIC32 Family Reference Manual"* for the EBI timing diagrams and additional information.

29.2 ADC Control Registers

TABLE 29-2: ADC REGISTER MAP

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B000	ADCCON1	31:16	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>			FRACT	SELRES<1:0>		STRGSRC<4:0>					0060
		15:0	ON	—	SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—	—	IRQVS<2:0>			STRGLVL	—	—	—	0000
B004	ADCCON2	31:16	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>		SAMC<9:0>											0000
		15:0	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>			—	ADCDIV<6:0>							0000
B008	ADCCON3	31:16	ADCSEL<1:0>		CONCLKDIV<5:0>						DIGEN7	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0	0000
		15:0	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT	GLSWTRG	GSWTRG	ADINSEL<5:0>						0000
B00C	ADCTRGMODE	31:16	—	—	—	—	—	—	SH4ALT<1:0>		SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>		0000
		15:0	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0	0000
B010	ADCIMCON1	31:16	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8	0000
		15:0	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0	0000
B014	ADCIMCON2	31:16	DIFF31	SIGN31	DIFF30	SIGN30	DIFF29	SIGN29	DIFF28	SIGN28	DIFF27	SIGN27	DIFF26	SIGN26	DIFF25	SIGN25	DIFF24	SIGN24	0000
		15:0	DIFF23	SIGN23	DIFF22	SIGN22	DIFF21	SIGN21	DIFF20	SIGN20	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16	0000
B018	ADCIMCON3	31:16	—	—	—	—	—	—	—	—	DIFF43	SIGN43	DIFF42	SIGN42	DIFF41	SIGN41	DIFF40	SIGN40	0000
		15:0	DIFF39	SIGN39	DIFF38	SIGN38	DIFF37	SIGN37	DIFF36	SIGN36	DIFF35	SIGN35	DIFF34	SIGN34	DIFF33	SIGN33	DIFF32	SIGN32	0000
B020	ADCGIRQEN1	31:16	AGIEN31	AGIEN30	AGIEN29	AGIEN28	AGIEN27	AGIEN26	AGIEN25	AGIEN24	AGIEN23	AGIEN22	AGIEN21	AGIEN20	AGIEN19	AGIEN18	AGIEN17	AGIEN16	0000
		15:0	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0	0000
B024	ADCGIRQEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	AGIEN43	AGIEN42	AGIEN41	AGIEN40	AGIEN39	AGIEN38	AGIEN37	AGIEN36	AGIEN35	AGIEN34	AGIEN33	AGIEN32	0000
B028	ADCCSS1	31:16	CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16	0000
		15:0	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
B02C	ADCCSS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CSS43	CSS42	CSS41	CSS40	CSS39	CSS38	CSS37	CSS36	CSS35	CSS34	CSS33	CSS32	0000
B030	ADCDSTAT1	31:16	ARDY31	ARDY30	ARDY29	ARDY28	ARDY27	ARDY26	ARDY25	ARDY24	ARDY23	ARDY22	ARDY21	ARDY20	ARDY19	ARDY18	ARDY17	ARDY16	0000
		15:0	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0	0000
B034	ADCDSTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ARDY43	ARDY42	ARDY41	ARDY40	ARDY39	ARDY38	ARDY37	ARDY36	ARDY35	ARDY34	ARDY33	ARDY32	0000
B038	ADCCMPEN1	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B03C	ADCCMP1	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B040	ADCCMPEN2	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B044	ADCCMP2	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B048	ADCCMPEN3	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 30-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

39.0 SECURE DIGITAL HOST CONTROLLER (SDHC)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 57. "Secure Digital Host Controller (SDHC)"** (DS60001334), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The SDHC module uses a 32-bit System Bus master and slave interface to connect the Host system and standard card interface on the device side.

The core has a built-in DMA controller so that data can be automatically transferred between system memory and the SD/SDIO/eMMC card without intervention from the CPU.

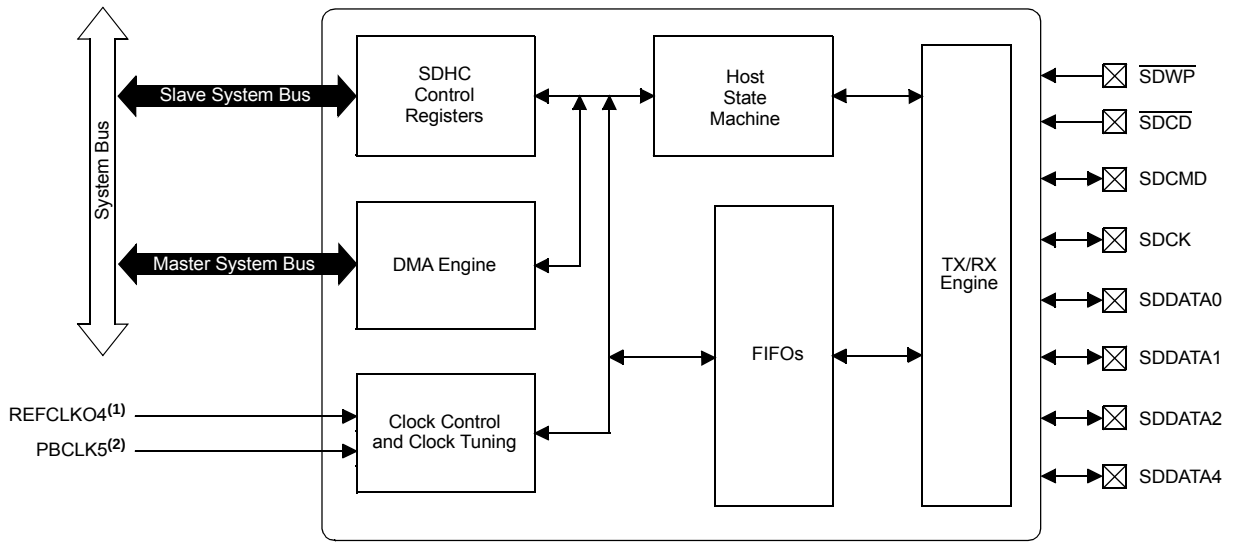
The SDHC module includes the following features:

- SD Association specification compliance:
  - SD Host Controller Simplified Specification, version 2.00
  - Physical Layer Simplified Specification, version 2.00
  - SDIO Simplified Specification, version 2.00
- eMMC Standard: JESD84-A441
- Default and High-Speed modes of operation
- 1-bit or 4-bit data transfers
- Built-in clock divider
- PIO and ADMA modes of data transfer
- 3.3V operation
- Interrupt support
- Stop at block gap

A block diagram of the SDHC module is provided in Figure 39-1.

Note: Transmit and receive buffer addresses in ADMA mode should be word-aligned. When multiple descriptors are used to transfer a single block, all but the last descriptor should have a transfer size in multiples of four.

FIGURE 39-1: SECURE DIGITAL HOST CONTROLLER (SDHC) BLOCK DIAGRAM



Note 1: When configuring the REFCLKO4 clock source, a value of '0' for the ROTRIM<8:0> bits must be selected. REFCLKO4 must be turned on before SDHC Special Function Registers (SFR) access.

2: This clock source is only used for SDHC Special Function Register (SFR) access.

REGISTER 39-4: SDHCRESPx: SDHC RESPONSE REGISTER 'x' ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RESP<31:0>:** Response bits

These bits indicate the bit positions of Responses [31:0] defined in the *"SD Host Controller Simplified Specification* (version 2.00). Refer to Table 39-2 for full bit definitions.

TABLE 39-2: RESPONSE BIT DEFINITION FOR EACH RESPONSE TYPE

Response Type (see Note 1)	Response Meaning	Response Register
R1, R1b (normal response)	Card status	SDHCRESP0<31:0>
R1b (Auto CMD12 response)	Card status for Auto CMD12	SDHCRESP3<31:0>
R2 (CID, CSD register)	CID or CSD register	SDHCRESP0<31:0> SDHCRESP1<31:0> SDHCRESP2<31:0> SDHCRESP3<31:0>
R3 (OCR register)	OCR register for memory	SDHCRESP0<31:0>
R4 (OCR register)	OCR register for I/O, etc.	SDHCRESP0<31:0>
R5, R5b	SDIO response	SDHCRESP0<31:0>
R6 (published RCA response)	New published RCA<31:16>, etc.	SDHCRESP0<31:0>

Note 1: For additional information, refer to the "*SD Host Controller Simplified Specification"* (version 2.00), the "*Physical Layer Simplified Specification"* (version 2.00), and the *"SDIO Simplified Specification"* (version 2.00). These documents are available for download by visiting the SD Association web site at: http://www.sdcard.org/downloads/pls/simplified_specs/archive/index.html

REGISTER 39-8: SDHCCON2: SDHC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0, HC	R/W-0, HC	R/W-0, HC
	—	—	—	—	—	SWRDATA	SWRCMD	SWRALL
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DTOC<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SDCLKDIV<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SDCLKEN	ICLK STABLE	ICLKEN

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **SWRDATA:** Software Reset for DATA Line bit
1 = DMA and part of the data logic are reset
0 = Continue operation

bit 25 **SWRCMD:** Software Reset for CMD Line bit
1 = Clears Present State and Interrupt Status registers and CMD bits
0 = Continue operation

bit 24 **SWRALL:** Software Reset for All bit
1 = Issue reset command and reinitialize the SD card
0 = Divided Clock mode is selected

bit 23-20 **Unimplemented:** Read as '0'

bit 19-16 **DTOC<3:0>:** Data Time-out Counter Value bits
1111 = Reserved
1110 = Time-out clock x 2^{27}
•
•
•
0001 = Time-out clock x 2^{14}
0000 = Time-out clock x 2^{13}

bit 15-8 **SDCLKDIV<7:0>:** SDCLK Divider Select bits
When 8-bit Divided Clock mode is selected:
0x80 - Base clock divided by 256
0x40 - Base clock divided by 128
0x20 - Base clock divided by 64
0x10 - Base clock divided by 32
0x08 - Base clock divided by 16
0x04 - Base clock divided by 8
0x02 - Base clock divided by 4
0x01 - Base clock divided by 2
0x00 - Base clock

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **SDCLKEN:** SD Clock Enable bit
1 = SD clock is enabled
0 = SD clock is disabled

bit 1 **ICLKSTABLE:** Internal Clock Stable bit
1 = Internal clock is ready
0 = Internal clock is not ready

bit 0 **ICLKEN:** Internal Clock Enable bit
1 = Oscillate
0 = Stop

NOTES:

43.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

43.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 44-54: EBI TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EB10	TEBICLK	Internal EBI Clock Period (SYSCLK)	5	—	—	ns	—
EB11	TEBIRC	EBI Read Cycle Time (TRC<5:0>)	10	—	—	ns	—
EB12	TEBIPRC	EBI Page Read Cycle Time (TPRC<3:0>)	10	—	—	ns	—
EB13	TEBIAS	EBI Write Address Setup (TAS<1:0>)	5	—	—	ns	—
EB14	TEBIWP	EBI Write Pulse Width (TWP<5:0>)	5	—	—	ns	—
EB15	TEBIWR	EBI Write Recovery Time (TWR<1:0>)	5	—	—	ns	—
EB16	TEBICO	EBI Output Control Signal Delay	—	—	5	ns	See **Note 1**
EB17	TEBIDO	EBI Output Data Signal Delay	—	—	5	ns	See **Note 1**
EB18	TEBIDS	EBI Input Data Setup	2.5	—	—	ns	See **Note 1**
EB19	TEBIDH	EBI Input Data Hold	1.5	—	—	ns	See **Note 1, 2**

Note 1: Maximum pin capacitance = 10 pF.

2: Hold time from EBI Address change is 0 ns.

TABLE 44-55: GLCD CONTROLLER TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
GD20	tGCLK	Pixel Clock Frequency	—	—	50	MHz	—