Microchip Technology - PIC32MZ1064DAG169T-I/6J Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1064dag169t-i-6j

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07B0	OFF156	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B4	OFF157	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B8	OFF158	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07BC	OFF159	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C0	OFF160	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C4	OFF161	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C8	OFF162	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07CC	OFF163	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D0	OFF164	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D4	OFF165	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D8	OFF166	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07DC	OFF167	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is only available on devices with a Crypto module.

REGISTER 11-6: USBIE0CSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	NAKLIM<4:0>				
23:16	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SPEED<1:0>		—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	RXCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **NAKLIM<4:0>:** Endpoint 0 NAK Limit bits

The number of frames/microframes (Hi-Speed transfers) after which Endpoint 0 should time-out on receiving a stream of NAK responses.

bit 23-22 **SPEED<1:0>:** Operating Speed Control bits
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-7 **Unimplemented:** Read as '0'

bit 6-0 **RXCNT<6:0>:** Receive Count bits

The number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while the RXPKTRDY bit is set.

NOTES:

REGISTER 22-4: SQI1CON: SQI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	r-0	R/W-0
	—	—	—	—	—	—	—	SCHECK(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DDRMODE	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<7:0>							

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **Reserved:** Must be programmed as '0'

bit 24 **SCHECK:** Flash Status Check bit(1)
- 1 = Check the status of the Flash
- 0 = Do not check the status of the Flash

bit 23 **DDRMODE:** Double Data Rate Mode bit
- 1 = Set the SQI transfers to DDR mode
- 0 = Set the SQI transfers to SDR mode

bit 22 **DASSERT:** Chip Select Assert bit
- 1 = Chip Select is deasserted after transmission or reception of the specified number of bytes
- 0 = Chip Select is not deasserted after transmission or reception of the specified number of bytes

bit 21-20 **DEVSEL<1:0>:** SQI Device Select bits
- 11 = Reserved
- 10 = Reserved
- 01 = Select Device 1
- 00 = Select Device 0

bit 19-18 **LANEMODE<1:0>:** SQI Lane Mode Select bits
- 11 = Reserved
- 10 = Quad Lane mode
- 01 = Dual Lane mode
- 00 = Single Lane mode

bit 17-16 **CMDINIT<1:0>:** Command Initiation Mode Select bits

If it is Transmit, commands are initiated based on a write to the transmit register or the contents of TX buffer. If CMDINIT is Receive, commands are initiated based on reads to the read register or RX buffer availability.
- 11 = Reserved
- 10 = Receive
- 01 = Transmit
- 00 = Idle

bit 15-0 **TXRXCOUNT<15:0>:** Transmit/Receive Count bits

These bits specify the total number of bytes to transmit or received (based on CMDINIT).

Note 1: When this bit is set to '1', the SQI module uses the SQI1MEMSTAT register to control the status check command process.

REGISTER 25-5: PMDIN: PARALLEL PORT INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAIN<15:0>:** Port Data Input bits

This register is used for both Parallel Master Port mode and Enhanced Parallel Slave mode.

In Parallel Master mode, a write to the MSB triggers the write transaction on the PMP port. Similarly, a read to the MSB triggers the read transaction on the PMP port.

When MODE16 = 1, MSB = DATAIN<15:8>. When MODE16 = 0, MSB = DATAIN<7:0>.

Note: This register is not used in Dual Buffer Master mode (i.e., DUALBUF bit (PMPCON<17>) = 1).

26.1 EBI Control Registers

TABLE 26-1: EBI REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1014	EBICS0	31:16	CSADDR<15:0>																2000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1018	EBICS1	31:16	CSADDR<15:0>																1000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
101C	EBICS2	31:16	CSADDR<15:0>																2040
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1020	EBICS3	31:16	CSADDR<15:0>																1040
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1054	EBIMSK0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
1058	EBIMSK1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
105C	EBIMSK2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1060	EBIMSK3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1094	EBISMT0	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
1098	EBISMT1	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
109C	EBISMT2	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
10A0	EBIFTRPD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRPD<11:0>												00C8
10A4	EBISMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SMDWIDTH2<2:0>			SMDWIDTH1<2:0>			SMDWIDTH0<2:0>			—	—	—	—	—	—	SMRP	0201

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 29-21: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	AINID<4:0>				
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **AINID<4:0>:** Digital Comparator '*x*' Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by the Digital Comparator.

Note: Only analog inputs <31:0> can be processed by the Digital Comparator module '*x*' ('*x*' = 1-5).

11111 = AN31 is being monitored
11110 = AN30 is being monitored
•
•
•
00001 = AN1 is being monitored
00000 = AN0 is being monitored

bit 7 **ENDCMP:** Digital Comparator '*x*' Enable bit

1 = Digital Comparator '*x*' is enabled
0 = Digital Comparator '*x*' is not enabled, and the DCMPED status bit (ADCCMP*x*CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator '*x*' Global Interrupt Enable bit

1 = A Digital Comparator '*x*' interrupt is generated when the DCMPED status bit (ADCCMP*x*CON<5>) is set
0 = A Digital Comparator '*x*' interrupt is disabled

bit 5 **DCMPED:** Digital Comparator '*x*' "Output True" Event Status bit

The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI and IELOLO bits.

Note: This bit is cleared by reading the AINID<5:0> bits (ADCCMP0CON<13:8>) or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator '*x*' output true event has occurred (output of Comparator is '1')
0 = Digital Comparator '*x*' output is false (output of Comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator '*x*' Event bit

1 = Generate a digital comparator event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate a digital comparator event

bit 3 **IEHIHI:** High/High Digital Comparator '*x*' Event bit

1 = Generate a Digital Comparator '*x*' Event when the DCMPHI<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 2 **IEHILO:** High/Low Digital Comparator '*x*' Event bit

1 = Generate a Digital Comparator '*x*' Event when the DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate an event

REGISTER 29-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

bit 5-6 **Unimplemented:** Read as '0'

bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

31.1 Ethernet Control Registers

TABLE 31-3: ETHERNET CONTROLLER REGISTER SUMMARY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	ETHCON1	31:16	PTV<15:0>																0000
		15:0	ON	—	SIDL	—	—	—	TXRTS	RXEN	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC	0000
2010	ETHCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RXBUFSZ<6:0>							—	—	—	—	0000
2020	ETHTXST	31:16	TXSTADDR<31:16>																0000
		15:0	TXSTADDR<15:2>														—	—	0000
2030	ETHRXST	31:16	RXSTADDR<31:16>																0000
		15:0	RXSTADDR<15:2>														—	—	0000
2040	ETHHT0	31:16	HT<31:0>																0000
		15:0																	0000
2050	ETHHT1	31:16	HT<63:32>																0000
		15:0																	0000
2060	ETHPMM0	31:16	PMM<31:0>																0000
		15:0																	0000
2070	ETHPMM1	31:16	PMM<63:32>																0000
		15:0																	0000
2080	ETHPMCS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMCS<15:0>																0000
2090	ETHPMO	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMO<15:0>																0000
20A0	ETHRXFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	HTEN	MPEN	—	NOTPM	PMMODE<3:0>				CRC ERREN	CRC OKEN	RUNT ERREN	RUNTEN	UCEN	NOT MEEN	MCEN	BCEN	0000
20B0	ETHRXWM	31:16	—	—	—	—	—	—	—	—	RXFWM<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	RXEWM<7:0>								0000
20C0	ETHIEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TX BUSEIE	RX BUSEIE	—	—	—	EW MARKIE	FW MARKIE	RX DONEIE	PK TPENDIE	RX ACTIE	—	TX DONEIE	TX ABORTIE	RX BUFNAIE	RX OVFLWIE	0000
20D0	ETHIRQ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW	0000
20E0	ETHSTAT	31:16	—	—	—	—	—	—	—	—	BUFCNT<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	BUSY	TXBUSY	RXBUSY	—	—	—	—	—	0000
2100	ETH RXOVFLOW	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVFLWCNT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values default to the factory programmed value.

REGISTER 31-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR4<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR3<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits
These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits
These bits hold the third transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

REGISTER 35-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current
10 = 10 times base current
01 = Base current level
00 = 1000 times base current(4)

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<2:0> bits must be set to '1110' to select the C2OUT pin.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 44-20) in **Section 44.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

REGISTER 36-14: GLCDLxRES: GRAPHICS LCD CONTROLLER LAYER 'x' RESOLUTION REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESX<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **RESX<10:0>:** X Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the X dimension.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **RESY<10:0>:** Y Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the Y dimension.

REGISTER 36-19: GLCDCURLUTx: GRAPHICS LCD CONTROLLER CURSOR LUT REGISTER 'x' ('x' = 0-15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RED<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RED<7:0>:** Cursor Lookup Table Red Component bit

bit 15-8 **GREEN<7:0>:** Cursor Lookup Table Green Component bit

bit 7-0 **BLUE<7:0>:** Cursor Lookup Table Blue Component bit

Note: The bits in this register contain the 8-bit RGB color value (0-255).

REGISTER 38-1: DDRTSEL: DDR TARGET SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TSEL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **TSEL<7:0>:** Target Select bits

These bits select the target to program arbitration parameters. This field must be set before an arbitration parameter is programmed for a target. The value in this field represents the target number (0-4) multiplied by the field size of the arbitration parameter.

REGISTER 38-4: DDRMINCMD: DDR MINIMUM COMMAND REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	MINCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **MINCMD<7:0>:** Minimum Command bits

These bits in conjunction with the RQPER<7:0> bits (DDRRQPER<7:0>) determine the percentage of total bandwidth that is allocated to the target. If the number of DDR bursts specified by MINCMD<7:0> are not serviced for the target when it has been requesting access for (RQPER<7:0> * 4) number of clocks, then the target's requests are treated with high priority until this condition becomes satisfied.

Note: The TSEL<7:0> bits (DDRTSEL<7:0>) must be programmed with the target number multiplied by the size of the MINLIMIT field (5) before this register is used to program the minimum burst limit for that target.

TABLE 44-8: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial	
Parameter No.	**Typical(2)**	**Maximum**	**Units**	**Conditions**
Idle Current (I_{IDLE}): Core Off, Clock on Base Current (1)				
DC30	19	35	mA	8 MHz(3)
DC31	55	70	mA	100 MHz(3)
DC32	90	123	mA	200 MHz

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- V_{DDR1V8} = 1.8V
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBPMD = 1), V_{USB3V3} is connected to V_{SS}, PBCLKx divisor = 1:2 ('x' ≠ 7)
- CPU is in Idle mode (CPU core Halted)
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared (except USBPMD)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DDIO}
- RTCC and JTAG are disabled
- I/O Analog Charge Pump is disabled (IOANCPEN bit (CFGCON<7>) = 0)
- ADC Input Charge Pump is disabled (AICPMPEN bit (ADCCON1<12> = 0)

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

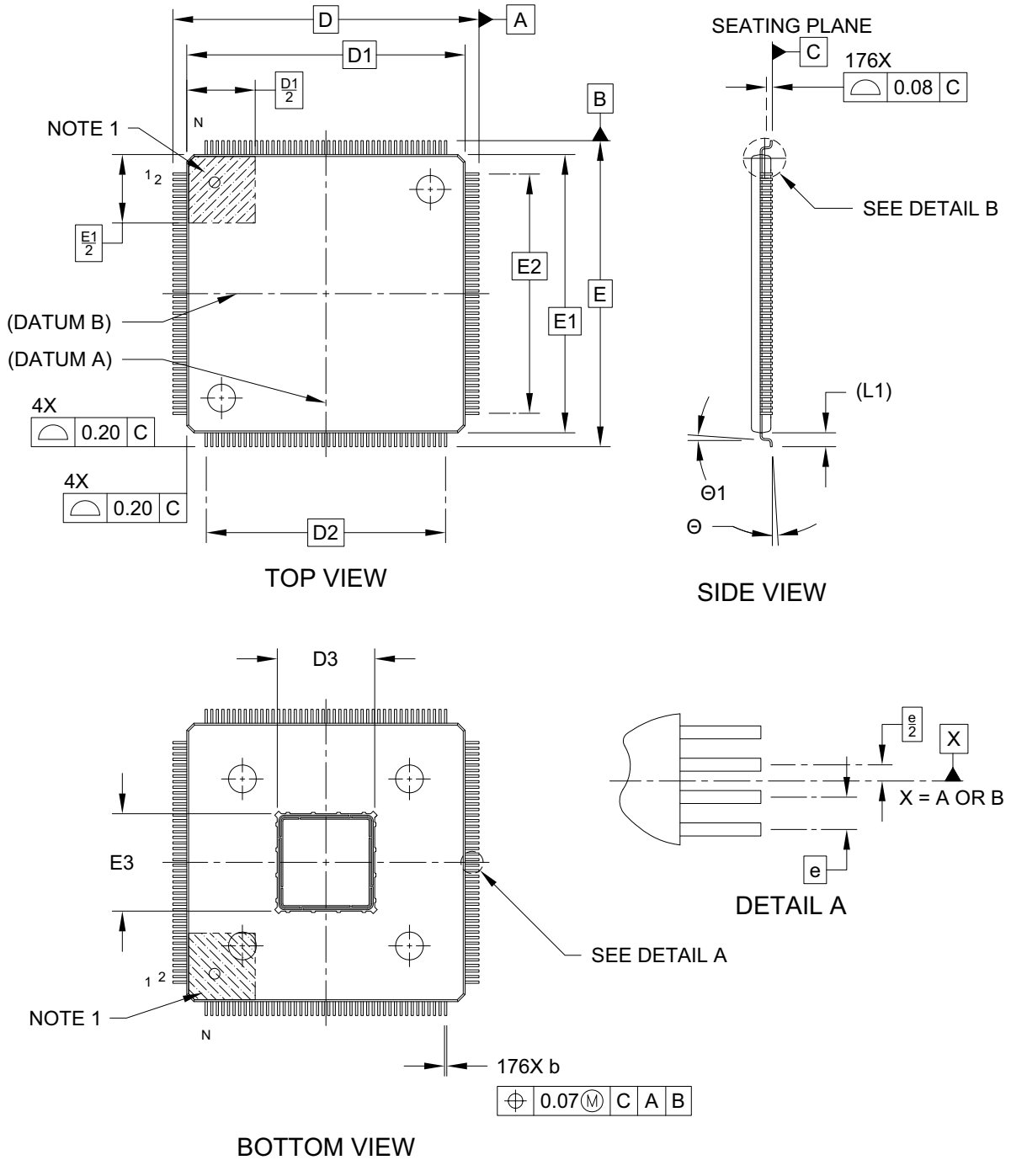
TABLE 44-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20	VOH	**Output High Voltage** I/O Pins 4x Sink Driver Pins - RA0-RA3, RA9, RA10, RA14, RA15 RB0, RB4, RB6, RB7, RB10, RB11, RB12, RB14 RC12-RC15 RD6, RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8, RF12 RG15 RH0, RH1, RH4-RH14 RJ0-RJ2, RJ8, RJ9, RJ11	2.4	—	—	V	$I_{OH} \geq$ -10 mA, V_{DDIO} = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins - RA4, RA5 RB2, RB3, RB5, RB8, RB9, RB13, RB14, RB15 RC1-RC4 RD0-RD3, RD9, RD10, RD12, RD13 RE0-RE7 RF0, RF1, RF4, RF5, RF13 RG0, RG1, RG6, RG7, RG8, RG9 RH2, RH3, RH7, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	2.4	—	—	V	$I_{OH} \geq$ -15 mA, V_{DDIO} = 3.3V
		Output High Voltage I/O Pins: 12x Source Driver Pins - RA6, RA7 RD4, RD5 RG12-RG14	2.4	—	—	V	$I_{OH} \geq$ -20 mA, V_{DDIO} = 3.3V

Note 1: Parameters are characterized, but not tested.

176-Lead Low Profile Quad Flat Pack (2J) - 20x20x1.4 mm Body [LQFP] With 7x7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-367A Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (July 2015)

This is the initial released version of the document.

Revision B (November 2015)

In this revision, the document status has been updated from Advance Information to Preliminary.

This revision includes the following major changes, which are referenced by their respective chapter in Table A-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology	The pin names for 169-pin devices were updated (see Table 5). The pin names for 288-pin devices were updated (see Table 7).
4.0 “Memory Organization”	The Boot Flash Sequence and Configuration Word Summary tables were updated (see Table 4-3 and Table 4-4). The BFxSEQ3/ABFxSEQ3: Boot Flash ‘x’ Sequence Word 0 Register was updated (see Register 4-1).
6.0 “Resets”	The All Resets values were updated for the RCON register in the Resets Register Map (see Table 6-1).
7.0 “CPU Exceptions and Interrupt Controller”	The OFF199 register was added to the Interrupt Register Map (see Table 7-3).
8.0 “Oscillator Configuration”	The All Resets values for the OSCON and PB6DIV registers were updated in the Oscillator Register Map (see Table 8-2). The PLLODIV<2:0> bit values in the SPLLCON register were updated (see Register 8-3).
10.0 “Direct Memory Access (DMA) Controller”	The All Resets values were updated in the DMA Channel 0 through Channel 7 Register Map (see Table 10-3).
11.0 “Hi-Speed USB with On-The-Go (OTG)”	The All Resets value for bits 15:0 of the USBOTG register was updated in the USB Register Map 1 (see Table 11-1). The value at POR was updated for bits 24 and 13 of the USBCRCON register (see Register 11-30).
12.0 “I/O Ports”	The TRISC bits in the PORTC Register Map were updated (see Table 12-5). The ANSH3 bit was added to the ANSELH register in the PORTH Register Map (see Table 12-10). The RPD15R register was removed from the Peripheral Pin Select Output Register Map (see Table 12-14).
18.0 “Watchdog Timer (WDT)”	The All Resets value for bits 15:0 of the WDTCON register in the Watchdog Timer Register Map was updated (see Table 18-1).
21.0 “Serial Peripheral Interface (SPI) and Inter-IC Sound (I^{2S})”	The All Resets value for bits 15:0 of the SPI1STAT and SPI1CON2 registers in the Watchdog Timer Register Map were updated (see Table 21-1).
22.0 “Serial Quad Interface (SQI)”	The All Resets value for bits 15:0 of the SQI1XCON1 register in the Serial Quadrature Interface (SQI) Register Map was updated (see Table 22-1).

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