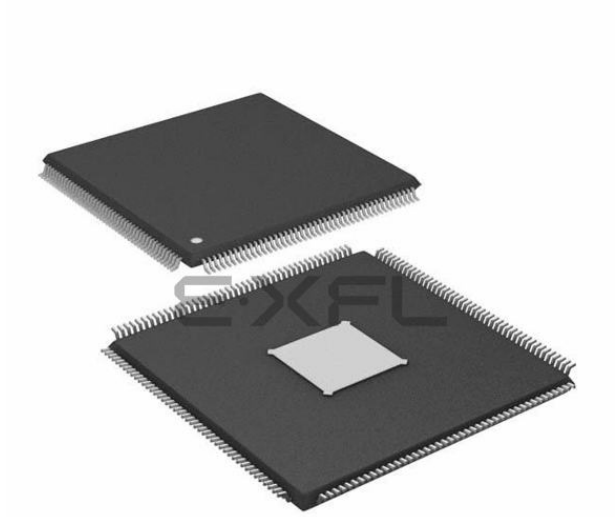

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Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
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Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1064dag176t-i-2j

NOTES:

REGISTER 4-2: SBFLAG0: SYSTEM BUS STATUS FLAG REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	T0PGV0(1)	T3PGV	T6PGV	T2PGV	T5PGV	T4PGV	T1PGV

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-7 **Unimplemented:** Read as '0'

bit 6 **T0PGV0:** Target 0 (System Bus 0) Permission Group Violation Status bit(1)
- 1 = Target 0 (System Bus 0) is reporting a Permission Group (PG) violation
- 0 = Target 0 (System Bus 0) is not reporting a PG violation

bit 5 **T3PGV:** Target 3 (RAM Bank 2) Permission Group Violation Status bit
- 1 = Target 3 is reporting a Permission Group (PG) violation
- 0 = Target 3 is not reporting a PG violation

bit 4 **T6PGV:** Target 6 (EBI) Permission Group Violation Status bit
- 1 = Target 6 is reporting a Permission Group (PG) violation
- 0 = Target 6 is not reporting a PG violation

bit 3 **T2PGV:** Target 2 (RAM Bank 1) Permission Group Violation Status bit
- 1 = Target 2 is reporting a Permission Group (PG) violation
- 0 = Target 2 is not reporting a PG violation

bit 2 **T5GV:** Target 5 (DDR2 Target 1 and Target 2) Permission Group Violation Status bit
- 1 = Target 5 is reporting a Permission Group (PG) violation
- 0 = Target 5 is not reporting a PG violation

bit 1 **T4PGV:** Target 4 (DDR2 Target 0) Permission Group Violation Status bit
- 1 = Target 4 is reporting a Permission Group (PG) violation
- 0 = Target 4 is not reporting a PG violation

bit 0 **T1PGV:** Target 1 (Flash Memory) Permission Group Violation Status bit
- 1 = Target 1 is reporting a Permission Group (PG) violation
- 0 = Target 1 is not reporting a PG violation

Note 1: System Bus 0 represents an internal sub-system element and should be treated as a general System Bus violation.

Note: All errors are cleared at the source (i.e., SBTxELOG1, SBTxELOG2, SBTxECLRS, or SBTxECLRM registers).

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO(1)	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>(1)				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP(1)	CRCTYP	—	—	CRCCH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1)

When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R-0	R/W-0
	AUTOCLR	ISO AUTORQ	DMAREQEN	DISNYET PIDERR	DMAREQMD	— DATATWEN	— DATATGGL	INCOMPRX
23:16	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0, HC	R-0, HS	R/W-0, HS	R-0, HS, HC	R/W-0, HS
	CLRDT	SENTSTALL RXSTALL	SENDSTALL REQPKT	FLUSH	DATAERR DERRNAKT	OVERRUN ERROR	FIFOFULL	RXPKTRDY
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					RXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXMAXP<7:0>							

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AUTOCLR:** RXPKTRDY Automatic Clear Control bit

1 = RXPKTRDY will be automatically cleared when a packet of RXMAXP bytes has been unloaded from the RX FIFO. When packets of less than the maximum packet size are unloaded, RXPKTRDY will have to be cleared manually. When using a DMA to unload the RX FIFO, data is read from the RX FIFO in 4-byte chunks regardless of the RXMAXP.

0 = No automatic clearing of RXPKTRDY

This bit should not be set for high-bandwidth Isochronous endpoints.

bit 30 **ISO:** Isochronous Endpoint Control bit (*Device mode*)

1 = Enable the RX endpoint for Isochronous transfers

0 = Enable the RX endpoint for Bulk/Interrupt transfers

AUTORQ: Automatic Packet Request Control bit (*Host mode*)

1 = REQPKT will be automatically set when RXPKTRDY bit is cleared.

0 = No automatic packet request

This bit is automatically cleared when a short packet is received.

bit 29 **DMAREQEN:** DMA Request Enable Control bit

1 = Enable DMA requests for the RX endpoint.

0 = Disable DMA requests for the RX endpoint.

bit 28 **DISNYET:** Disable NYET Handshakes Control/PID Error Status bit (*Device mode*)

1 = In Bulk/Interrupt transactions, disables the sending of NYET handshakes. All successfully received RX packets are ACKed including at the point at which the FIFO becomes full.

0 = Normal operation.

In Bulk/Interrupt transactions, this bit only has any effect in Hi-Speed mode, in which mode it should be set for all Interrupt endpoints.

PIDERR: PID Error Status bit (*Host mode*)

1 = In ISO transactions, this indicates a PID error in the received packet.

0 = No error

bit 27 **DMAREQMD:** DMA Request Mode Selection bit

1 = DMA Request Mode 1

0 = DMA Request Mode 0

TABLE 12-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15C8	RPD2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD2R<3:0>				0000
15CC	RPD3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD3R<3:0>				0000
15D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD4R<3:0>				0000
15D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD5R<3:0>				0000
15D8	RPD6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD6R<3:0>				0000
15DC	RPD7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD7R<3:0>				0000
15E4	RPD9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD9R<3:0>				0000
15EC	RPD11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD11R<3:0>				0000
15F0	RPD12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD12R<3:0>				0000
15F8	RPD14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD14R<3:0>				0000
160C	RPE3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE3R<3:0>				0000
1614	RPE5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE5R<3:0>				0000
1620	RPE8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE8R<3:0>				0000
1624	RPE9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE9R<3:0>				0000
1640	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF0R<3:0>				0000
1644	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF1R<3:0>				0000
1648	RPF2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF2R<3:0>				0000
164C	RPF3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF3R<3:0>				0000
1650	RPF4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF4R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

15.1 Input Capture Control Registers

TABLE 15-2: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0																	xxxx
2200	IC2CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0																	xxxx
2400	IC3CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0																	xxxx
2600	IC4CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0																	xxxx
2800	IC5CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0																	xxxx
2A00	IC6CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2A10	IC6BUF	31:16	IC6BUF<31:0>																xxxx
		15:0																	xxxx
2C00	IC7CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2C10	IC7BUF	31:16	IC7BUF<31:0>																xxxx
		15:0																	xxxx
2E00	IC8CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2E10	IC8BUF	31:16	IC8BUF<31:0>																xxxx
		15:0																	xxxx
3000	IC9CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3010	IC9BUF	31:16	IC9BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

TABLE 22-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2044	SQI1BD STAT	31:16	—	—	—	—	—	—	—	—	—	—	BDSTATE<3:0>				DMA START	DMAACTV	0000
		15:0	BDCON<15:0>																0000
2048	SQI1BD POLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	POLLCON<15:0>																0000
204C	SQI1BD TXDSTAT	31:16	—	—	—	TXSTATE<3:0>				—	—	—	TXBUFCNT<5:0>						0000
		15:0	—	—	—	—	—	—	—	TXCURBUFLEN<8:0>									0000
2050	SQI1BD RXDSTAT	31:16	—	—	—	RXSTATE<3:0>				—	—	—	RXBUFCNT<5:0>						0000
		15:0	—	—	—	—	—	—	—	RXCURBUFLEN<8:0>									0000
2054	SQI1THR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THRES<3:0>				0000
2058	SQI1INT SIGEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE	0000
205C	SQI1 TAPCON	31:16	—	—	DDRCLKINDLY<5:0>						SDRDATINDLY<3:0>				DDRDATINDLY<3:0>				0000
		15:0	—	—	SDRCLKINDLY<5:0>						DATAOUTDLY<3:0>				CLKOUTDLY<3:0>				0000
2060	SQI1 MEMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	STATPOS	TYPESTAT<1:0>		STATBYTES<1:0>		0000
		15:0	STATCMD<15:0>																0000
2064	SQI1 XCON3	31:16	—	—	—	INIT1 SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>		INIT1CMD3<7:0>								0000
		15:0	INIT1CMD2<7:0>								INIT1CMD1<7:0>								0000
2068	SQI1 XCON4	31:16	—	—	—	INIT2 SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>		INIT2CMD3<7:0>								0000
		15:0	INIT2CMD2<7:0>								INIT2CMD1<7:0>								0000

FIGURE 27-6: FORMAT OF BD_DSTADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_DSTADDR<31:24>							
23-16	BD_DSTADDR<23:16>							
15-8	BD_DSTADDR<15:8>							
7-0	BD_DSTADDR<7:0>							

bit 31-0 **BD_DSTADDR:** Buffer Destination Address
The destination address of the buffer that needs to be passed through the PE-CRDMA for encryption or authentication. This address must be on a 32-bit boundary.

FIGURE 27-7: FORMAT OF BD_NXTADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_NXTADDR<31:24>							
23-16	BD_NXTADDR<23:16>							
15-8	BD_NXTADDR<15:8>							
7-0	BD_NXTADDR<7:0>							

bit 31-0 **BD_NXTADDR:** Next BD Pointer Address Has Next Buffer Descriptor
The next buffer can be a next segment of the previous buffer or a new packet.

FIGURE 27-8: FORMAT OF BD_UPDPTR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_UPDADDR<31:24>							
23-16	BD_UPDADDR<23:16>							
15-8	BD_UPDADDR<15:8>							
7-0	BD_UPDADDR<7:0>							

bit 31-0 **BD_UPDADDR:** UPD Address Location
The update address has the location where the CRDMA results are posted. The updated results are the ICV values, key output values as needed.

Step 4: The user sets the ON bit to '1', which enables the ADC control clock. The following ADCx activation sequence is to be followed at all times:

Step 5: The user waits for the interrupt/polls the BGVRRDY bit (ADCCON2<31>) and the WKRDYx bit (ADCANCON<15,13:8>) = 1, which signals that the device analog environment (band gap and VREF) is ready.

Step 6: Set the DIGENx bit (ADCCON3<15,13:8>) to '1', which enables the digital circuitry to immediately begin processing incoming triggers to perform data conversions.

Standard non-interleaved dedicated Class_1 ADCx throughput rate formula is shown in Equation 29-1.

EQUATION 29-1: THROUGHPUT RATE

ADC Throughput Rate = 1/((Sample time + Conversion time)(TAD))
= 1 / ((SAMC+# bit resolution+1)(TAD))

Example:
SAMC = 3 TAD, 12-bit mode, TAD = 20 ns = 50 MHz:
Throughput rate:
= 1 / ((3+13)(20 ns))
= 1/(16 * 20 ns)
= 3.125 msps

TABLE 29-1: PIC32MZXXDAXX INTERLEAVED ADC THROUGHPUT RATES

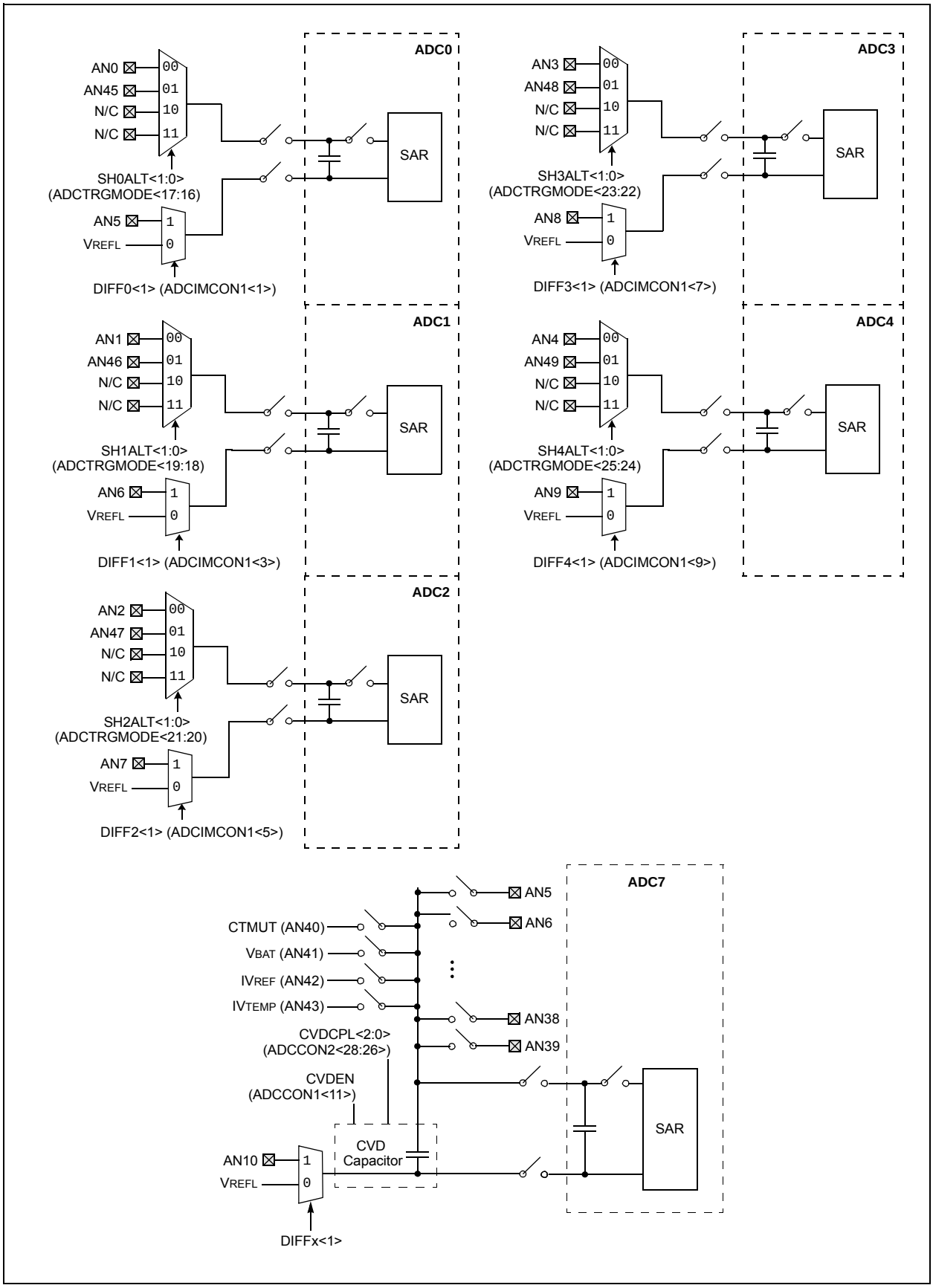
#No.of Interleaved ADC Possible	ADC TAD(min) = 20ns (50Mhz max)			
	12-bit (max.) msps	10-bit (max.) msps	8-bit (max.) msps	6-bit (max.) msps
1	3.125 msps	3.571 msps	4.167 msps	5.0 msps
2	6.250 msps	7.143 msps	8.333 msps	10.00 msps
3	8.330 msps	10.00 msps	12.50 msps	12.50 msps
4	12.50 msps	12.50 msps	16.667 msps	16.667 msps

Note: Interleaved ADCs in this context means connecting the same analog source signal to multiple dedicated Class_1 ADCs (i.e., ADC0-ADC5), and using independent staggered trigger sources accordingly for each interleaved ADC.

Note 1: Prior to enabling the ADC module, the user application must copy the ADC calibration data (DEVADC0-DEVADC4, DEVADC7; see Register 41-8) from the Configuration memory into the ADC Configuration registers (ADC0CFG-ADC4CFG, ADC7CFG).

2: If V_{DDIO} is greater than 2.5V, set the AICPMPEN bit (ADCCON1<12>) and the IOANCPEN bit (CFGCON<7>) to '0'. If V_{DDIO} is less than 2.5V, set both bits to '1'.

FIGURE 29-2: S&H BLOCK DIAGRAM



36.0 GRAPHICS LCD (GLCD) CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 54. "Graphics LCD Controller"** (DS60001379), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Graphics LCD (GLCD) Controller is designed to directly interface with display panels with up to 24-bit color depth.

The GLCD Controller transfers display data from a memory device and formats it for a display device. The memory may be internal RAM or DDR2.

The parallel interface at the pins will operate at standard 3.3V output, requires 28 pins for 24-bit color, and is shared by general purpose I/O functions.

Key features of the GLCD Controller include:

- Supports a 50 MHz Pixel Clock (dependent on DDR2 bandwidth)
- Up to 800x480 (WVGA) with Overlay and smaller with three Overlay layers. High resolution is possible with smaller displays.
- Color depths: 8, 16**(1)**, 18, and 24 bits
- Up to three design timing layers, each including:
  - Configurable Alpha blending
  - Configurable Stride and Pitch
- Input formats: RGBA8888, ARGB8888, RGB888, RGB565, RGBA5551, YUYV, RGB332, LUT8, and Gray-scale
- Output formats: RGB888, RGB666, BT.656
- Dithering for 18-bit displays
- High-quality YUV conversion
- Global color palette look-up table (CLUT) supporting 256 colors
- Global gamma correction, brightness and contrast support
- Programmable cursors supporting 16 colors
- Programmable polarity on HSYNC, VSYNC, DE, and PCLK
- Integrated DMA to offload the CPU
- Programmable (level/edge) interrupt on HSYNC and VSYNC

Note 1: 16-bit color depth is supported through the GLCDMODE bit (CFGCON2<30>). When set, functions shared with GD0, GD1, GD2, GD8, GD9, GD16, GD17, GD18 are available for general purpose use.

A block diagram of the GLCD Controller interface is provided in Figure 36-1.

TABLE 38-1: DDR SDRAM CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
80E8	DDR CMD210	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80EC	DDR CMD211	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80F0	DDR CMD212	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80F4	DDR CMD213	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80F8	DDR CMD214	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80FC	DDR CMD215	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
9100	DDR SCLSTART	31:16	—	—	SCL PHCAL	SCL START	—	SCLEN	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCL UBPASS	SCL LBPASS	0000
910C	DDR SCLLAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—				0000
		15:0	—	—	—	—	—	—	—	—	DDRCLKDLY<3:0>				CAPCLKDLY<3:0>				0000
9118	DDR SCLCFG0	31:16	—	—	—	—	—	—	—	ODTCSW	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RCASLAT<3:0>				—	—	DDR2	BURST8	0000
911C	DDR SCLCFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	DBL REFDLY	WCASLAT<3:0>				—	—	—	—	—	—	—	SCLSEN	0000
9120	DDR PHYPADCON	31:16	—	PREAMBDLY<1:0>		RCVREN	—	—	—	—	DRVSTRPFET<3:0>				DRVSTRNFET<3:0>				0000
		15:0	—	HALF RATE	WR CMDDLY	—	—	—	NOEXT DLL	EOEN CLKCYC	ODTPUCAL<1:0>		ODTPDCAL<1:0>		ADDC DRVSEL	DAT DRVSEL	ODTEN	ODTSEL	0000
9124	DDR PHYDLLR	31:16	DLYSTVAL<3:0>				—	DIS RECALIB	RECALIBCNT<17:8>										0000
		15:0	RECALIBCNT<7:0>								—	—	—	—	—	—	—	—	0000
9128	DDR PHYDLLCTRL	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DDRDLLTRIM<7:0>								0000
9140	DDR PHYCLKDLY	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	SCL UBPASS	SCL LBPASS	—	CLKDLYDELTA<2:0>			0000
915C	DDR ADLLBYP	31:16	—	—	—	—	—	—	—	ANL DLLBYP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
916C	DDR SCLCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLLANSEL<1:0>		0000
9188	DDR PHYSCLADR	31:16	SCLBANKADR<3:0>				SCLCOLADR<12:0>												0000
		15:0	SCLROWADR<15:0>																0000

REGISTER 39-1: SDHCBLKCON: SDHC BLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<15:8>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<7:0>(1)							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	BSIZE<9:8>(2)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BSIZE<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **BCOUNT<31:0>:** Blocks Count for Current Transfer bits(1)

These bits represent the number of blocks. The software sets this value between 1 and 65,535 blocks and the SDHC decrements the count after each block transfer and stops when the count reaches zero.
0xFFFF = 65,535 blocks
0x0002 = 2 blocks
0x0001 = 1 block
0x0000 = Stop count Blocks Count for Current Transfer bits

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **BSIZE<9:0>:** Transfer Block Size bits(2)

These bits specify the block size of the data transfer for CMD17, CMD18, CMD24, CMD25, and CMD53.
0x200 = 512 bytes
0x1FF = 511 bytes
•
•
•
0x002 = 2 bytes
0x001 = 1 byte
0x000 = No data transfer

Note 1: These bits are only used when the BCEN bit (SDHCMODE<1>) is set to '1' and is valid only for multiple block transfers. The BCOUNT<15:0> bits need not be set if the BSIZE bit (SDHCMODE<5>) is set to '0'.

2: These bits can only be accessed when no transactions are in progress. Read operations during transfers will return an invalid value and write operations to these bits will be ignored.

REGISTER 39-12: SDHCSTAT2: SDHC STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HC	U-0	U-0	R-0, HC	R-0, HC	R-0, HC	R-0, HC	R-0, HC
	CNISSE	—	—	ACIDXE	ACEBE	ACCRCE	ACTOE	ACNEXEC

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **CNISSE:** Command Not Issued by Auto CMD12 Error bit
- 1 = Command was not issued
- 0 = No error

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **ACIDXE:** Auto CMD12 Index Error bit
- 1 = Index error was generated
- 0 = Index error was not generated

bit 3 **ACEBE:** Auto CMD12 End Bit Error bit
- 1 = End bit error was generated
- 0 = End bit error was not generated

bit 2 **ACCRCE:** Auto CMD12 CRC Error bit
- 1 = CRC error was generated
- 0 = CRC error was not generated

bit 1 **ACTOE:** Auto CMD12 Time-out Error bit
- 1 = Time-out error was generated
- 0 = Time-out error was not generated

bit 0 **ACNEXEC:** Auto CMD12 Not Executed bit
- 1 = Auto CMD12 was not executed
- 0 = Auto CMD12 was executed

REGISTER 39-16: SDHCADESTAT: SDHC ADMA ERROR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0, HC	R-0, HC	R-0, HC
	—	—	—	—	—	ADLMERR	ADERRST<1:0>	

Legend:			
R = Readable bit	W = Writable bit	HC = Hardware Cleared U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **ADLMERR:** ADMA Length Mismatch Error bit
1 = Length mismatch error has occurred
0 = Length mismatch error has not occurred

bit 1-0 **ADERRST<1:0>:** ADMA Error State bits
11 = Data transfer error
10 = Reserved
01 = Fetch descriptor error
00 = Stop DMA error

REGISTER 39-17: SDHCAADDR: SDHC ADMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ADDR<31:0>:** ADMA Address Register bits
These bits contain the address of the executing command of the ADMA descriptor table.

REGISTER 40-1: DSCON: DEEP SLEEP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	HC, R/W-y	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	DSEN(1)	—	DSGPREN	RTCDIS	—	—	—	RTCCWDIS
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DSBOR(2)	RELEASE

Legend:	HC = Hardware Cleared	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **DSEN:** Deep Sleep Enable bit(1)
- 1 = Deep Sleep mode is entered on a WAIT instruction
- 0 = Sleep mode is entered on a WAIT instruction

bit 14 **Unimplemented:** Read as '0'

bit 13 **DSGPREN:** General Purpose Registers Enable bit
- 1 = General purpose register retention is enabled in Deep Sleep mode
- 0 = No general purpose register retention in Deep Sleep mode

bit 12 **RTCDIS:** RTCC Module Disable bit
- 1 = RTCC module is not enabled
- 0 = RTCC module is enabled

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RTCCWDIS:** RTCC Wake-up Disable bit
- 1 = Wake-up from RTCC is disabled
- 0 = Wake-up from RTCC is enabled

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit(2)
- 1 = DSBOREN was enabled and V_{DDCORE} dropped below the DSBOR threshold during Deep Sleep(2)
- 0 = DSBOREN was disabled, or V_{DDCORE} did not drop below the DSBOR threshold during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit
- 1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states
- 0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

Note 1: To enter Deep Sleep mode, Sleep mode must be executed after setting the DSEN bit.

2: Unlike all other events, a Deep Sleep Brown-out Reset (BOR) event will not cause a wake-up from Deep Sleep mode; this bit is present only as a status bit.

41.3 High-Voltage Detect (HVD1V8) on V_{DDR1V8}

The High-Voltage Detect (HVD) module monitors the DDR2 PHY voltage at the V_{DDR1V8} supply voltage (1.8V). If a dangerously high voltage is detected, the device is held in reset as long as the HVD condition persists.

Recovery from an HVD event is indicated by the HVD1V8R bit (RCON<29>).

41.4 On-Chip Voltage Regulator

The core and digital logic for all PIC32MZ DA devices is designed to operate at a nominal 1.8V. To simplify system designs, devices in the PIC32MZ DA family incorporate an on-chip regulator providing the required core logic voltage from V_{DDIO}.

41.4.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as T_{PU}, code execution is disabled. T_{PU} is applied every time the device resumes operation after any power-down, including Sleep mode.

41.4.2 ON-CHIP REGULATOR AND BOR

PIC32MZ DA devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 44.1 "DC Characteristics"**.

41.5 On-chip Temperature Sensor

PIC32MZ DA devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **Section 44.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **Section 29.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information).

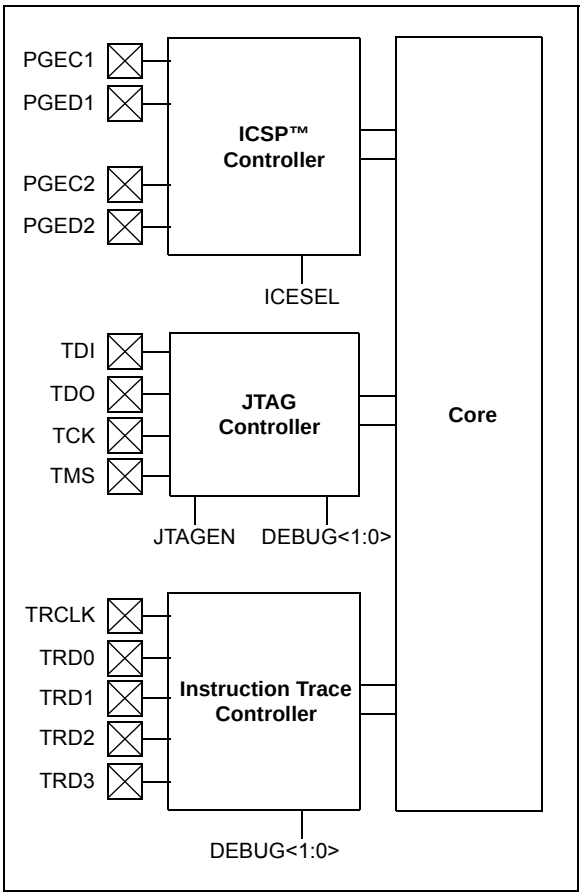
41.6 Programming and Diagnostics

PIC32MZ DA devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 41-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS



44.1 DC Characteristics

TABLE 44-1: OPERATING MIPS VS. VOLTAGE

Characteristic	V_{DDIO} Range (in Volts) (Note 1)	V_{DDCORE} Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comments
				PIC32MZ DA Devices	
DC5	2.2V-3.6V	1.7V-1.9V	-40°C to +85°C	200 MHz	—

Note 1: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

TABLE 44-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DDIO} \times (I_{DD} - S\ I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = S\ (\{V_{DDIO} - V_{OH}\} \times I_{OH}) + S\ (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 44-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 169-pin LFBGA (11x11x1.4 mm)	θ_{JA}	25	—	°C/W	**1**
Package Thermal Resistance, 169-pin LFBGA (11x11x1.56 mm)	θ_{JA}	24	—	°C/W	**1,2**
Package Thermal Resistance, 176-pin LQFP (20x20x1.45 mm)	θ_{JA}	17	—	°C/W	**1**
Package Thermal Resistance, 176-pin LQFP (20x20x1.45 mm)	θ_{JA}	19	—	°C/W	**1,2**
Package Thermal Resistance, 288-pin LFBGA (15x15x1.4 mm)	θ_{JA}	22	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-$_{JA}$ (θ_{JA}) numbers are achieved by package simulations.

2: Devices with internal DDR2 SDRAM.

TABLE 44-42: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

FIGURE 44-20: CANx MODULE I/O TIMING CHARACTERISTICS

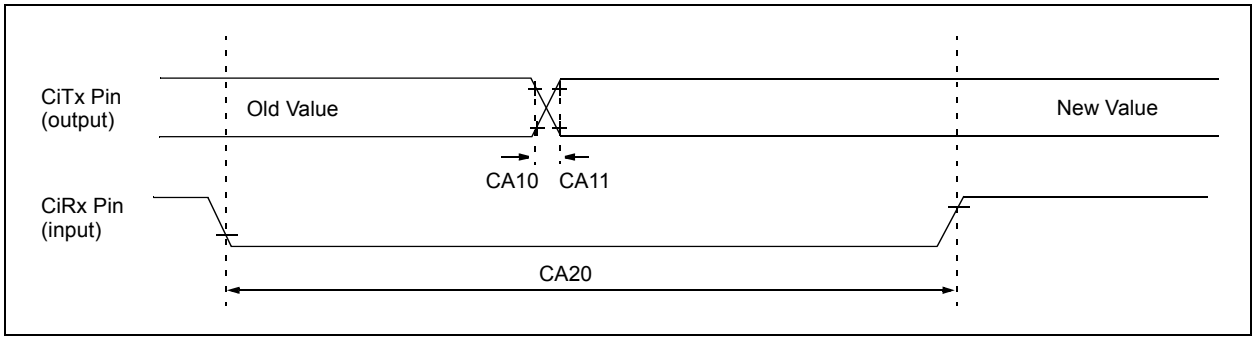


TABLE 44-44: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.