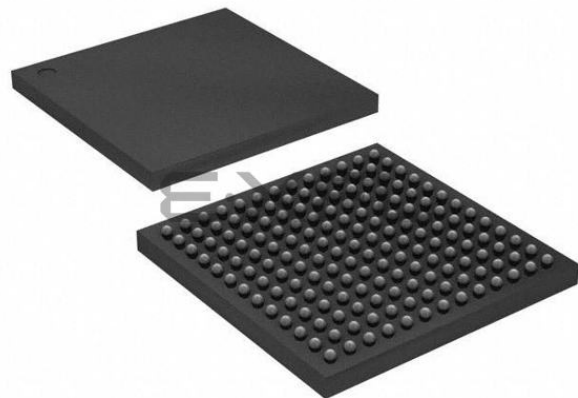




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, PMP, SPI, SQT, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025daa169-i-hf

PIC32MZ Graphics (DA) Family

TABLE 1: PIC32MZ DA FEATURES COMMON TO ALL DEVICES

Boot Flash Memory (KB)	Remappable Peripherals					12-bit ADC Channels	Analog Comparators	CTMU	USB 2.0 HS OTG	I ² C	GLCD	GPU	EBI	PMP	SQI	SDHC	RTCC	Ethernet	I/O Pins	JTAG	Trace
	Remappable Pins	Timers ⁽¹⁾ /Capture/Compare	UART	SPI/I ² S	CAN 2.0B																
160	47	9/9/9	6	6	2	5	45	2	Y	Y	5	Y	Y	Y	Y	Y	Y	Y	120	Y	Y

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.

TABLE 2: 169-PIN LFBGA PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/Dedicated)	
PIC32MZ1025DAA169	1024	256	No	—	N	8/24	
PIC32MZ1025DAB169		640			Y	8/26	
PIC32MZ1064DAA169					N	8/24	
PIC32MZ1064DAB169		2048			256	Y	8/26
PIC32MZ2025DAA169	N					8/24	
PIC32MZ2025DAB169	640				Y	8/26	
PIC32MZ2064DAA169					N	8/24	
PIC32MZ2064DAB169	1024	256			Yes (INT)	32	N
PIC32MZ1025DAG169		640	Y	8/26			
PIC32MZ1025DAH169			N	8/24			
PIC32MZ1064DAG169		2048	256	Y			8/26
PIC32MZ1064DAH169				N			8/24
PIC32MZ2025DAG169			640	Y			8/26
PIC32MZ2025DAH169				N			8/24
PIC32MZ2064DAG169		640	640	N			8/24
PIC32MZ2064DAH169	Y			8/26			

TABLE 3: 176-PIN LQFP PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/Dedicated)
PIC32MZ1025DAA176	1024	256	No	—	N	8/24
PIC32MZ1025DAB176		640			Y	8/26
PIC32MZ1064DAA176					N	8/24
PIC32MZ1064DAB176		2048			256	Y
PIC32MZ2025DAA176	N					8/24
PIC32MZ2025DAB176	640				Y	8/26
PIC32MZ2064DAA176					N	8/24
PIC32MZ2064DAB176	1024	256			Yes (INT)	32
PIC32MZ1025DAG176			640	N		
PIC32MZ1025DAH176		256		Y		
PIC32MZ1064DAG176			2048	640		
PIC32MZ1064DAH176	Y	8/26				
PIC32MZ2025DAG176	256	N		8/24		
PIC32MZ2025DAH176		640		Y		
PIC32MZ2064DAG176	2048		640	N		
PIC32MZ2064DAH176		Y		8/26		

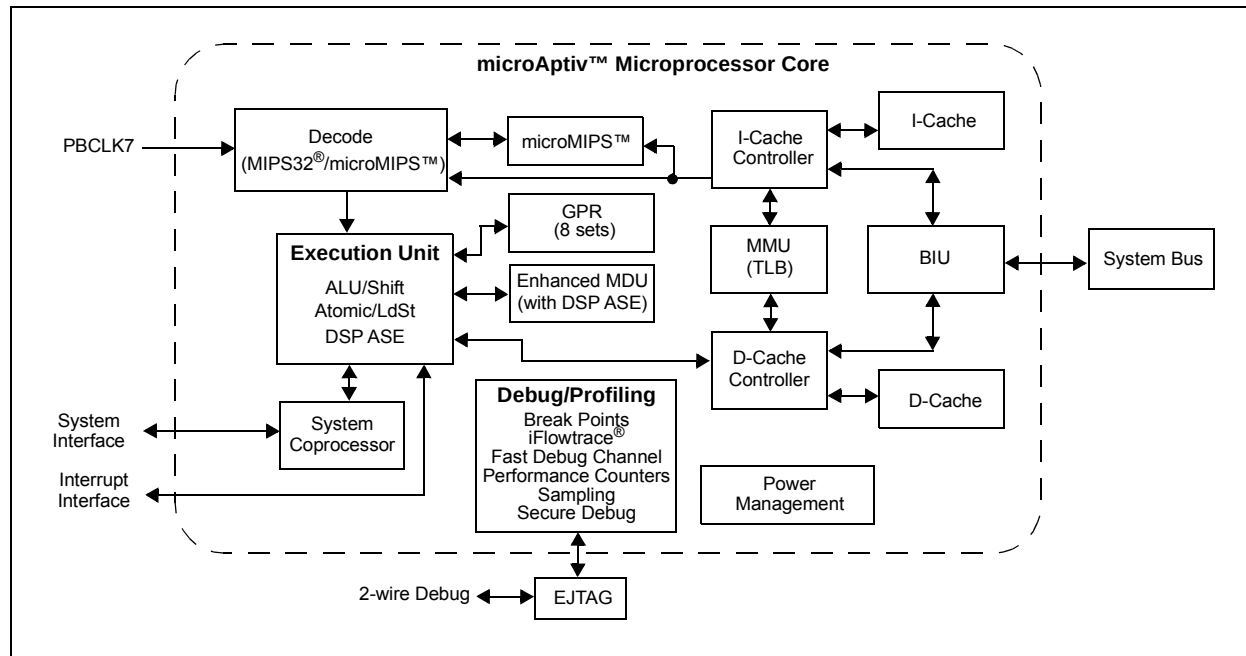
TABLE 4: 288-PIN LFBGA PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	Crypto/RNG	DMA Channels (Programmable/Dedicated)
PIC32MZ1025DAA288	1024	256	Yes (EXT)	N	8/24
PIC32MZ1025DAB288		640		Y	8/26
PIC32MZ1064DAA288				N	8/24
PIC32MZ1064DAB288				Y	8/26
PIC32MZ2025DAA288	2048			256	N
PIC32MZ2025DAB288		Y		8/26	
PIC32MZ2064DAA288		640		N	8/24
PIC32MZ2064DAB288				Y	8/26

PIC32MZ Graphics (DA) Family

A block diagram of the PIC32MZ DA family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ DA FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



PIC32MZ Graphics (DA) Family

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend: r = Reserved
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'
bit 0 **NF:** Nested Fault bit
1 = Nested Fault feature is implemented

REGISTER 3-5: CONFIG7: CONFIGURATION REGISTER 7; CP0 REGISTER 16, SELECT 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	WII	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31 **WII:** Wait IE Ignore bit
1 = Indicates that this processor will allow an interrupt to unblock a WAIT instruction
bit 30-0 **Unimplemented:** Read as '0'

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1380	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1390	PB6DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8803
13A0	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
13C0	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0000
13D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SPLL RDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

TABLE 16-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4A00	OC6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4A10	OC6R	31:16	OC6R<31:0>																XXXX
		15:0	OC6R<31:0>																XXXX
4A20	OC6RS	31:16	OC6RS<31:0>																XXXX
		15:0	OC6RS<31:0>																XXXX
4C00	OC7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4C10	OC7R	31:16	OC7R<31:0>																XXXX
		15:0	OC7R<31:0>																XXXX
4C20	OC7RS	31:16	OC7RS<31:0>																XXXX
		15:0	OC7RS<31:0>																XXXX
4E00	OC8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4E10	OC8R	31:16	OC8R<31:0>																XXXX
		15:0	OC8R<31:0>																XXXX
4E20	OC8RS	31:16	OC8RS<31:0>																XXXX
		15:0	OC8RS<31:0>																XXXX
5000	OC9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5010	OC9R	31:16	OC9R<31:0>																XXXX
		15:0	OC9R<31:0>																XXXX
5020	OC9RS	31:16 15:0	OC9RS<31:0>																XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

PIC32MZ Graphics (DA) Family

REGISTER 17-3: DMTCLR: DEADMAN TIMER CLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP2<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit

-n = Bit Value at POR: ('0', '1', x = unknown)

P = Programmable bit r = Reserved bit

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2<7:0>:** Clear Timer bits

00001000 = Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if, and only if, preceded by correct loading of STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading the DMTCNT bit and observing the counter being reset.

All other write patterns = Set BAD2 bit, the value of STEP1<7:0> will remain unchanged, and the new value being written STEP2<7:0> will be captured. These bits are also cleared when a DMT reset event occurs.

PIC32MZ Graphics (DA) Family

REGISTER 20-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>**: Alarm Repeat Counter Value bits⁽²⁾

11111111 = Alarm will trigger 256 times

•
•
•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

PIC32MZ Graphics (DA) Family

REGISTER 22-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>**: Current DMA Receive State Status bits

These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>**: DMA Buffer Byte Count Status bits

These bits provide information on the internal buffer space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLN<7:0>**: Current DMA Receive Buffer Length Status bits

These bits provide the length of the current DMA receive buffer.

REGISTER 22-21: SQI1THR: SQI THRESHOLD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	THRES<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **THRES<3:0>**: SQI Control Threshold Value bits

The SQI control threshold interrupt is asserted when the amount of space indicated by THRES<6:0> is available in the SQI control buffer.

PIC32MZ Graphics (DA) Family

REGISTER 26-2: EBIMSKx: EXTERNAL BUS INTERFACE ADDRESS MASK REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	REGSEL<2:0>		
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MEMTYPE<2:0>			MEMSIZE<4:0>				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **REGSEL<2:0>**: Timing Register Set for Chip Select 'x' bits

111 = Reserved

•
•
•

011 = Reserved

010 = Use EBISMT2

001 = Use EBISMT1

000 = Use EBISMT0

bit 7-5 **MEMTYPE<2:0>**: Select Memory Type for Chip Select 'x' bits

111 = Reserved

•
•
•

011 = Reserved

010 = NOR-Flash

001 = SRAM

000 = Reserved

bit 4-0 **MEMSIZE<4:0>**: Select Memory Size for Chip Select 'x' bits

11111 = Reserved

•
•
•

01010 = Reserved

01001 = 16 MB

01000 = 8 MB

00111 = 4 MB

00110 = 2 MB

00101 = 1 MB

00100 = 512 KB

00011 = 256 KB

00010 = 128 KB

00001 = 64 KB (smaller memories alias within this range)

00000 = Chip Select is not used

PIC32MZ Graphics (DA) Family

NOTES:

PIC32MZ Graphics (DA) Family

27.2 Crypto Engine Buffer Descriptors

Host software creates a linked list of buffer descriptors and the hardware updates them. Table 27-3 provides a list of the Crypto Engine buffer descriptors, followed by format descriptions of each buffer descriptor (see Figure 27-2 through Figure 27-10).

TABLE 27-3: CRYPTO ENGINE BUFFER DESCRIPTORS

Name (see Note 1)	Bit 31/2315/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
BD_CTRL	31:24	DESC_EN	—	CRY_MODE<2:0>		—	—	—
	23:16	—	SA_FETCH_EN	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
	15:8	BD_BUFLEN<15:8>						
	7:0	BD_BUFLEN<7:0>						
BD_SA_ADDR	31:24	BD_SAADDR<31:24>						
	23:16	BD_SAADDR<23:16>						
	15:8	BD_SAADDR<15:8>						
	7:0	BD_SAADDR<7:0>						
BD_SCRADDR	31:24	BD_SRCADDR<31:24>						
	23:16	BD_SRCADDR<23:16>						
	15:8	BD_SRCADDR<15:8>						
	7:0	BD_SRCADDR<7:0>						
BD_DSTADDR	31:24	BD_DSTADDR<31:24>						
	23:16	BD_DSTADDR<23:16>						
	15:8	BD_DSTADDR<15:8>						
	7:0	BD_DSTADDR<7:0>						
BD_NXTPTR	31:24	BD_NXTADDR<31:24>						
	23:16	BD_NXTADDR<23:16>						
	15:8	BD_NXTADDR<15:8>						
	7:0	BD_NXTADDR<7:0>						
BD_UPDPTR	31:24	BD_UPDADDR<31:24>						
	23:16	BD_UPDADDR<23:16>						
	15:8	BD_UPDADDR<15:8>						
	7:0	BD_UPDADDR<7:0>						
BD_MSG_LEN	31:24	MSG_LENGTH<31:24>						
	23:16	MSG_LENGTH<23:16>						
	15:8	MSG_LENGTH<15:8>						
	7:0	MSG_LENGTH<7:0>						
BD_ENC_OFF	31:24	ENCR_OFFSET<31:24>						
	23:16	ENCR_OFFSET<23:16>						
	15:8	ENCR_OFFSET<15:8>						
	7:0	ENCR_OFFSET<7:0>						

Note 1: The buffer descriptor must be allocated in memory on a 64-bit boundary.

TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
B0AC	ADCCMPCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000	
B0B0	ADCCMPCON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000	
B0B4	ADCCMPCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000	
B0B8	ADCFSTAT	31:16	FEN	—	—	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	FIEN	FRDY	FWROVERR	—	—	—	—	0000		
		15:0	FCNT<7:0>								FSIGN	—	—	—	—	ADCID<2:0>			0000	
B0BC	ADCFIFO	31:16	DATA<31:16>																0000	
		15:0	DATA<15:0>																0000	
B0C0	ADCBASE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	ADCBASE<15:0>																0000	
B0D0	ADCTRGSNS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	—	LVL11	LVL10	LVL9	LVL8	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	0000	
B0D4	ADC0TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>			—	ADCDIV<6:0>					0300		
		15:0	—	—	—	—	—	—	SAMC<9:0>					ADCDIV<6:0>					0000	
B0D8	ADC1TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>			—	ADCDIV<6:0>					0300		
		15:0	—	—	—	—	—	—	SAMC<9:0>					ADCDIV<6:0>					0000	
B0DC	ADC2TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>			—	ADCDIV<6:0>					0300		
		15:0	—	—	—	—	—	—	SAMC<9:0>					ADCDIV<6:0>					0000	
B0E0	ADC3TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>			—	ADCDIV<6:0>					0300		
		15:0	—	—	—	—	—	—	SAMC<9:0>					ADCDIV<6:0>					0000	
B0E4	ADC4TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>			—	ADCDIV<6:0>					0300		
		15:0	—	—	—	—	—	—	SAMC<9:0>					ADCDIV<6:0>					0000	
B0F0	ADCEIEN1	31:16	EIEN31	EIEN30	EIEN29	EIEN28	EIEN27	EIEN26	EIEN25	EIEN24	EIEN23	EIEN22	EIEN21	EIEN20	EIEN19	EIEN18	EIEN17	EIEN16	0000	
		15:0	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0	0000	
B0F4	ADCEIEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	EIEN43	EIEN42	EIEN41	EIEN40	EIEN39	EIEN38	EIEN37	EIEN36	EIEN35	EIEN34	EIEN33	EIEN32	0000	
B0F8	ADCEISTAT1	31:16	EIRDY31	EIRDY30	EIRDY29	EIRDY28	EIRDY27	EIRDY26	EIRDY25	EIRDY24	EIRDY23	EIRDY22	EIRDY21	EIRDY20	EIRDY19	EIRDY18	EIRDY17	EIRDY16	0000	
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000	
B0FC	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	EIRDY43	EIRDY42	EIRDY41	EIRDY40	EIRDY39	EIRDY38	EIRDY37	EIRDY36	EIRDY35	EIRDY34	EIRDY33	EIRDY32	0000	
B100	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>					WKIEN7	—	—	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	—	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	—	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000	
B600	ADC0CFG ⁽¹⁾	31:16	ADCCFG<31:16>																0000	
		15:0	ADCCFG<15:0>																0000	
B604	ADC1CFG ⁽¹⁾	31:16	ADCCFG<31:16>																0000	
		15:0	ADCCFG<15:0>																0000	

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

PIC32MZ Graphics (DA) Family

REGISTER 30-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-22 **Unimplemented:** Read as '0'
- bit 21 **TXBO:** Transmitter in Error State Bus OFF ($TERRCNT \geq 256$)
- bit 20 **TXBP:** Transmitter in Error State Bus Passive ($TERRCNT \geq 128$)
- bit 19 **RXBP:** Receiver in Error State Bus Passive ($RERRCNT \geq 128$)
- bit 18 **TXWARN:** Transmitter in Error State Warning ($128 > TERRCNT \geq 96$)
- bit 17 **RXWARN:** Receiver in Error State Warning ($128 > RERRCNT \geq 96$)
- bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning
- bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter
- bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 30-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-0 **FIFOIP<31:0>:** FIFO Interrupt Pending bits
- 1 = One or more enabled FIFO interrupts are pending
- 0 = No FIFO interrupts are pending

PIC32MZ Graphics (DA) Family

REGISTER 30-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FLTEN23:** Filter 23 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN22:** Filter 22 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MZ Graphics (DA) Family

REGISTER 31-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits
Increment counter for frames successfully transmitted.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

36.1 Graphics LCD Controller Control Registers

TABLE 36-1: GRAPHICS LCD CONTROLLER REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0	All Resets
A000	GLCD MODE	31:16	LCDEN	CURSOR EN	—	VSYNC POL	HSYNC POL	DEPOL	—	DITHER	VSYNC CYC	PCLK POL	—	PGRAMP EN	FORCE BLANK	—	—	—	0000
		15:0	—	—	—	—	—	—	YUV OUTPUT	FORMAT CLK	RGBSEQ<2:0>			—	—	—	—	—	0000
A004	GLCD CLKCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0401
		15:0	—	—	LPREFETCH<5:0>						—	—	CLKDIV<5:0>						0000
A008	GLCD BGCOLOR	31:16	RED<7:0>								GREEN<7:0>								0000
		15:0	BLUE<7:0>								ALPHA<7:0>								0000
A00C	GLCDRES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A014	GLCD FPORCH	31:16	—	—	—	—	FPORCHX<10:0>												0000
		15:0	—	—	—	—	FPORCHY<10:0>												0000
A018	GLCD BLANKING	31:16	—	—	—	—	BLANKINGX<10:0>												0000
		15:0	—	—	—	—	BLANKINGY<10:0>												0000
A01C	GLCD BPORCH	31:16	—	—	—	—	BPORCHX<10:0>												0000
		15:0	—	—	—	—	BPORCHY<10:0>												0000
A020	GLCD CURSOR	31:16	—	—	—	—	CURSORX<10:0>												0000
		15:0	—	—	—	—	CURSORY<10:0>												0000
A030	GLCD LOMODE	31:16	LAYEREN	DISA BIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>								0000
		15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>				0000
A034	GLCD LOSTART	31:16	—	—	—	—	STARTX<10:0>												0000
		15:0	—	—	—	—	STARTY<10:0>												0000
A038	GLCD LOSIZE	31:16	—	—	—	—	SIZEX<10:0>												0000
		15:0	—	—	—	—	SIZEY<10:0>												0000
A03C	GLCD LOBADDR	31:16	BASEADDR<31:16>																0000
		15:0	BASEADDR<15:0>																0000
A040	GLCD LOSTRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRIDE<15:0>																0000
A044	GLCD LORES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A050	GLCD L1MODE	31:16	LAYEREN	DISA BIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>								0000
		15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: For the PIXELxy bits, x = 0-31 and y = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

PIC32MZ Graphics (DA) Family

REGISTER 36-1: GLCDMODE: GRAPHICS LCD CONTROLLER MODE REGISTER (CONTINUED)

- bit 19 **FORCEBLANK:** Force Output to Blank bit
 1 = Forces output to blank
 0 = No effect
- bit 18-10 **Unimplemented:** Read as '0'
- bit 9 **YUVOUTPUT:** YUV Output Enable bit
 1 = YUV is enabled
 0 = RGB is enabled
- bit 8 **FORMATCLK:** Formatting Clock Divide Enable bit
 1 = Formatting clock is not divided
 0 = Formatting clock is divided
- bit 7-5 **RGBSEQ<2:0>:** RGB Sequential Modes bit
 111 = BT.656
 110 = YUYV
 101 = Reserved
 100 = Reserved
 011 = Reserved
 010 = Reserved
 001 = Reserved
 000 = Parallel RGB (RGB888, RGB666, RGB332)
- bit 4-0 **Unimplemented:** Read as '0'

PIC32MZ Graphics (DA) Family

REGISTER 36-10: GLCDLxSTART: GRAPHICS LCD CONTROLLER LAYER 'x' START REGISTER (‘x’ = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	STARTX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STARTX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	STARTY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STARTY<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **STARTX<10:0>:** Layer Start X Dimension bits

These bits specify the pixel offset of the starting X dimension of the layer.

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **STARTY<10:0>:** Layer Start Y Dimension bits

These bits specify the pixel offset of the starting Y dimension of the layer.

REGISTER 36-11: GLCDLxSIZE: GRAPHICS LCD CONTROLLER LAYER 'x' SIZE REGISTER (‘x’ = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SIZEX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SIZEX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SIZEY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SIZEY<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **SIZEX<10:0>:** Layer Size X Dimension bits

These bits specify the pixel size of the layer in the X dimension.

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **SIZEY<10:0>:** Layer size Y Dimension bits

These bits specify the pixel size of the layer in the Y dimension.

PIC32MZ Graphics (DA) Family

REGISTER 38-24: DDRSCLSTART: DDL SELF CALIBRATION LOGIC START REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	U-0	W-0	U-0	R/W-0
	—	—	SCL PHCAL	SCL START	—	SCLLEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	SCLUB PASS ⁽¹⁾	SCLLB PASS ⁽¹⁾

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-30 **Unimplemented:** Write as '0'

bit 29 **SCLPHCAL:** Start Phase Self-calibration Logic bit
1 = Phase calibration is enabled
0 = Phase calibration is disabled

bit 28 **SCLSTART:** Start Self Calibration Logic bit
1 = Start self calibration
0 = Do not start self calibration

bit 27 **Unimplemented:** Write as '0'

bit 26 **SCLLEN:** Self Calibration Logic Enable bit
1 = Enable dynamic self calibration logic
0 = Disable dynamic self calibration logic

Note: Enabling dynamic self calibration may impact performance.

bit 25-2 **Unimplemented:** Write as '0'

bit 1 **SCLUBPASS:** Self Calibration Logic Upper Data Byte Status bit⁽¹⁾
1 = Self calibration logic for upper data byte passed
0 = Self calibration logic for upper data byte failed

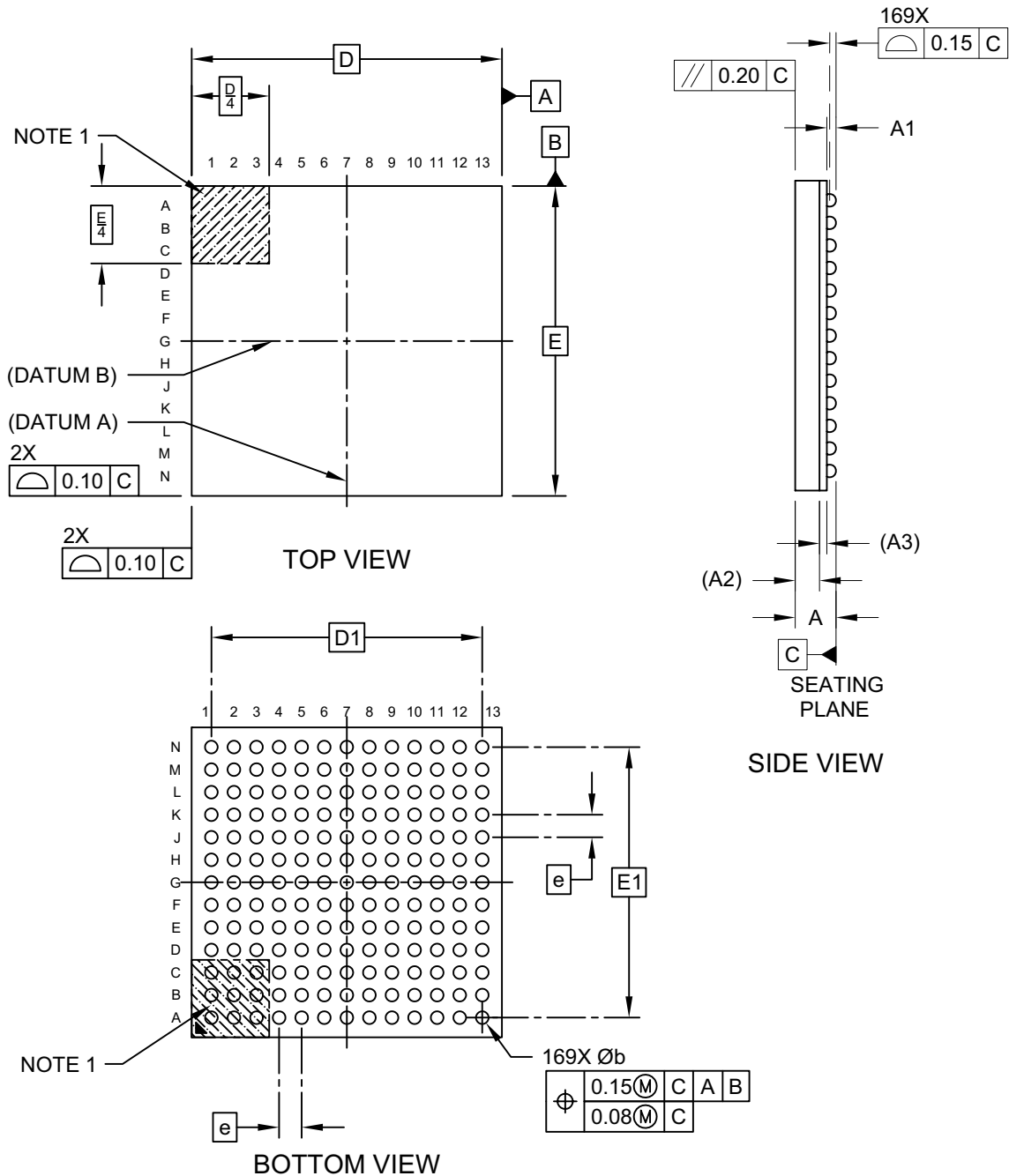
bit 0 **SCLLBPASS:** Self Calibration Logic Lower Data Byte Status bit⁽¹⁾
1 = Self calibration logic for lower data byte passed
0 = Self calibration logic for lower data byte failed

Note 1: This bit is set by hardware when the SCL process has passed and is complete.

PIC32MZ Graphics (DA) Family

169-Ball Low Profile Ball Grid Array (6JX) - 11x11 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-439A Sheet 1 of 2