Microchip Technology - PIC32MZ2025DAA169T-I/HF Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025daa169t-i-hf

TABLE 1-22: DDR2 SDRAM CONTROLLER PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
DDR2 SDRAM Controller						
DDRCK	DDR Internal to the Package	DDR Internal to the Package	K2	O	SSTL	Differential Clocks
$\overline{\text{DDRCK}}$			K1	O	SSTL	
DDRCKE			L2	O	SSTL	Clock Enable
$\overline{\text{DDRCS0}}$			N2	O	SSTL	Chip Select 0
$\overline{\text{DDRRAS}}$			M1	O	SSTL	Row Address Strobe
$\overline{\text{DDRCAS}}$			P2	O	SSTL	Column Address Strobe
$\overline{\text{DDRWE}}$			L1	O	SSTL	Write Enable Strobe
DDRLDM			G3	O	SSTL	Lower Data Byte Mask
DDRUDM			A3	O	SSTL	Upper Data Byte Mask
DDRODT			N1	O	SSTL	On-Die Termination
DDRLDQS			E1	I/O	SSTL	Lower Data Byte Qualifier Strobes (Differential)
$\overline{\text{DDRLDQS}}$			E2	I/O	SSTL	
DDRUDQS			B2	I/O	SSTL	Upper Data Byte Qualifier Strobes (Differential)
$\overline{\text{DDRUDQS}}$			A2	I/O	SSTL	
DDRBA0			M2	O	SSTL	Bank Address Select 0
DDRBA1			M3	O	SSTL	Bank Address Select 1
DDRBA2			U4	O	SSTL	Bank Address Select 2
DDRA0			R1	O	SSTL	DDR2 Address Bus
DDRA1			L3	O	SSTL	
DDRA2			N3	O	SSTL	
DDRA3			R2	O	SSTL	
DDRA4			P3	O	SSTL	
DDRA5			T1	O	SSTL	
DDRA6			U1	O	SSTL	
DDRA7			T2	O	SSTL	
DDRA8			U2	O	SSTL	
DDRA9			R3	O	SSTL	
DDRA10			P1	O	SSTL	
DDRA11			V2	O	SSTL	
DDRA12			T3	O	SSTL	
DDRA13			U3	O	SSTL	
DDRA14			T4	O	SSTL	
DDRA15			V3	O	SSTL	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select; SSTL = Stub Series Terminated Logic

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
084C	OFF195	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0850	OFF196	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0854	OFF197	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0858	OFF198	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
085C	OFF199	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0860	OFF200	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0864	OFF201	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0868	OFF202	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
086C	OFF203	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0874	OFF205	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0878	OFF206	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
087C	OFF207	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0880	OFF208	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0884	OFF209	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0888	OFF210	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08A4	OFF211	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0898	OFF214	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
089C	OFF215	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is only available on devices with a Crypto module.

REGISTER 11-24: USBExRPC: USB ENDPOINT 'x' REQUEST PACKET COUNT REGISTER (HOST MODE ONLY) ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RQPKTCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RQPKTCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RQPKTCNT<15:0>:** Request Packet Count bits
Sets the number of packets of size MAXP that are to be transferred in a block transfer. This register is only available in *Host mode* when AUTOREQ is set.

REGISTER 11-25: USBDPBFD: USB DOUBLE PACKET BUFFER DISABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-17 **EP7TXD:EP1TXD:** TX Endpoint 'x' Double Packet Buffer Disable bits
1 = TX double packet buffering is disabled for endpoint 'x'
0 = TX double packet buffering is enabled for endpoint 'x'

bit 16 **Unimplemented:** Read as '0'

bit 15-1 **EP7RXD:EP1RXD:** RX Endpoint 'x' Double Packet Buffer Disable bits
1 = RX double packet buffering is disabled for endpoint 'x'
0 = RX double packet buffering is enabled for endpoint 'x'

bit 0 **Unimplemented:** Read as '0'

REGISTER 15-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)	P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Input Capture Module Enable bit
- 1 = Module enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is ‘1’)**(1)**
- 0 = Timery is the counter source for capture
- 1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow occurred
- 0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: Refer to Table 15-1 for Timerx and Timery selections.

16.1 Output Compare Control Registers

TABLE 16-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
4020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
4200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
4220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
4400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
4420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
4600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
4620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
4800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
4820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

21.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

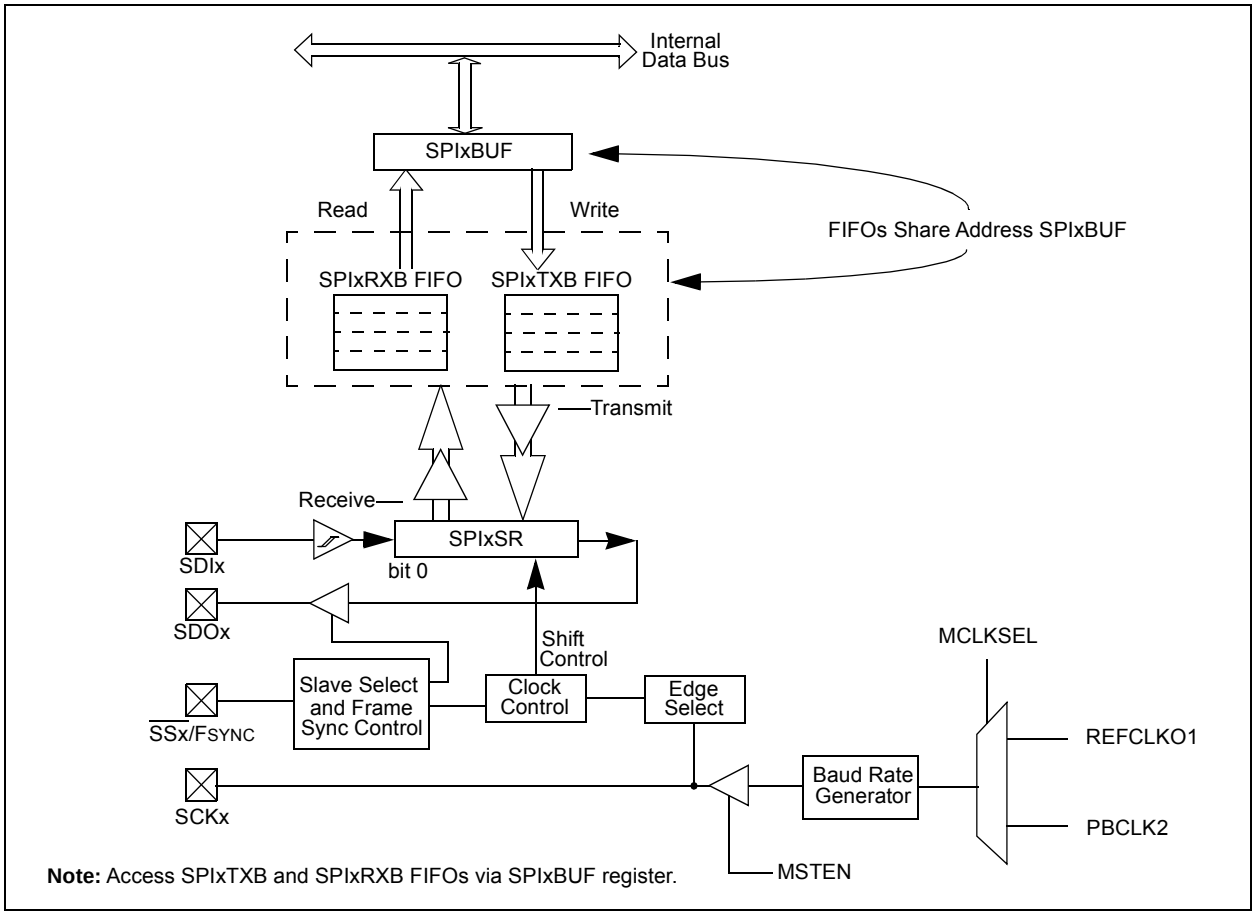
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 21-1: SPI/I^2S MODULE BLOCK DIAGRAM



22.1 SQI Control Registers

TABLE 22-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	SQI1 XCON1	31:16	—	—	SDRCMD	DDRDATA	DDR DUMMY	DDR MODE	DDR ADDR	DDRCMD	DUMMYBYTES<2:0>			ADDRBYTES<2:0>			READOPCODE<7:6>		0000
		15:0	READOPCODE<5:0>						TYPEDATA<1:0>		TYPEDUMMY<1:0>		TYPEMODE<1:0>		TYPEADDR<1:0>		TYPECMD<1:0>		0000
2004	SQI1 XCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>		MODECODE<7:0>								0000
2008	SQI1CFG	31:16	—	—	—	—	—	—	CSEN<1:0>		SQIEN	—	DATAEN<1:0>		CON BUFRST	RXBUFST	TXBUFST	RESET	0000
		15:0	—	—	—	BURSTEN	—	HOLD	WP	—	—	—	LSBF	CPOL	CPHA	MODE<2:0>			0000
200C	SQI1CON	31:16	—	—	—	—	—	—	—	SCHECK	DDRMODE	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>		0000
		15:0	TXRXCOUNT<15:0>																0000
2010	SQI1 CLKCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKDIV<10:8>			0000
		15:0	CLKDIV<7:0>								—	—	—	—	—	—	STABLE	EN	0000
2014	SQI1 CMDTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TXCMDTHR<5:0>						—	—	RXCMDTHR<5:0>						0000
2018	SQI1 INTTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TXINTTHR<5:0>						—	—	RXINTTHR<5:0>						0000
201C	SQI1 INTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEIE	PKT COMPIE	BD DONEIE	CON THRIE	CON EMPTYIE	CON FULLIE	RX THRIE	RX FULLIE	RX EMPTYIE	TX THRIE	TX FULLIE	TX EMPTYIE	0000
2020	SQI1 INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEIF	PKT COMPIF	BD DONEIF	CON THRIF	CON EMPTYIF	CON FULLIF	RX THRIF	RX FULLIF	RX EMPTYIF	TX THRIF	TX FULLIF	TX EMPTYIF	0000
2024	SQI1 TXDATA	31:16	TXDATA<31:16>																0000
		15:0	TXDATA<15:0>																0000
2028	SQI1 RXDATA	31:16	RXDATA<31:16>																0000
		15:0	RXDATA<15:0>																0000
202C	SQI1 STAT1	31:16	—	—	—	—	—	—	—	—	—	—	TXBUFFREE<5:0>						0000
		15:0	—	—	—	—	—	—	—	—	—	—	RXBUFCNT<5:0>						0000
2030	SQI1 STAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMDSTAT<1:0>		0000
		15:0	—	—	—	—	—	CONAVAIL<3:0>				SDID3	SDID2	SDID1	SDID0	—	RXUN	TXOV	00x0
2034	SQI1 BDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	START	POLLEN	DMAEN	0000
2038	SQI1BD CURADD	31:16	BDCURRADDR<31:16>																0000
		15:0	BDCURRADDR<15:0>																0000
2040	SQI1BD BASEADD	31:16	BDADDR<31:16>																0000
		15:0	BDADDR<15:0>																0000

REGISTER 22-14: SQI1BDCON: SQI BUFFER DESCRIPTOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	START	POLLEN	DMAEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **START:** Buffer Descriptor Processor Start bit
- 1 = Start the buffer descriptor processor
- 0 = Disable the buffer descriptor processor

bit 1 **POLLEN:** Buffer Descriptor Poll Enable bit
- 1 = BDP poll is enabled
- 0 = BDP poll is not enabled

bit 0 **DMAEN:** DMA Enable bit
- 1 = DMA is enabled
- 0 = DMA is disabled

REGISTER 22-15: SQI1BDCURADD: SQI BUFFER DESCRIPTOR CURRENT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BDCURRADDR<31:0>:** Current Buffer Descriptor Address bits
These bits contain the address of the current descriptor being processed by the Buffer Descriptor Processor.

REGISTER 22-23: SQI1TAPCON: SQI TAP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DDRCLKINDLY<5:0>					
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SDRDATINDLY<3:0>				DDRDATINDLY<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	SDRCLKINDLY<5:0>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUTDLY<3:0>				CLKOUTDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-24 **DDRCLKINDLY<5:0>:** SQI Clock Input Delay in DDR Mode bits
These bits are used to add fractional delays to SQI Clock Input while sampling the incoming data in DDR mode.
111111 = 64 taps added on clock input
111110 = 63 taps added on clock input
•
•
•
000001 = 2 taps added on clock input
000000 = 1 tap added on clock input

bit 23-20 **SDRDATINDLY<3:0>:** SQI Data Input Delay in SDR Mode bits
These bits are used to add fractional delays to SQI Data Output while writing the data to the Flash in SDR mode.
1111 = 16 taps added on data input
1110 = 15 taps added on data input
•
•
•
0001 = 2 taps added on data input
0000 = 1 tap added on data input

bit 19-16 **DDRDATINDLY<3:0>:** SQI Data Output Delay in DDR Mode bits
These bits are used to add fractional delays to SQI Data Output while writing the data to the Flash in DDR mode.
1111 = 16 taps added on data input
1110 = 15 taps added on data input
•
•
•
0001 = 2 taps added on data input
0000 = 1 tap added on data input

bit 15-14 **Unimplemented:** Read as '0'

27.3 Security Association Structure

Table 27-11 shows the Security Association Structure.

The Crypto Engine uses the Security Association to determine the settings for processing a Buffer Descriptor Processor. The Security Association contains:

- Which algorithm to use
- Whether to use engines in parallel (for both authentication and encryption/decryption)
- The size of the key
- Authentication key
- Encryption/decryption key
- Authentication Initialization Vector (IV)
- Encryption IV

FIGURE 27-11: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_CTRL	31:24	—	—	VERIFY	—	NO_RX	OR_EN	ICVONLY	IRFLAG
	23:16	LNC	LOADIV	FB	FLAGS	—	—	—	ALGO<6>
	15:8	ALGO<5:0>						ENCTYPE	KEYSIZE<1>
	7:0	KEYSIZE<0>	MULTITASK<2:0>			CRYPTOALGO<3:0>			
SA_AUTHKEY1	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY2	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY3	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY4	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY5	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY6	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY7	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY8	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_ENCKEY1	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY2	31:24	ENCKEY<31:24>							

TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B608	ADC2CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B60C	ADC3CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B610	ADC4CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B61C	ADC7CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B640	ADCSYSCFG1	31:16	AN<31:16>																0000
		15:0	AN<15:0>																0000
B644	ADCSYSCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	AN<43:32>												0000
BA00	ADCDATA0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA04	ADCDATA1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA08	ADCDATA2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA0C	ADCDATA3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA10	ADCDATA4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA14	ADCDATA5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA18	ADCDATA6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA1C	ADCDATA7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA20	ADCDATA8	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA24	ADCDATA9	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA28	ADCDATA10	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA2C	ADCDATA11	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA30	ADCDATA12	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 29-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF15:** AN15 Mode bit
1 = AN15 is using Differential mode
0 = AN15 is using Single-ended mode

bit 30 **SIGN:15** AN15 Signed Data Mode bit
1 = AN15 is using Signed Data mode
0 = AN15 is using Unsigned Data mode

bit 29 **DIFF14:** AN14 Mode bit
1 = AN14 is using Differential mode
0 = AN14 is using Single-ended mode

bit 28 **SIGN14:** AN14 Signed Data Mode bit
1 = AN14 is using Signed Data mode
0 = AN14 is using Unsigned Data mode

bit 27 **DIFF13:** AN13 Mode bit
1 = AN13 is using Differential mode
0 = AN13 is using Single-ended mode

bit 26 **SIGN13:** AN13 Signed Data Mode bit
1 = AN13 is using Signed Data mode
0 = AN13 is using Unsigned Data mode

bit 25 **DIFF12:** AN12 Mode bit
1 = AN12 is using Differential mode
0 = AN12 is using Single-ended mode

bit 24 **SIGN12:** AN12 Signed Data Mode bit
1 = AN12 is using Signed Data mode
0 = AN12 is using Unsigned Data mode

bit 23 **DIFF11:** AN11 Mode bit
1 = AN11 is using Differential mode
0 = AN11 is using Single-ended mode

bit 22 **SIGN11:** AN11 Signed Data Mode bit
1 = AN11 is using Signed Data mode
0 = AN11 is using Unsigned Data mode

bit 21 **DIFF10:** AN10 Mode bit
1 = AN10 is using Differential mode
0 = AN10 is using Single-ended mode

REGISTER 29-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 6 **SIGN19:** AN19 Signed Data Mode bit
1 = AN19 is using Signed Data mode
0 = AN19 is using Unsigned Data mode

bit 5 **DIFF18:** AN18 Mode bit
1 = AN18 is using Differential mode
0 = AN18 is using Single-ended mode

bit 4 **SIGN18:** AN18 Signed Data Mode bit
1 = AN18 is using Signed Data mode
0 = AN18 is using Unsigned Data mode

bit 3 **DIFF17:** AN17 Mode bit
1 = AN17 is using Differential mode
0 = AN17 is using Single-ended mode

bit 2 **SIGN17:** AN17 Signed Data Mode bit
1 = AN17 is using Signed Data mode
0 = AN17 is using Unsigned Data mode

bit 1 **DIFF16:** AN16 Mode bit
1 = AN16 is using Differential mode
0 = AN16 is using Single-ended mode

bit 0 **SIGN16:** AN16 Signed Data Mode bit
1 = AN16 is using Signed Data mode
0 = AN16 is using Unsigned Data mode

TABLE 30-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
0100	C1FLTCON4	31:16	FLTEN19	MSEL19<1:0>		FSEL19<4:0>					FLTEN18	MSEL18<1:0>		FSEL18<4:0>					0000
		15:0	FLTEN17	MSEL17<1:0>		FSEL17<4:0>					FLTEN16	MSEL16<1:0>		FSEL16<4:0>					0000
0110	C1FLTCON5	31:16	FLTEN23	MSEL23<1:0>		FSEL23<4:0>					FLTEN22	MSEL22<1:0>		FSEL22<4:0>					0000
		15:0	FLTEN21	MSEL21<1:0>		FSEL21<4:0>					FLTEN20	MSEL20<1:0>		FSEL20<4:0>					0000
0120	C1FLTCON6	31:16	FLTEN27	MSEL27<1:0>		FSEL27<4:0>					FLTEN26	MSEL26<1:0>		FSEL26<4:0>					0000
		15:0	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					FLTEN24	MSEL24<1:0>		FSEL24<4:0>					0000
0130	C1FLTCON7	31:16	FLTEN31	MSEL31<1:0>		FSEL31<4:0>					FLTEN30	MSEL30<1:0>		FSEL30<4:0>					0000
		15:0	FLTEN29	MSEL29<1:0>		FSEL29<4:0>					FLTEN28	MSEL28<1:0>		FSEL28<4:0>					0000
0140-0330	C1RXFn (n = 0-31)	31:16	SID<10:0>											--	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
0340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0																	0000
0350	C1FIFOCONn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
0360	C1FIFOINTn (n = 0)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
0370	C1FIFOUAn (n = 0)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
0380	C1FIFOCIn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000
0390-0B40	C1FIFOCONn C1FIFOINTn C1FIFOUAn C1FIFOCIn (n = 1-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
		31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
		31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 31-22: ETHALGNERR: ETHERNET CONTROLLER ALIGNMENT ERRORS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **ALGNERRCNT<15:0>:** Alignment Error Count bits

Increment count for frames with alignment errors. Note that an alignment error is a frame that has an FCS error and the frame length in bits is not an integral multiple of 8 bits (a.k.a., dribble nibble)

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

REGISTER 31-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 34-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit Select bits(1)
1111 = Selects analog input on HLVDIN
1110 = Selects trip point 14
1101 = Selects trip point 13
1100 = Selects trip point 12
1011 = Selects trip point 11
1010 = Selects trip point 10
1001 = Selects trip point 9
1000 = Selects trip point 8
0111 = Selects trip point 7
0110 = Selects trip point 6
0101 = Selects trip point 5
0100 = Selects trip point 4
0011 = Reserved; do not use
0010 = Reserved; do not use
0001 = Reserved; do not use
0000 = Reserved; do not use

Note 1: To avoid false HLVD events, all HLVD module setting changes should occur only when the module is disabled (ON = 0). See Table 44-6 in **44.0 "Electrical Characteristics"** for the actual trip points.

2: Once this bit is set to '1', it can only be cleared by disabling or enabling the HLVD module (or through the HLVDMD bit).

REGISTER 35-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 24 **EDG1STAT:** Edge1 Status bit
Indicates the status of Edge1 and can be written to control edge source
1 = Edge1 has occurred
0 = Edge1 has not occurred

bit 23 **EDG2MOD:** Edge2 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge2 programmed for a positive edge response
0 = Edge2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = Reserved
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = PBCLK3
1011 = IC5 Capture Event is selected
1010 = IC4 Capture Event is selected
1001 = IC3 Capture Event is selected
1000 = IC2 Capture Event is selected
0111 = IC1 Capture Event is selected
0110 = OC4 Capture Event is selected
0101 = OC3 Capture Event is selected
0100 = OC2 Capture Event is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ON Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** Stop-in-Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge1 must occur before Edge2 can occur
0 = No edge sequence is needed

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<2:0> bits must be set to '1110' to select the C2OUT pin.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 44-20) in **Section 44.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

REGISTER 39-10: SDHCINTEN: SDHC INTERRUPT FLAG ENABLE REGISTER (CONTINUED)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CARDIE:** Card Interrupt Flag Enable bit
1 = Card interrupt flag is enabled
0 = Card interrupt flag is masked

bit 7 **CARDRIE:** Card Removal Interrupt Flag Enable bit
1 = Card removal interrupt flag is enabled
0 = Card removal interrupt flag is masked

bit 6 **CARDIIE:** Card Insertion Interrupt Flag Enable bit
1 = Card insertion interrupt flag is enabled
0 = Card insertion interrupt flag is masked

bit 5 **BRRDYIE:** Buffer Read Ready Interrupt Flag Enable bit
1 = Buffer read ready interrupt flag is enabled
0 = Buffer read ready interrupt flag is masked

bit 4 **BWRDYIE:** Buffer Write Ready Interrupt Flag Enable bit
1 = Buffer write ready interrupt flag is enabled
0 = Buffer write ready interrupt flag is masked

bit 3 **DMAIE:** DMA Interrupt Flag Enable bit
1 = DMA interrupt flag is enabled
0 = DMA interrupt flag is masked

bit 2 **BGIE:** Block Gap Interrupt Flag Enable bit
1 = Block gap event interrupt flag is enabled
0 = Block gap event interrupt flag is masked

bit 1 **TXEIE:** Transfer Complete Interrupt Flag Enable bit
1 = Transfer complete interrupt flag is enabled
0 = Transfer complete interrupt flag is masked

bit 0 **CEIE:** Command Complete Interrupt Flag Enable bit
1 = Command complete interrupt flag is enabled
0 = Command complete interrupt flag is masked

TABLE 44-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDDIO	I/O Supply Voltage **(Note 1)**	2.2	—	3.6	V	—
DC11	VDDCORE	Core Supply Voltage **(Note 1)**	1.7	1.8	1.9	V	—
DC12	SVDDIO/ SVDDCORE	**VDDIO/VDDCORE Rise Rate** to Ensure Internal Power-on Reset Signal **(Note 2)**	0.000011	—	1.1	V/µs	300 ms to 3 µs @ 3.3v
DC13	VBAT	Battery Supply Voltage	2.2	—	3.6	V	—
DC14	VDDR1V8	DDR Memory Supply Voltage	1.7	1.8	1.9	V	—
DC15	DDRVREF	DDR Reference Voltage	0.49 x VDDR1V8	0.50 x VDDR1V8	0.51 x VDDR1V8	V	—

Note 1: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

2: Voltage on VDDIO must always be greater than or equal to VDDCORE during power-up.

TABLE 44-5: ELECTRICAL CHARACTERISTICS: RESETS

DC CHARACTERISTICS (Note 1)			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
RST10	VPORIO	VDDIO POR Voltage **(Note 2)**	VSS + 0.3	—	1.75	V	—
RST11	VPORCORE /VBATSW	VDDCORE POR Voltage **(Note 2)** VDDCORE to VBAT Switch Voltage **(Note 3)**	VSS + 0.3	—	1.7	V	—
RST12	VBORIO	BOR Event on VDDIO transition high-to-low **(Note 4)**	1.92	—	2.2	V	—
RST13	VPORBAT	POR Event on VBAT **(Note 4)**	1.35	—	2.2	V	—
RST14	VHVD1V8	High Voltage Detect on VDDR1V8 pins	2.16	—	2.24	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: This is the limit to which VDDIO/VDDCORE must be lowered to ensure Power-on Reset.

3: Device enters VBAT mode upon VDDCORE Power-on Reset.

4: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages.