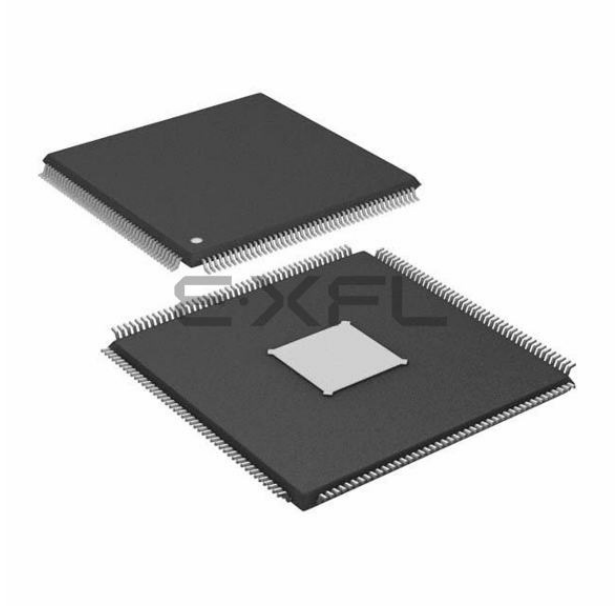
Microchip Technology - PIC32MZ2025DAA176-I/2J Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025daa176-i-2j

REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—					PLLIDIV<2:0>		
7:0	R/W-y	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	PLLICLK	—	—	—	—	PLLRANGE<2:0>		

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits

111 = Reserved
110 = Reserved
101 = PLL Divide by 32
100 = PLL Divide by 16
011 = PLL Divide by 8
010 = PLL Divide by 4
001 = PLL Divide by 2
000 = Reserved

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits

1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

The default setting is specified by the FPLLMULT<6:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

bit 15-11 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
11A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
11B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
11C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
11D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
11E0	DCH2CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
11F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1210	DCH2SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
1220	DCH2DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
1230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-7: USBIE0CSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-0	R-x	R-x	R-x	R-1	R-0
	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **MPRXEN:** Automatic Amalgamation Option bit
1 = Automatic amalgamation of bulk packets is done
0 = No automatic amalgamation

bit 30 **MPTXEN:** Automatic Splitting Option bit
1 = Automatic splitting of bulk packets is done
0 = No automatic splitting

bit 29 **BIGEND:** Byte Ordering Option bit
1 = Big Endian ordering
0 = Little Endian ordering

bit 28 **HBRXEN:** High-bandwidth RX ISO Option bit
1 = High-bandwidth RX ISO endpoint support is selected
0 = No High-bandwidth RX ISO support

bit 27 **HBTXEN:** High-bandwidth TX ISO Option bit
1 = High-bandwidth TX ISO endpoint support is selected
0 = No High-bandwidth TX ISO support

bit 26 **DYNFIFOS:** Dynamic FIFO Sizing Option bit
1 = Dynamic FIFO sizing is supported
0 = No Dynamic FIFO sizing

bit 25 **SOFTCONE:** Soft Connect/Disconnect Option bit
1 = Soft Connect/Disconnect is supported
0 = Soft Connect/Disconnect is not supported

bit 24 **UTMIDWID:** UTMI+ Data Width Option bit
Always '0', indicating 8-bit UTMI+ data width

bit 23-0 **Unimplemented:** Read as '0'

NOTES:

REGISTER 22-3: SQI1CFG: SQI CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CSEN<1:0>	
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	SQIEN	—	DATAEN<1:0>		CON BUFRST	RX BUFRST	TX BUFRST	RESET
15:8	U-0	r-0	r-0	R/W-0	r-0	R/W-0	R/W-0	U-0
	—	—	—	BURSTEN(1)	—	HOLD	WP	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LSBF	CPOL	CPHA	MODE<2:0>		

Legend:	HC = Hardware Cleared	r = Reserved	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-24 **CSEN<1:0>:** Chip Select Output Enable bits
- 11 = Chip Select 0 and Chip Select 1 are used
- 10 = Chip Select 1 is used (Chip Select 0 is not used)
- 01 = Chip Select 0 is used (Chip Select 1 is not used)
- 00 = Chip Select 0 and Chip Select 1 are not used

bit 23 **SQIEN:** SQI Enable bit
- 1 = SQI module is enabled
- 0 = SQI module is disabled

bit 22 **Unimplemented:** Read as '0'

bit 21-20 **DATAEN<1:0>:** Data Output Enable bits
- 11 = Reserved
- 10 = SQID3-SQID0 outputs are enabled
- 01 = SQID1 and SQID0 data outputs are enabled
- 00 = SQID0 data output is enabled

bit 19 **CONBUFRST:** Control Buffer Reset bit
- 1 = A reset pulse is generated clearing the control buffer
- 0 = A reset pulse is not generated

bit 18 **RXBUFRST:** Receive Buffer Reset bit
- 1 = A reset pulse is generated clearing the receive buffer
- 0 = A reset pulse is not generated

bit 17 **TXBUFRST:** Transmit Buffer Reset bit
- 1 = A reset pulse is generated clearing the transmit buffer
- 0 = A reset pulse is not generated

bit 16 **RESET:** Software Reset Select bit

This bit is automatically cleared by the SQI module. All of the internal state machines and buffer pointers are reset by this reset pulse.
- 1 = A reset pulse is generated
- 0 = A reset pulse is not generated

bit 15 **Unimplemented:** Read as '0'

bit 14-13 **Reserved:** Must be programmed as '0'

Note 1: This bit must be programmed as '1'.

REGISTER 22-23: SQI1TAPCON: SQI TAP CONTROL REGISTER (CONTINUED)

bit 13-8 **SDRCLKINDLY<5:0>:** SQI Clock Input Delay in SDR Mode bits

These bits are used to add fractional delays to SQI Clock Input while sampling the incoming data in DDR mode.

111111 = 64 taps added on clock input
111110 = 63 taps added on clock input

•
•
•

000001 = 2 taps added on clock input
000000 = 1 tap added on clock input

bit 7-4 **DATAOUTDLY<3:0>:** SQI Data Output Delay bits

These bits are used to add fractional delays to SQI Data Output while writing the data to the Flash in all modes of operation.

1111 = 16 taps added on data output
1110 = 15 taps added on data output

•
•
•

0001 = 2 taps added on data output
0000 = 1 tap added on data output

bit 3-0 **CLKOUTDLY<3:0>:** SQI Clock Output Delay bits

These bits are used to add fractional delays to SQI Clock Output while writing the data to the Flash in all modes of operation.

1111 = 16 taps added on clock output
1110 = 15 taps added on clock output

•
•
•

0001 = 2 taps added on clock output
0000 = 1 tap added on clock output

REGISTER 27-2: CECON: CRYPTO ENGINE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **SWAPOEN:** Swap Output Data Enable bit
- 1 = Output data is byte swapped when written by dedicated DMA
- 0 = Output data is not byte swapped when written by dedicated DMA

bit 6 **SWRST:** Software Reset bit
- 1 = Initiate a software reset of the Crypto Engine
- 0 = Normal operation

bit 5 **SWAPEN:** I/O Swap Enable bit
- 1 = TFDMA inputs and RFDMA outputs are swapped
- 0 = TFDMA inputs and RFDMA outputs are not swapped

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **BDPCHST:** Buffer Descriptor Processor (BDP) Fetch Enable bit

This bit should be enabled only after all DMA descriptor programming is completed.
- 1 = BDP descriptor fetch is enabled
- 0 = BDP descriptor fetch is disabled

bit 1 **BDPPLEN:** Buffer Descriptor Processor Poll Enable bit

This bit should be enabled only after all DMA descriptor programming is completed.
- 1 = Poll for descriptor until valid bit is set
- 0 = Do not poll

bit 0 **DMAEN:** DMA Enable bit
- 1 = Crypto Engine DMA is enabled
- 0 = Crypto Engine DMA is disabled

REGISTER 29-16: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6)

bit 24 **AFRDY:** Digital Filter '*x*' Data Ready Status bit
1 = Data is ready in the FLTRDATA<15:0> bits
0 = Data is not ready

Note: This bit is cleared by reading the FLTRDATA<15:0> bits or by disabling the Digital Filter module (by setting AFEN to '0').

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **CHNLID<4:0>:** Digital Filter Analog Input Selection bits
These bits specify the analog input to be used as the oversampling filter data source.
11111 = Reserved
.
.
.
01100 = Reserved
01011 = AN11
.
.
.
00001 = AN1
00000 = AN0

Note: Only the first 12 analog inputs, Class 1 (AN0-AN11) and Class 2 (AN5-AN11), can use a digital filter.

bit 15-0 **FLTRDATA<15:0>:** Digital Filter '*x*' Data Output Value bits
The filter output data is as per the fractional format set in the FRACT bit (ADCCON1<23>). The FRACT bit should not be changed while the filter is enabled. Changing the state of the FRACT bit after the operation of the filter ended will not update the value of the FLTRDATA<15:0> bits to reflect the new format.

REGISTER 29-25: ADCDATAx: ADC OUTPUT DATA REGISTER 'x' ('x' = 0 THROUGH 43)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

Note 1: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

2: Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

REGISTER 29-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WKUPCLKCNT<3:0>			
23:16	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WKIEN7	—	—	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0
15:8	R-0, HS, HC	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	WKRDY7	—	—	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ANEN7	—	—	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-24 **WKUPCLKCNT<3:0>:** Wake-up Clock Count bits

These bits represent the number of ADC clocks required to warm-up the ADC module before it can perform conversion. Although the clocks are specific to each ADC, the WKUPCLKCNT bit is common to all ADC modules.

1111 = 2^{15} = 32,768 clocks
.
.
.
0110 = 2^6 = 64 clocks
0101 = 2^5 = 32 clocks
0100 = 2^4 = 16 clocks
0011 = 2^4 = 16 clocks
0010 = 2^4 = 16 clocks
0001 = 2^4 = 16 clocks
0000 = 2^4 = 16 clocks

bit 23 **WKIEN7:** Shared ADC (ADC7) Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDY7 status bit is set
0 = Disable interrupt

bit 22-21 **Unimplemented:** Read as '0'

bit 20-16 **WKIEN4:WKIEN0:** ADC4-ADC0 Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDYx status bit is set
0 = Disable interrupt

bit 15 **WKRDY7:** Shared ADC (ADC7) Wake-up Status bit

1 = ADC7 Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN7 to '1'
0 = ADC7 Analog and Bias circuitry is not ready

Note: This bit is cleared by hardware when the ANEN7 bit is cleared

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **WKRDY4:WKRDY0:** ADC4-ADC0 Wake-up Status bit

1 = ADCx Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN*x* to '1'
0 = ADCx Analog and Bias circuitry is not ready

Note: These bits are cleared by hardware when the ANEN*x* bit is cleared

REGISTER 34-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit Select bits(1)
1111 = Selects analog input on HLVDIN
1110 = Selects trip point 14
1101 = Selects trip point 13
1100 = Selects trip point 12
1011 = Selects trip point 11
1010 = Selects trip point 10
1001 = Selects trip point 9
1000 = Selects trip point 8
0111 = Selects trip point 7
0110 = Selects trip point 6
0101 = Selects trip point 5
0100 = Selects trip point 4
0011 = Reserved; do not use
0010 = Reserved; do not use
0001 = Reserved; do not use
0000 = Reserved; do not use

Note 1: To avoid false HLVD events, all HLVD module setting changes should occur only when the module is disabled (ON = 0). See Table 44-6 in **44.0 "Electrical Characteristics"** for the actual trip points.

2: Once this bit is set to '1', it can only be cleared by disabling or enabling the HLVD module (or through the HLVDMD bit).

REGISTER 38-7: DDRMEMCFG1: DDR MEMORY CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RWADDRMSK<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RWADDRMSK<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **RWADDRMSK<12:0>:** Row Address Mask bits

These bits, which are used in conjunction with the RWADDR<4:0> bits (DDRMEMCFG0<4:0>), specify which bits of user address space are used to derive the row address for the DDR memory.

REGISTER 38-14: DDRDLYCFG1: DDR DELAY CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	SLFREF EXDLY<8>	NXTDAT AVDLY<4>	W2RCS DLY<4>	W2RDLY<4>	W2PCHRG-DLY<4>	PWRDNEXDLY<5:4>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWRDNEXDLY<3:0>				PWRDNMINDLY <3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFEXDLY<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFMINDLY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30 **SLFREFEXDLY:** Self Refresh Exit Delay bit 8

This bit specifies the minimum number of clocks required before normal operation after exiting Self Refresh mode.

bit 29 **NXTDATAVDLY:** Next Data Available Delay bit 4

These bits specify the minimum number of clock cycles required between a Write command and the write data transfer handshake signal "next data request". Also, see the NXTDATAVDLY<3:0> bits (DDRXFERCFG<7:4>).

bit 28 **W2RCSDLY:** Write-to-Read Chip Select Delay bit 4

This bit specify the minimum number of clocks required between a write command and a read command to different Chip Selects. Also, see W2RCSDLY<3:0> (DDRDLYCFG0<7:4>).

bit 27 **W2RDLY:** Write-to-Read Delay bit 4

This bit specifies the minimum number of clocks required between a write command and a read command to the same Chip Select. Also, see W2RDLY<3:0> (DDRDLYCFG0<3:0>).

bit 26 **W2PCHRGDLY:** Write to Precharge Delay bit 4

These bits specify the minimum number of clocks required from a Write command to a Precharge command to the same bank as the write. Also, see WPCHRGDLY<3:0> (DDRDLYCFG2<15:12>).

bit 25-20 **PWRDNEXDLY<5:0>:** Power Down Exit Delay bits

These bits specify the minimum number of clocks required before normal operation after exiting Power Down mode.

bit 19-16 **PWRDNMINDLY<3:0>:** Power Down Minimum Delay bits

These bits specify the minimum number of clocks to stay in Power Down mode after entering it.

bit 15-8 **SLFREFEXDLY<7:0>:** Self Refresh Exit Delay bits

These bits specify the minimum number of clocks required before normal operation after exiting Self Refresh mode.

bit 7-0 **SLFREFMINDLY<7:0>:** Self Refresh Minimum Delay bits

These bits specify the minimum number of clocks to stay in Self Refresh mode after entering it.

REGISTER 39-7: SDHCCON1: SDHC CONTROL REGISTER 1 (CONTINUED)

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **DMASEL<1:0>:** DMA Select bits

11 = Reserved
10 = 32-bit address ADMA2 is selected
01 = Reserved
00 = Reserved

bit 2 **HSEN:** High-Speed Enable bit

1 = High-Speed mode is enabled
0 = Normal Speed mode is enabled

bit 1 **DTXWIDTH:** Data Transfer Width bit

1 = 4-bit mode
0 = 1-bit mode

bit 0 **Unimplemented:** Read as '0'

REGISTER 41-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>				
15:8	R/P	R/P	r-1	r-1	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	IESO	FSOSCEN	DMTINV<2:0>			FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FDMTEN:** Deadman Timer enable bit
1 = Deadman Timer is enabled and *cannot* be disabled by software
0 = Deadman Timer is disabled and *can* be enabled by software

bit 30-26 **DMTCNT<4:0>:** Deadman Timer Count Select bits
11111 = Reserved
.
.
.
11000 = Reserved
10111 = 2^{31} (2147483648)
10110 = 2^{30} (1073741824)
10101 = 2^{29} (536870912)
10100 = 2^{28} (268435456)
.
.
.
00001 = 2^{9} (512)
00000 = 2^{8} (256)

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **WDTSPGM:** Watchdog Timer Stop During Flash Programming bit
1 = Watchdog Timer stops during Flash programming
0 = Watchdog Timer runs during Flash programming (for read/execute while programming Flash applications)

REGISTER 41-7: DEVCFG4/ADEVCFG4: DEVICE CONFIGURATION WORD 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	R/P	R/P	R/P	R/P
	—	—	—	SWDTPS<4:0>				
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as '1'

bit 29-24 **SWDTPS<4:0>:** Sleep Mode Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 31-29 **Reserved:** Write as '1'

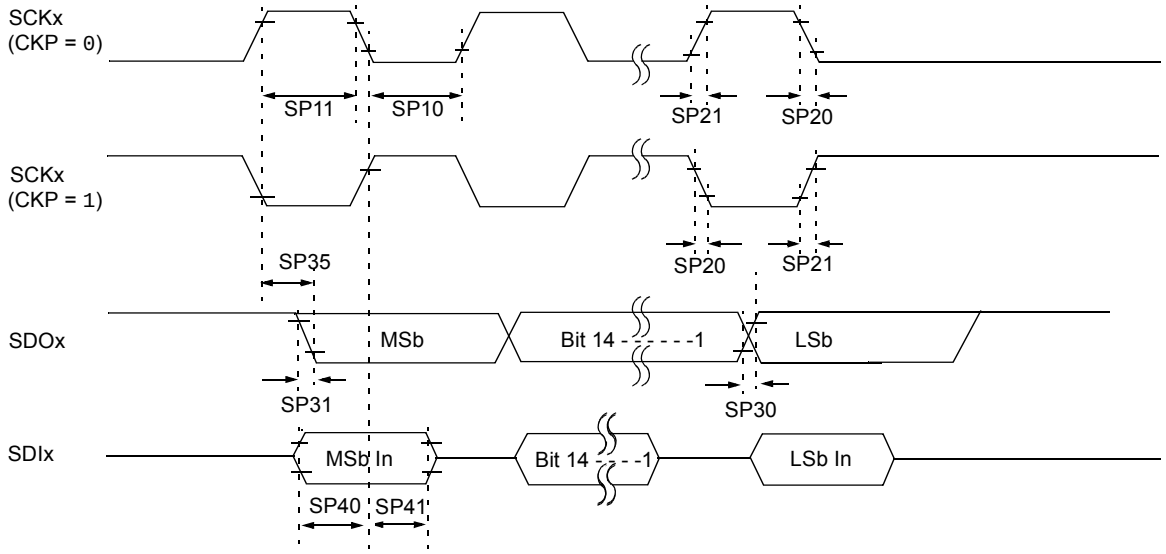
TABLE 44-19: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	—	—	10	µs	See **Note 1**
D313	DACREFH	CVREF Input Voltage Reference Range	AVSS	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24		CVRCON<CVRR> = 1
			—	—	DACREFH/32		CVRCON<CVRR> = 0
D316	DACACC	Absolute Accuracy(2)	—	—	1/4	LSB	DACREFH/24, CVRCON<CVRR> = 1
			—	—	1/2	LSB	DACREFH/32, CVRCON<CVRR> = 0

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

FIGURE 44-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

Revision D (March 2017)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-3.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology	Table 5, updated pin B4 to VDDCORE and B6 to VDDIO.
4.0 "Memory Organization"	Figure 4-1, updated KSEG3 from "cacheable" to "not cacheable"
6.0 "Resets"	Updated Figure 6-1.
8.0 "Oscillator Configuration"	Table 8-1, added SYSCLK to peripheral EBI.
26.0 "External Bus Interface (EBI)"	Figure 26-1, changed PBCLK8 to SYSCLK
29.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	Register 29-1, bit 12, updated notes and added table.
38.0 "DDR2 SDRAM Controller"	Table 38-1, swapped register names DRVSTRPFET and DRVSTRNFET. Table 38-1, added offset address 9140. Register 38-28, swapped register names and definitions DRVSTRPFET and DRVSTRNFET. Added Register 38-30,
40.0 "Power-Saving Features"	Register 40-1, updated "command" to "instruction." Updated **40.2.4 "VBAT Mode"**
41.0 "Special Features"	Register 41-5, updated "command" to "instruction.". Register 41-9, bit 7, updated notes and added table.
44.0 "Electrical Characteristics"	Updated **44.1 "DC Characteristics"** Updated Table 44-4 and Table 44-5. Table 44-18, Added parameter D306. Table 44-56, updated values for parameters DDR10, DDR19, DDR22, and DDR23.

Revision F (January 2018)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-5.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
1.0 "Device Overview"	The PIC32MZ DA Family Block Diagram was updated (see Figure 1-1). The 176-pin LQFP pin number for SDA3 in the I1C1 through I2C5 Pinout I/O Descriptions was updated (see Table 1-10). The 169-pin LFBGA pin numbers for EBIOE and EBIWE in the EBI Pinout I/O Descriptions were updated (see Table 1-13).
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	The following sections were added: • **2.7.1 "Crystal Oscillator Design Consideration"** • **2.9 "Considerations When Interfacing to Remotely Powered Circuits"**
4.0 "Memory Organization"	The PIC32MZ DA Family Memory Map was updated (see Figure 4-1).
10.0 "Direct Memory Access (DMA) Controller"	CRCTYP bit number references in the DMA CRC Control Register were updated (see Register 10-4, Register 10-5, and Register 10-6).
36.0 "Graphics LCD (GLCD) Controller"	The key features for the module were updated.
37.0 "2-D Graphics Processing Unit (GPU)"	The key features for the module were updated. The GPURESET bit reference in **Note 2** was updated.
38.0 "DDR2 SDRAM Controller"	The definition when SCLLBPASS is set to '0' was updated and the SCLPHCAL bit was added (see Register 38-24). The following registers were added: • **Register 38-31: "DDRPHYCLKDLY: DDR Clock Delta Delay Register"** • **Register 38-32: "DDRADLLBYP: DDR ANALOG DLL BYPASS Register"** • **Register 38-33: "DDRSCLCFG2: DDR SCL Configuration Register 2"** • **Register 38-34: "DDRPHYSCLADR: DDR PHY SCL Address Register"**
41.0 "Special Features"	The Device Configuration Word 0 registers, DEVCFG0/ADEVCFG0, was extensively updated (see Register 41-3). The bit value definitions for the FCKSM<1:0> bits and the POSCMOD<1:0> bits in the Device Configuration Word 1 registers, DEVCFG1/ADEVCFG1, were updated (see Register 41-4).
44.0 "Electrical Characteristics"	Parameter DO50 (COSCO) was removed from the Capacitive Loading Requirements on Output Pins (see Table 44-22).