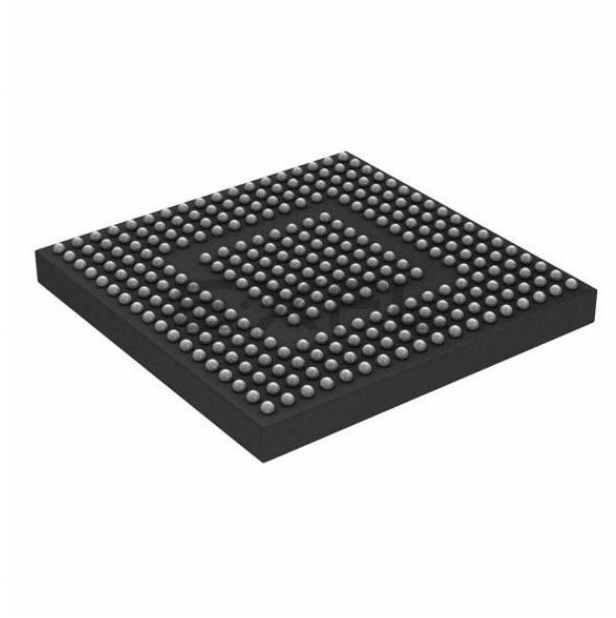
Microchip Technology - PIC32MZ2025DAA288T-I/4J Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	288-LFBGA
Supplier Device Package	288-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025daa288t-i-4j

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
PORTD						
RD0	H3	79	V5	I/O	ST	PORTD is a bidirectional I/O port
RD1	G1	73	M4	I/O	ST	
RD2	G2	74	R6	I/O	ST	
RD3	G3	75	T6	I/O	ST	
RD4	F1	70	K4	I/O	ST	
RD5	F2	71	L4	I/O	ST	
RD6	K11	121	V16	I/O	ST	
RD7	M10	120	T15	I/O	ST	
RD9	H1	76	U6	I/O	ST	
RD10	H2	77	V6	I/O	ST	
RD11	N10	119	U15	I/O	ST	
RD12	J1	80	U5	I/O	ST	
RD13	J2	81	N4	I/O	ST	
RD14	E9	158	J18	I/O	ST	
RD15	F11	157	J16	I/O	ST	
PORTE						
RE0	C4	40	B7	I/O	ST	PORTE is a bidirectional I/O port
RE1	A4	36	D8	I/O	ST	
RE2	N3	99	V10	I/O	ST	
RE3	M3	98	T9	I/O	ST	
RE4	B3	43	B6	I/O	ST	
RE5	F3	17	K3	I/O	ST	
RE6	F6	23	C11	I/O	ST	
RE7	C7	24	B11	I/O	ST	
RE8	E6	25	C10	I/O	ST	
RE9	D6	26	B10	I/O	ST	
PORTF						
RF0	L1	91	V7	I/O	ST	PORTF is a bidirectional I/O port
RF1	K3	90	U7	I/O	ST	
RF2	A3	41	A7	I/O	ST	
RF3	M1	93	U8	I/O	ST	
RF4	L3	44	U9	I/O	ST	
RF5	K2	89	T7	I/O	ST	
RF8	J3	82	P4	I/O	ST	
RF12	C6	27	A11	I/O	ST	
RF13	A6	28	A10	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-12: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Parallel Master Port						
PMA0	H13	142	N17	I/O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	J11	136	R18	I/O	TTL/ST	Parallel Master Port Address bit 1 Input (Buffered Slave modes) and Output (Master modes)
PMA2	C5	33	B9	O	—	Parallel Master Port Address (Demultiplexed Master modes)
PMA3	H11	135	R17	O	—	
PMA4	J12	139	N15	O	—	
PMA5	A11	174	B18	O	—	
PMA6	F3	69	K3	O	—	
PMA7	B12	173	E16	O	—	
PMA8	N2	96	V9	O	—	
PMA9	M2	95	T8	O	—	
PMA10	K3	90	U7	O	—	
PMA11	L1	91	V7	O	—	
PMA12	J1	80	U5	O	—	
PMA13	J2	81	N4	O	—	
PMA14	G2	74	R6	O	—	
PMA15	G3	75	T6	O	—	
PMCS1	G2	74	R6	O	—	Parallel Master Port Chip Select 1 Strobe
PMCS2	G3	75	T6	O	—	Parallel Master Port Chip Select 2 Strobe
PMD0	C4	40	B7	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	A4	36	D8	I/O	TTL/ST	
PMD2	N3	99	V10	I/O	TTL/ST	
PMD3	M3	98	T9	I/O	TTL/ST	
PMD4	B3	43	B6	I/O	TTL/ST	
PMD5	B7	17	A12	I/O	TTL/ST	
PMD6	F6	23	C11	I/O	TTL/ST	
PMD7	C7	24	B11	I/O	TTL/ST	
PMD8	K2	89	T7	I/O	TTL/ST	
PMD9	L3	97	U9	I/O	TTL/ST	
PMD10	A9	10	A15	I/O	TTL/ST	
PMD11	G10	143	N18	I/O	TTL/ST	
PMD12	A8	14	C13	I/O	TTL/ST	
PMD13	G12	144	M16	I/O	TTL/ST	
PMD14	L11	127	V17	I/O	TTL/ST	
PMD15	H1	76	U6	I/O	TTL/ST	
PMALL	H13	142	N17	O	—	Parallel Master Port Address Latch Enable Low Byte (Multiplexed Master modes)
PMALH	J11	136	R18	O	—	Parallel Master Port Address Latch Enable High Byte (Multiplexed Master modes)
PMRD	B8	16	A13	O	—	Parallel Master Port Read Strobe
PMWR	A7	15	B13	O	—	Parallel Master Port Write Strobe

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-23: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Power and Ground						
AVDD	D9	3, 4	F13, G13	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	C8, D8	5, 6	F12, G12	P	P	Ground reference for analog modules. This pin must be connected at all times.
VDDIO	B6, G9, H9, J9, K9, L6, L7, L9	19, 38, 86, 102, 117, 124, 155, 156, 165	C16, D15, D16, E15, F11, F15, G11, G15, H11, H12, H13, H15, J10, J15, K10, L11, L12, M12, M13, M15, N12, N13, R9, R10, R12, R13, R14	P	—	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
VDDCORE	B4, C9, L8, N1	18, 39, 84, 116	D7, D14, R11, V4	P	—	1.8V positive supply for peripheral logic. This pin must be connected at all times.
VSS	C2, F5, G5, G6, G7, G8, H7, H8, J7, J8, K7, K8	21, 22, 29, 37, 48, 49, 83, 87, 94, 103, 115, 122, 123, 153, 154	A5, B5, C7, D10, D11, D12, D13, F9, F10, G10, H10, J11, J12, J13, K11, K12, K13, K15, L10, L13, L15, M10, M11, N10, N11, R7, R8	P	—	Ground reference for logic, I/O pins, and USB. This pin must be connected at all times.
HLVDIN	B12	173	E16	P	—	Low-voltage detect pin.
VBAT	D10	166	F16	P	—	Positive supply for the battery backed section. It is recommended to connect this pin to VDDIO if VBAT mode is not used (i.e., not connected to the battery).
VDDR1V8	H5, H6, J5, J6, K5, K6 (**Note 2**)	57, 58, 59, 60, 61, 62, 63, 67, 68, 72, 78 (**Note 2**)	H6, H7, H8, J6, J7, J8, K6, K7, K8, L6, L7, L8 (**Note 2**)	P	—	Positive supply for the DDR2 SDRAM memory.

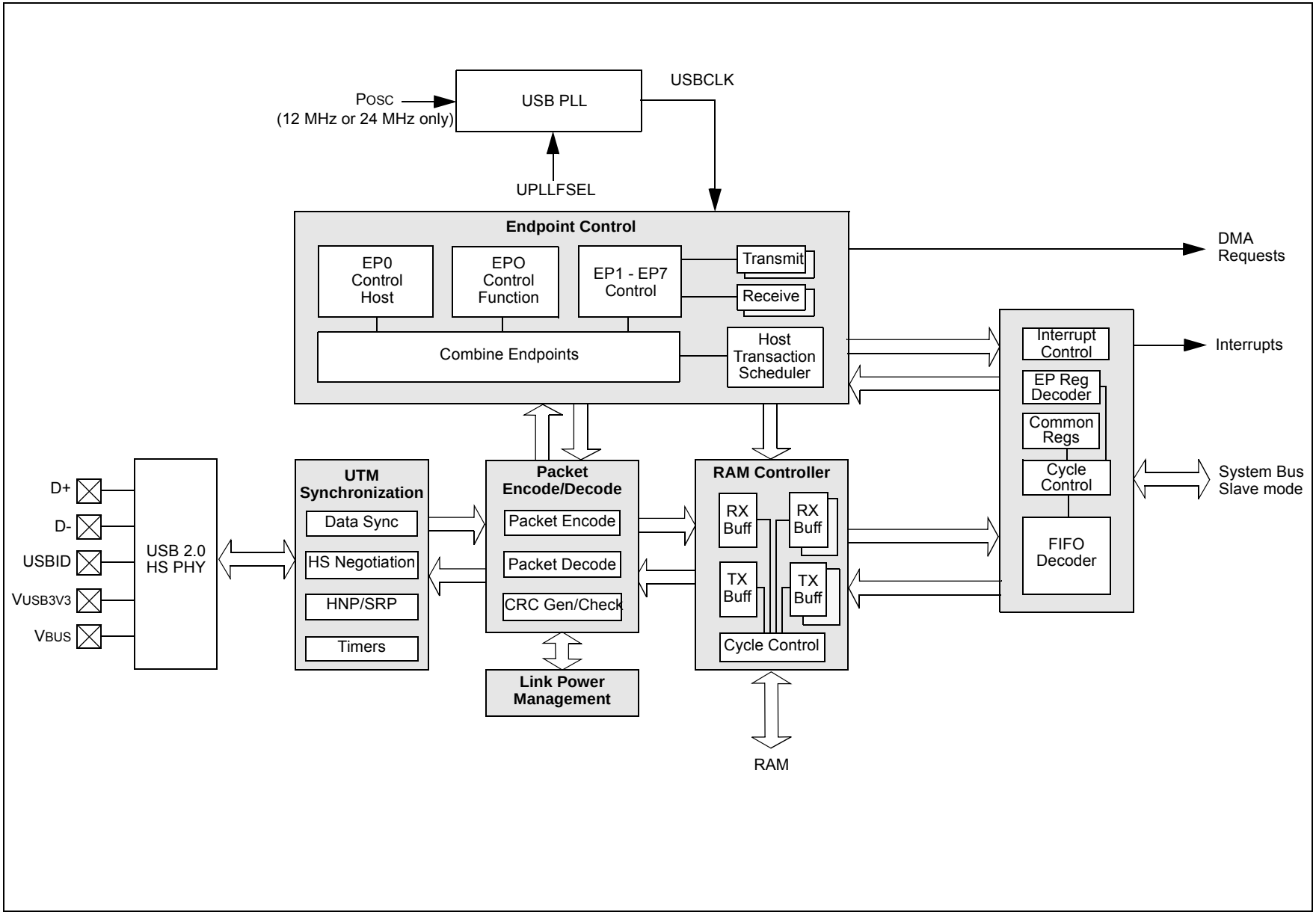
Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: The metal plane at the bottom of the device is internally tied to VSS1V8 and must be connected to 1.8V ground externally.

2: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.

3: This pin is a No Connect in devices without DDR.

FIGURE 11-1: PIC32MZ DA FAMILY USB INTERFACE DIAGRAM



REGISTER 11-16: USBINFO: USB INFORMATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	VPLEN<7:0>							
23:16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	WTCON<3:0>				WTID<3:0>			
15:8	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0
	DMACHANS<3:0>				RAMBITS<3:0>			
7:0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1
	RXENDPTS<3:0>				TXENDPTS<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **VPLEN<7:0>:** VBUS pulsing charge length bits
Sets the duration of the VBUS pulsing charge in units of 546.1 µs. (The default setting corresponds to 32.77 ms.)

bit 23-20 **WTCON<3:0>:** Connect/Disconnect filter control bits
Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667 µs.

bit 19-6 **WTID<3:0>:** ID delay valid control bits
Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.

bit 15-12 **DMACHANS<3:0>:** DMA Channels bits
These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ DA family, this number is 8.

bit 11-8 **RAMBITS<3:0>:** RAM address bus width bits
These read-only bits provide the width of the RAM address bus. For the PIC32MZ DA family, this number is 12.

bit 7-4 **RXENDPTS<3:0>:** Included RX Endpoints bits
This read-only register gives the number of RX endpoints in the design. For the PIC32MZ DA family, this number is 7.

bit 3-0 **TXENDPTS<3:0>:** Included TX Endpoints bits
These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ DA family, this number is 7.

REGISTER 12-1: [*pin name*]R: PERIPHERAL PIN SELECT INPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	[*pin name*]R<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **[*pin name*]R<3:0>:** Peripheral Pin Select Input bits
Where [*pin name*] refers to the pins that are used to configure peripheral input mapping. See Table for input pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

REGISTER 12-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RPnR<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **RPnR<3:0>:** Peripheral Pin Select Output bits
See Table for output pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

14.2 Timer2-Timer9 Control Registers

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0210	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0220	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0400	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0410	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0420	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0600	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0610	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0620	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0800	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0810	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0820	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF
0A00	T6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0A10	TMR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0A20	PR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0C00	T7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(1)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

REGISTER 22-26: SQI1XCON4: SQI XIP CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT2SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD3<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD2<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD1<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT2SCHECK:** Flash Initialization 2 Command Status Check bit
1 = Check the status after executing the INIT2 commands
0 = Do not check the status

bit 27-26 **INIT2COUNT<1:0>:** Flash Initialization 2 Command Count bits
11 = INIT2CMD1, INIT2CMD2, and INIT2CMD3 are sent
10 = INIT2CMD1 and INIT2CMD2 are sent, but INIT2CMD3 is still pending
01 = INIT2CMD1 is sent, but INIT2CMD2 and INIT2CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT2TYPE<1:0>:** Flash Initialization 2 Command Type bits
11 = Reserved
10 = INIT2 commands are sent in Quad Lane mode
01 = INIT2 commands are sent in Dual Lane mode
00 = INIT2 commands are sent in Single Lane mode

bit 24-16 **INIT2CMD3<7:0>:** Flash Initialization Command 3 bits
Third command of the Flash initialization.

bit 15-8 **INIT2CMD2<7:0>:** Flash Initialization Command 2 bits
Second command of the Flash initialization.

bit 7-0 **INIT2CMD1<7:0>:** Flash Initialization Command 1 bits
First command of the Flash initialization.

Note: Some Flash devices require write enable and sector unprotect commands before write/read operations and this register is useful in working with those Flash types (XIP mode only)

TABLE 24-1: UART1 THROUGH UART6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2600	U4MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2610	U4STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2620	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2630	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2640	U4BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2800	U5MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2810	U5STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2820	U5TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2830	U5RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2840	U5BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2A00	U6MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2A10	U6STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2A20	U6TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2A30	U6RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2A40	U6BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 24-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Module Enable bits(1)
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up enabled
- 0 = Wake-up disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
- 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
- 0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
- 1 = UxRX Idle state is '0'
- 0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
- 1 = High-Speed mode – 4x baud clock enabled
- 0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
- 11 = 9-bit data, no parity
- 10 = 8-bit data, odd parity
- 01 = 8-bit data, even parity
- 00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
- 1 = 2 Stop bits
- 0 = 1 Stop bit

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 25-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0>(1)		WAITM<3:0>(1)				WAITE<1:0>(1)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<15:0> by 1 every read/write cycle(2)
- 01 = Increment ADDR<15:0> by 1 every read/write cycle(2)
- 00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit
- 1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
- 0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
- 11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)
- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

REGISTER 26-4: EBIFTRPD: EXTERNAL BUS INTERFACE FLASH TIMING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	TRPD<11:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRPD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-0 **TRPD<11:0>:** Flash Timing bits
These bits define the number of clock cycles to hold the external Flash memory in reset.

Step 4: The user sets the ON bit to '1', which enables the ADC control clock. The following ADCx activation sequence is to be followed at all times:

Step 5: The user waits for the interrupt/polls the BGVRRDY bit (ADCCON2<31>) and the WKRDYx bit (ADCANCON<15,13:8>) = 1, which signals that the device analog environment (band gap and VREF) is ready.

Step 6: Set the DIGENx bit (ADCCON3<15,13:8>) to '1', which enables the digital circuitry to immediately begin processing incoming triggers to perform data conversions.

Standard non-interleaved dedicated Class_1 ADCx throughput rate formula is shown in Equation 29-1.

EQUATION 29-1: THROUGHPUT RATE

ADC Throughput Rate = 1/((Sample time + Conversion time)(TAD))
= 1 / ((SAMC+# bit resolution+1)(TAD))

Example:
SAMC = 3 TAD, 12-bit mode, TAD = 20 ns = 50 MHz:
Throughput rate:
= 1 / ((3+13)(20 ns))
= 1/(16 * 20 ns)
= 3.125 msps

TABLE 29-1: PIC32MZXXDAXX INTERLEAVED ADC THROUGHPUT RATES

#No.of Interleaved ADC Possible	ADC TAD(min) = 20ns (50Mhz max)			
	12-bit (max.) msps	10-bit (max.) msps	8-bit (max.) msps	6-bit (max.) msps
1	3.125 msps	3.571 msps	4.167 msps	5.0 msps
2	6.250 msps	7.143 msps	8.333 msps	10.00 msps
3	8.330 msps	10.00 msps	12.50 msps	12.50 msps
4	12.50 msps	12.50 msps	16.667 msps	16.667 msps

Note: Interleaved ADCs in this context means connecting the same analog source signal to multiple dedicated Class_1 ADCs (i.e., ADC0-ADC5), and using independent staggered trigger sources accordingly for each interleaved ADC.

Note 1: Prior to enabling the ADC module, the user application must copy the ADC calibration data (DEVADC0-DEVADC4, DEVADC7; see Register 41-8) from the Configuration memory into the ADC Configuration registers (ADC0CFG-ADC4CFG, ADC7CFG).

2: If V_{DDIO} is greater than 2.5V, set the AICPMPEN bit (ADCCON1<12>) and the IOANCPEN bit (CFGCON<7>) to '0'. If V_{DDIO} is less than 2.5V, set both bits to '1'.

REGISTER 31-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

36.0 GRAPHICS LCD (GLCD) CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 54. "Graphics LCD Controller"** (DS60001379), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Graphics LCD (GLCD) Controller is designed to directly interface with display panels with up to 24-bit color depth.

The GLCD Controller transfers display data from a memory device and formats it for a display device. The memory may be internal RAM or DDR2.

The parallel interface at the pins will operate at standard 3.3V output, requires 28 pins for 24-bit color, and is shared by general purpose I/O functions.

Key features of the GLCD Controller include:

- Supports a 50 MHz Pixel Clock (dependent on DDR2 bandwidth)
- Up to 800x480 (WVGA) with Overlay and smaller with three Overlay layers. High resolution is possible with smaller displays.
- Color depths: 8, 16**(1)**, 18, and 24 bits
- Up to three design timing layers, each including:
  - Configurable Alpha blending
  - Configurable Stride and Pitch
- Input formats: RGBA8888, ARGB8888, RGB888, RGB565, RGBA5551, YUYV, RGB332, LUT8, and Gray-scale
- Output formats: RGB888, RGB666, BT.656
- Dithering for 18-bit displays
- High-quality YUV conversion
- Global color palette look-up table (CLUT) supporting 256 colors
- Global gamma correction, brightness and contrast support
- Programmable cursors supporting 16 colors
- Programmable polarity on HSYNC, VSYNC, DE, and PCLK
- Integrated DMA to offload the CPU
- Programmable (level/edge) interrupt on HSYNC and VSYNC

Note 1: 16-bit color depth is supported through the GLCDMODE bit (CFGCON2<30>). When set, functions shared with GD0, GD1, GD2, GD8, GD9, GD16, GD17, GD18 are available for general purpose use.

A block diagram of the GLCD Controller interface is provided in Figure 36-1.

TABLE 44-7: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD} = I_{DDIO} + I_{DDCORE})

DC CHARACTERISTICS[1,2]			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial	
Parameter No.	**Typical[3]**	**Maximum**	**Units**	**Conditions**
I/O Operating Current (I_{DDIO}): Peripherals Enabled (PMDx=0, ON(PBxDIV<15>)=1)				
DC20	1.4	2.1	mA	8 MHz
DC21	3.5	4.1	mA	100 MHz[4]
DC22	5.6	6.5	mA	200 MHz
DC23	5.6	6.5	mA	200 MHz (L1 Cache and Prefetch modules disabled)[4]
I/O Operating Current (I_{DDCORE}): Peripherals Enabled (PMDx=0, ON(PBxDIV<15>)=1)				
DC20a	20	34	mA	8 MHz
DC21a	97	118	mA	100 MHz[4]
DC22a	152	180	mA	200 MHz
DC23a	128	153	mA	200 MHz (L1 Cache and Prefetch modules disabled)[4]
I/O Operating Current (I_{DDIO}): Peripherals Disabled (PMDx=1, ON(PBxDIV<15>)=0)				
DC24	1.4	2.1	mA	8 MHz
DC25	3.5	4.1	mA	100 MHz[4]
DC26	5.6	6.5	mA	200 MHz
DC27	5.6	6.5	mA	200 MHz (L1 Cache and Prefetch modules disabled)[4]
I/O Operating Current (I_{DDCORE}): Peripherals Disabled (PMDx=1, ON(PBxDIV<15>)=0)				
DC24a	19	33	mA	8 MHz
DC25a	90	109	mA	100 MHz[4]
DC26a	146	177	mA	200 MHz
DC27a	121	147	mA	200 MHz (L1 Cache and Prefetch modules disabled)[4]

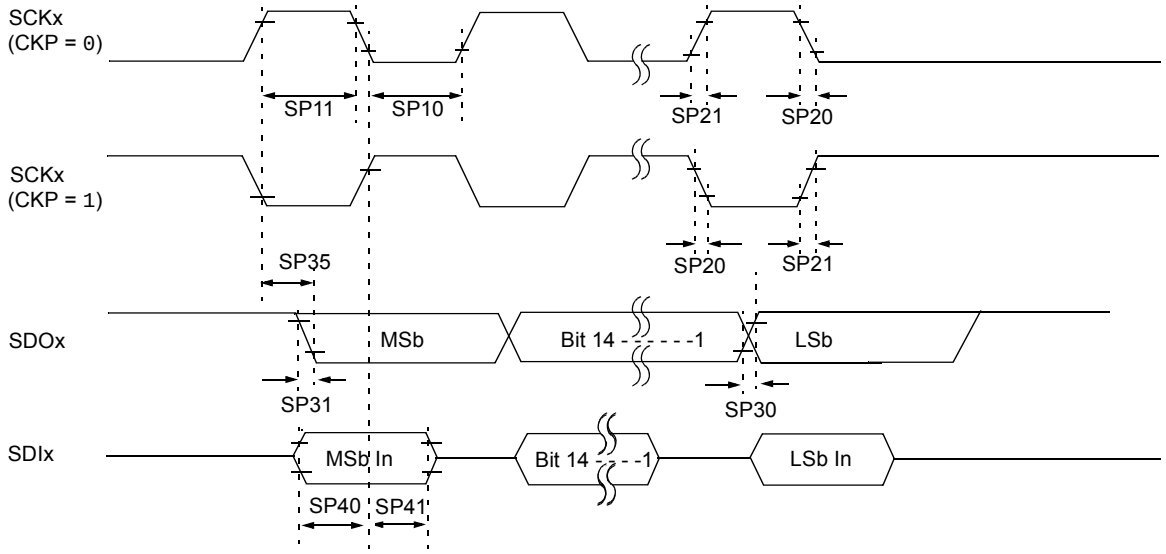
Note 1: A device's I_{DD} supply current is mainly a function of the operating voltage and frequency. Other factors, such as Peripheral Bus Clock (PBCLK) frequency, number of peripheral modules enabled, internal code execution pattern, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for I_{DD} measurements are as follows:
- V_{DDR1V8} = 1.8V
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
- CPU, Program Flash, and SRAM data memory are operational, Program Flash memory Wait states are equal to two
- No peripheral modules are operating (ON bit = 0)
- L1 Cache and Prefetch modules are enabled, unless otherwise specified in conditions.
- No peripheral modules are operating, (ON bit = 0)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DDIO}
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled
- I/O Analog Charge Pump is disabled (IOANCPEN bit (CFGCON<7>) = 0)
- ADC Input Charge Pump is disabled (AICPMPEN bit (ADCCON1<12> = 0)
- All Peripheral Bus Clocks, except PBCLK7, are disabled (ON bit (PBxDIV<15>) = 0, x = 2 through 6)

3: Data in "Typical" column is at 3.3V, +25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

FIGURE 44-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

FIGURE 44-26: TRANSMIT SIGNAL TIMING RELATIONSHIPS AT THE MII

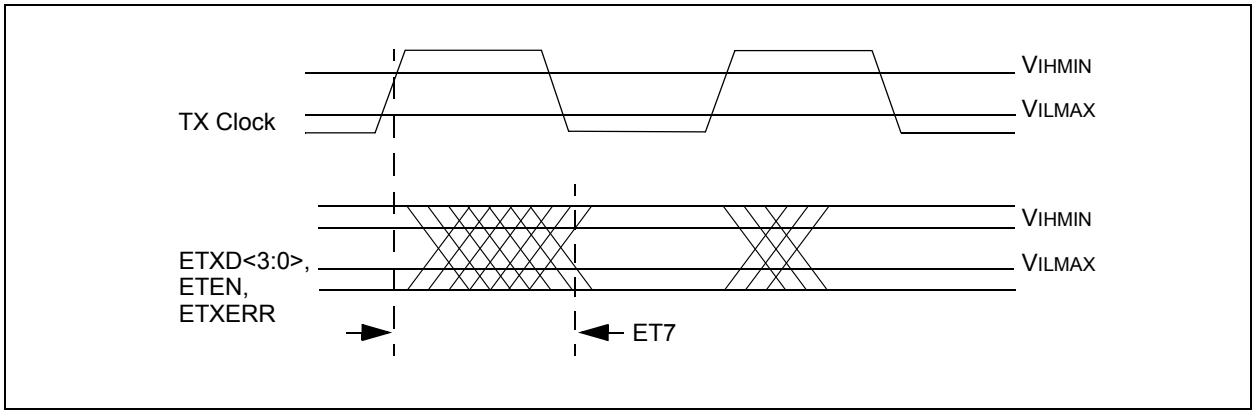
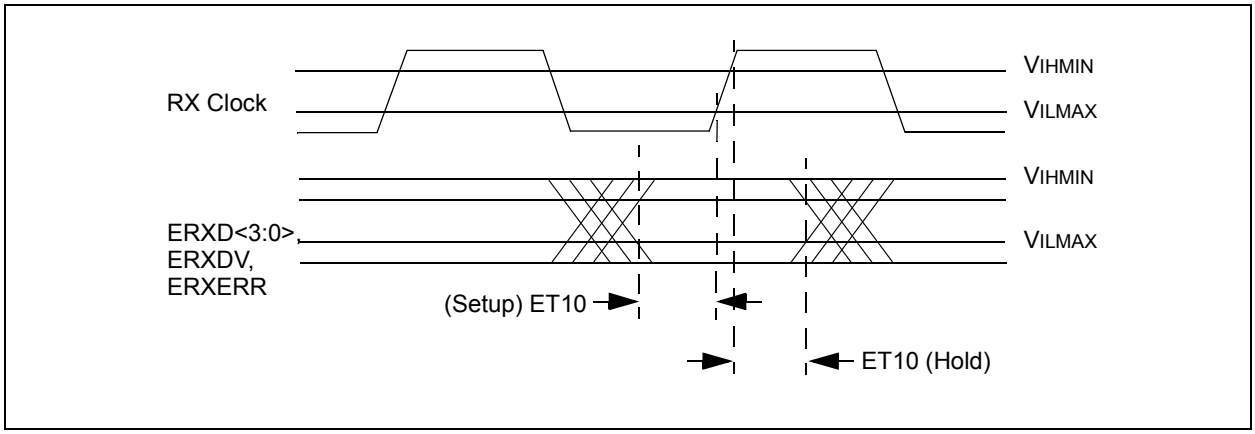


FIGURE 44-27: RECEIVE SIGNAL TIMING RELATIONSHIPS AT THE MII



Revision E (May 2017)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-4.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology	Updated the value of pin 168 from "CVREFOUT/AN5/RPB10/RB10" to "AN5/RPB10/RB10" (see Table 6).
25.0 "Parallel Master Port (PMP)"	The Virtual Address column heading was updated from BF80 to BF82 and the virtual addresses were updated from 70xx to E0xx (see Table 25-1).
36.0 "Graphics LCD (GLCD) Controller"	The resolutions in the key features list were updated.
39.0 "Secure Digital Host Controller (SDHC)"	The eMMC Standard: JESD84-A441 was added to the features list.
44.0 "Electrical Characteristics"	Table 44-7, Table 44-8, Table 44-9, Table 44-10, Table 44-11, Table 44-16, Table 44-18 updated various DC Characteristics parameters. Table 44-27, Table 44-28, Table 44-29 updated various AC Characteristics parameters.