Microchip Technology - PIC32MZ2025DAB169T-I/HF Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

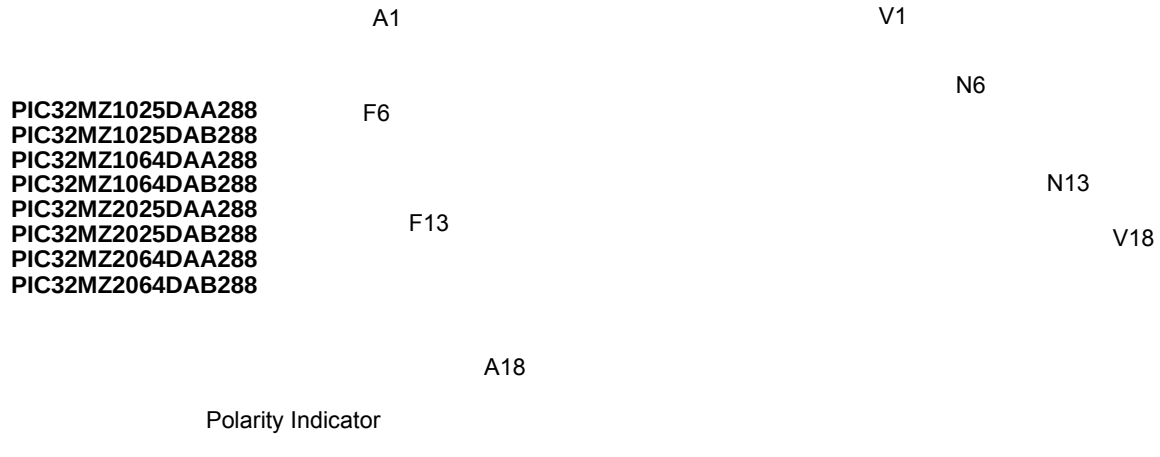
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025dab169t-i-hf

TABLE 7: PIN NAMES FOR 288-PIN DEVICES (CONTINUED)

288-PIN LFBGA (BOTTOM VIEW)



PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288

Ball/Pin Number	Full Pin Name
V3	DDRA15
V4	VDDCORE
V5	RTCC/RPD0/RD0
V6	SCK4/RD10
V7	GD6/EBIA11/RPF0/PMA11/RF0
V8	GD21/EBIA23/RH15
V9	GD3/EBIA8/RPG0/PMA8/RG0
V10	EBID2/PMD2/RE2
V11	ERXDV/ECRSDV/RH13
V12	ERXD3/RH9
V13	ETXD2/RH0
V14	ETXD0/RJ8
V15	ETXERR/RJ0
V16	ETXEN/RPD6/RD6
V17	GD1/EBID14/PMD14/RA4
V18	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.

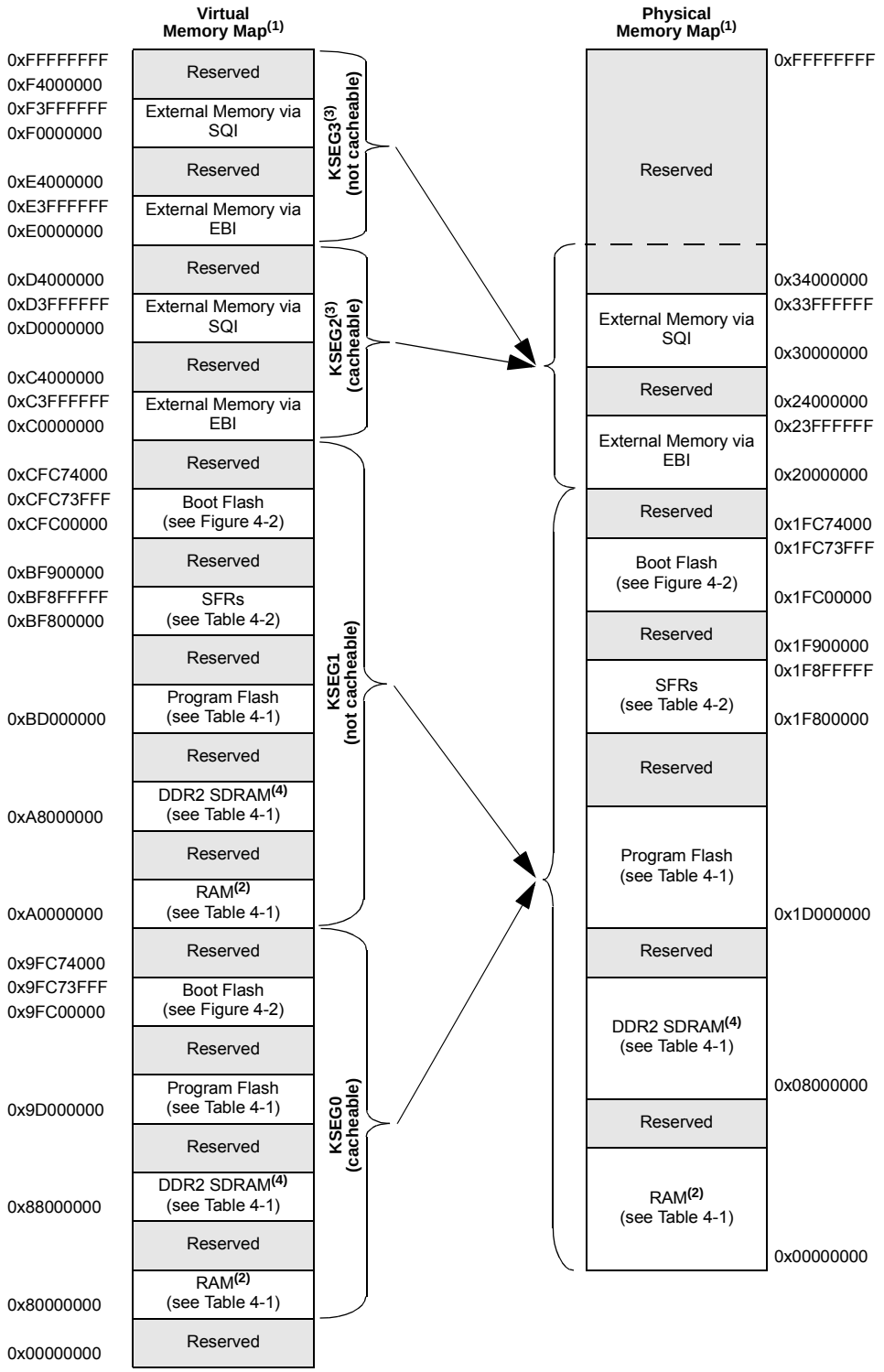
3: Shaded pins are 5V tolerant.

4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.

5: This pin is a No Connect when DDR is not connected in the system.

6: These pins are restricted to input functions only.

FIGURE 4-1: PIC32MZ DA FAMILY MEMORY MAP



Note 1: Memory areas are not shown to scale.

2: RAM memory is divided into two banks. Refer to Table 4-1 for additional information.

3: The MMU must be enabled and the TLB must be set up to access this segment.

4: This region is Reserved in devices without the DDR2 option.

REGISTER 4-7: SBTxELOG2: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 2 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	GROUP<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-3 **Unimplemented:** Read as '0'

bit 1-0 **GROUP<1:0>:** Requested Permissions Group bits
11 = Group 3
10 = Group 2
01 = Group 1
00 = Group 0

Note: Refer to Table 4-8 for the list of available targets and their descriptions.

REGISTER 4-8: SBTxECON: SYSTEM BUS TARGET 'x' ERROR CONTROL REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ERRP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ERRP:** Error Control bit
1 = Report protection group violation errors
0 = Do not report protection group violation errors

bit 23-0 **Unimplemented:** Read as '0'

Note: Refer to Table 4-8 for the list of available targets and their descriptions.

REGISTER 5-6: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PWPULOCK	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<23:16>							
15:8	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PWPULOCK:** Program Flash Memory Page Write-protect Unlock bit
1 = Register is not locked and can be modified
0 = Register is locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 30-24 **Unimplemented:** Read as '0'

bit 23-0 **PWP<23:0>:** Flash Program Write-protect (Page) Address bits
Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

15.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

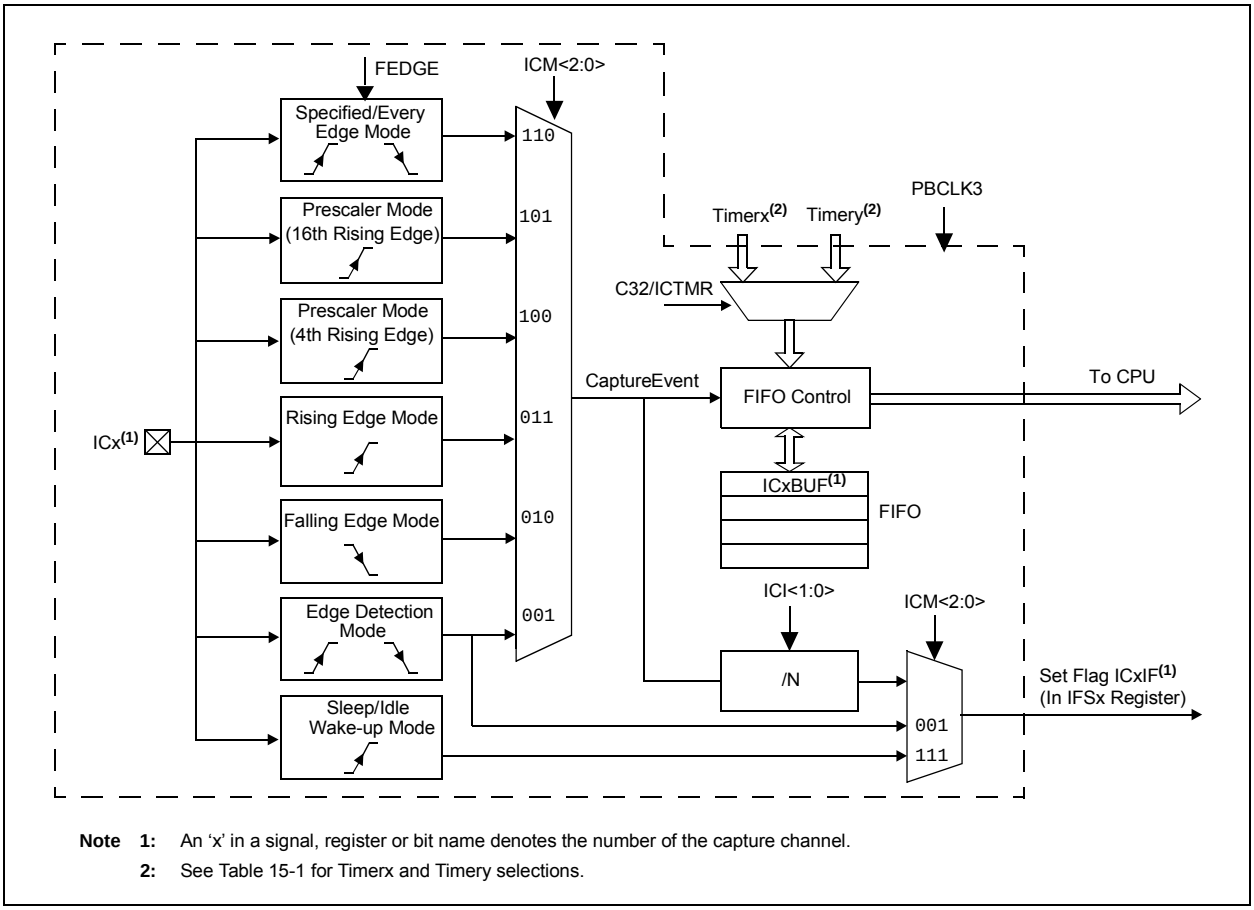
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 15-1 for Timerx and Timery selections.

REGISTER 20-4: RTCDATE: REAL-TIME CLOCK DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<3:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YEAR10<3:0>:** Binary-Coded Decimal Value of Years bits, 10 digits

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1 digit

bit 23-20 **MONTH10<3:0>:** Binary-Coded Decimal Value of Months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary-Coded Decimal Value of Days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary-Coded Decimal Value of Weekdays bits,1 digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 22-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal buffer space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

REGISTER 22-21: SQI1THR: SQI THRESHOLD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	THRES<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **THRES<3:0>:** SQI Control Threshold Value bits
The SQI control threshold interrupt is asserted when the amount of space indicated by THRES<6:0> is available in the SQI control buffer.

27.1 Crypto Engine Control Registers

TABLE 27-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>				START	ACTIVE	0000
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRLRLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 29-3: ADCCON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCSEL<1:0>		CONCLKDIV<5:0>					
23:16	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIGEN7	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R-0, HS, HC
	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP(1,2,3,4)	RQCNVRT
7:0	R/W-0	R/W, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GLSWTRG	GSWTRG	ADINSEL<5:0>					

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **ADCSEL<1:0>:** Analog-to-Digital Clock Source (TCLK) bits
11 = FRC
10 = REFCLK3
01 = System Clock (Tcy)
00 = PBCLK3

bit 29-24 **CONCLKDIV<5:0>:** Analog-to-Digital Control Clock (TQ) Divider bits
111111 = 64 * TCLK = TQ
•
•
•
000011 = 4 * TCLK = TQ
000010 = 3 * TCLK = TQ
000001 = 2 * TCLK = TQ
000000 = TCLK = TQ

bit 23 **DIGEN7:** Shared ADC (ADC7) Digital Enable bit
1 = ADC7 is digital enabled
0 = ADC7 is digital disabled

bit 22-21 **Unimplemented:** Read as '0'

bit 20 **DIGEN4:** ADC4 Digital Enable bit
1 = ADC4 is digital enabled
0 = ADC4 is digital disabled

bit 19 **DIGEN3:** ADC3 Digital Enable bit
1 = ADC3 is digital enabled
0 = ADC3 is digital disabled

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 30-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN19	MSEL19<1:0>		FSEL19<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN18	MSEL18<1:0>		FSEL18<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN17	MSEL17<1:0>		FSEL17<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN16	MSEL16<1:0>		FSEL16<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN19:** Filter 19 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL19<1:0>:** Filter 19 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL19<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN18:** Filter 18 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL18<1:0>:** Filter 18 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL18<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4 (CONTINUED)

bit 15 **FLTEN17:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL17<1:0>:** Filter 17 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL17<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN16:** Filter 16 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL16<1:0>:** Filter 16 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL16<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN27	MSEL27<1:0>		FSEL27<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN26	MSEL26<1:0>		FSEL26<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN25	MSEL25<1:0>		FSEL25<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN24	MSEL24<1:0>		FSEL24<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN27:** Filter 27 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL27<1:0>:** Filter 27 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL27<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN26:** Filter 26 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL26<1:0>:** Filter 26 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL26<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 31-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	CWINDOW<5:0>					
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	—	RETX<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RETX<3:0>:** Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is '0xF'.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 38-1: DDR SDRAM CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
80A8	DDR CMD110	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80AC	DDR CMD111	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80B0	DDR CMD112	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80B4	DDR CMD113	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80B8	DDR CMD114	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD<27:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80BC	DDR CMD115	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80C0	DDR CMD20	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80C4	DDR CMD21	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80C8	DDR CMD22	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80CC	DDR CMD23	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80D0	DDR CMD24	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80D4	DDR CMD25	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80D8	DDR CMD26	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80DC	DDR CMD27	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80E0	DDR CMD28	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80E4	DDR CMD29	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000

REGISTER 39-6: SDHCSTAT1: SDHC STATUS REGISTER 1 (CONTINUED)

bit 10 **BWEN:** Buffer Write Enable bit
1 = Buffer write is enabled
0 = Buffer write is disabled

bit 9 **RDACTIVE:** Read Transfer Active bit
1 = Data is being transferred
0 = No valid data

bit 8 **WRACTIVE:** Write Transfer Active bit
1 = Data is being transferred
0 = No valid data

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **DLACTIVE:** DAT Line Active bit
1 = DAT line is active
0 = DAT line is inactive

bit 1 **CINHDAT:** Command Inhibit (DAT) bit
1 = A command that uses the DAT line cannot be issued
0 = A command that uses the DAT line can be issued

bit 0 **CINHCMD:** Command Inhibit (CMD) bit
1 = A command cannot be issued
0 = A command can only be issued using the CMD line

Note: This register is used to recover from errors and for debugging.

REGISTER 39-15: SDHCFE: SDHC FORCE EVENT REGISTER (CONTINUED)

bit 7 **FECNIACE:** Force Event for Command Not Issued by Auto CMD12 Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **FEACIDXE:** Force Event for Auto CMD12 Index Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 3 **FEACEBE:** Force Event for Auto CMD12 End Bit Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 2 **FEACCRCE:** Force Event for Auto CMD12 CRC Error bit

bit 1 **FEACTOE:** Force Event for Auto CMD12 Time-out Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 0 **FEACNEE:** Force Event for Auto CMD12 Not Executed Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

REGISTER 41-14: CFGMPLL: MEMORY PLL CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	MPLLRDY	MPLLDIS	MPLLODIV2<2:0>			MPLLODIV1<2:0>		
23:16	R-0	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
	MPLL VREGRDY	MPLL VREGDIS	—	—	—	—	—	—
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	MPLLMULT<7:0>							
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	INTVREFCON<1:0>		MPLLIDIV<5:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **MPLLRDY:** Memory PLL Status bit
1 = MPLL clock is stable and is ready for use
0 = MPLL clock is not ready. Initializing DDR2 SDRAM when the clock is not ready will result in undefined behavior.

bit 30 **MPLLDIS:** MPLL Disable bit
1 = MPLL is disabled
0 = MPLL is enabled

Note: Clear this bit only after the MPLLVREGRDY bit is set to '1'.

bit 29-27 **MPLLODIV2<2:0>:** MPLL Output Divider 2 bits
111 = MPLL second stage output is divided by 7
110 = MPLL second stage output is divided by 6
101 = MPLL second stage output is divided by 5
100 = MPLL second stage output is divided by 4
011 = MPLL second stage output is divided by 3
010 = MPLL second stage output is divided by 2
001 = MPLL second stage output is divided by 1
000 = Reserved

Note: The Value in this field should be less than MPLLODIV1. Unless it is necessary, setting these bits to '001' (MPLL second stage output is divided by 1) will produce less clock jitter.

bit 26-24 **MPLLODIV1<2:0>:** MPLL Output Divider 1 bits
See bits 29-27 for available selections.

bit 23 **MPLLVREGRDY:** MPLL Voltage Regulator Ready bit
1 = MPLL voltage regulator is ready for use
0 = MPLL voltage regulator is not ready or is disabled

bit 22 **MPLLVREGDIS:** MPLL Voltage regulator Disable bit
1 = MPLL voltage regulator is disabled
0 = MPLL voltage regulator is enabled

bit 21-16 **Unimplemented:** Read as '0'

44.1 DC Characteristics

TABLE 44-1: OPERATING MIPS VS. VOLTAGE

Characteristic	V_{DDIO} Range (in Volts) (Note 1)	V_{DDCORE} Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comments
				PIC32MZ DA Devices	
DC5	2.2V-3.6V	1.7V-1.9V	-40°C to +85°C	200 MHz	—

Note 1: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

TABLE 44-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DDIO} \times (I_{DD} - S\ I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = S\ (\{V_{DDIO} - V_{OH}\} \times I_{OH}) + S\ (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 44-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 169-pin LFBGA (11x11x1.4 mm)	θ_{JA}	25	—	°C/W	**1**
Package Thermal Resistance, 169-pin LFBGA (11x11x1.56 mm)	θ_{JA}	24	—	°C/W	**1,2**
Package Thermal Resistance, 176-pin LQFP (20x20x1.45 mm)	θ_{JA}	17	—	°C/W	**1**
Package Thermal Resistance, 176-pin LQFP (20x20x1.45 mm)	θ_{JA}	19	—	°C/W	**1,2**
Package Thermal Resistance, 288-pin LFBGA (15x15x1.4 mm)	θ_{JA}	22	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-$_{JA}$ (θ_{JA}) numbers are achieved by package simulations.

2: Devices with internal DDR2 SDRAM.

TABLE 44-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDDIO	I/O Supply Voltage **(Note 1)**	2.2	—	3.6	V	—
DC11	VDDCORE	Core Supply Voltage **(Note 1)**	1.7	1.8	1.9	V	—
DC12	SVDDIO/ SVDDCORE	**VDDIO/VDDCORE Rise Rate** to Ensure Internal Power-on Reset Signal **(Note 2)**	0.000011	—	1.1	V/µs	300 ms to 3 µs @ 3.3v
DC13	VBAT	Battery Supply Voltage	2.2	—	3.6	V	—
DC14	VDDR1V8	DDR Memory Supply Voltage	1.7	1.8	1.9	V	—
DC15	DDRVREF	DDR Reference Voltage	0.49 x VDDR1V8	0.50 x VDDR1V8	0.51 x VDDR1V8	V	—

Note 1: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

2: Voltage on VDDIO must always be greater than or equal to VDDCORE during power-up.

TABLE 44-5: ELECTRICAL CHARACTERISTICS: RESETS

DC CHARACTERISTICS (Note 1)			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
RST10	VPORIO	VDDIO POR Voltage **(Note 2)**	VSS + 0.3	—	1.75	V	—
RST11	VPORCORE /VBATSW	VDDCORE POR Voltage **(Note 2)** VDDCORE to VBAT Switch Voltage **(Note 3)**	VSS + 0.3	—	1.7	V	—
RST12	VBORIO	BOR Event on VDDIO transition high-to-low **(Note 4)**	1.92	—	2.2	V	—
RST13	VPORBAT	POR Event on VBAT **(Note 4)**	1.35	—	2.2	V	—
RST14	VHVD1V8	High Voltage Detect on VDDR1V8 pins	2.16	—	2.24	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: This is the limit to which VDDIO/VDDCORE must be lowered to ensure Power-on Reset.

3: Device enters VBAT mode upon VDDCORE Power-on Reset.

4: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages.

TABLE 44-24: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OS51	FSYS	System Frequency	DC	—	200	MHz	USB module disabled
			30	—	200	MHz	USB module enabled
OS55a	FPB	Peripheral Bus Frequency	DC	—	100	MHz	For PBCLKx, 'x' < 7
OS55b			DC	—	200	MHz	For PBCLK7
OS56	FREF	Reference Clock Frequency	—	—	50	MHz	For REFCLK1, REFCLK3, REFCLK4, REFCLKO1, REFCLK3, and REFCLK4 pins

TABLE 44-25: SPLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OS50	FIN	PLL Input Frequency Range	5	—	64	MHz	ECPLL, HSPLL, FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	100	µs	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period
OS54	FVCO	PLL VCO Frequency Range	350	—	700	MHz	—
OS54a	FPLL	PLL Output Frequency Range	10	—	200	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter \quad \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter \quad \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} \quad \frac{D_{CLK}}{1.41}$$