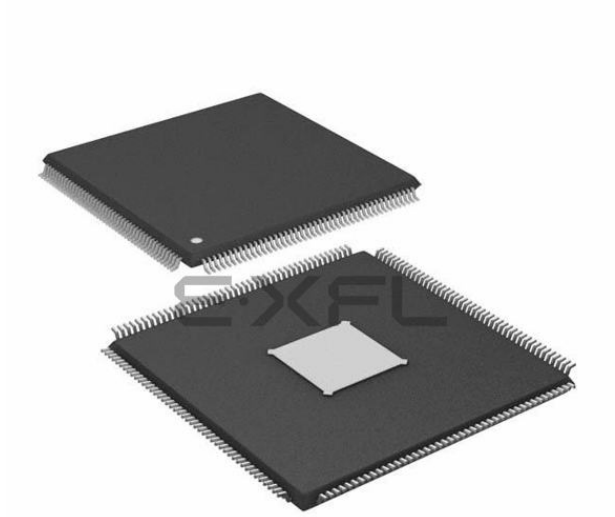

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 45x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP Exposed Pad |
| Supplier Device Package | 176-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025dab176-i-2j |

**TABLE 6: PIN NAMES FOR 176-PIN DEVICES**

**176-PIN LQFP (TOP VIEW)**

**PIC32MZ1025DAA176**
**PIC32MZ1025DAB176**
**PIC32MZ1064DAA176**
**PIC32MZ1064DAB176**
**PIC32MZ2025DAA176**
**PIC32MZ2025DAB176**
**PIC32MZ2064DAA176**
**PIC32MZ2064DAB176**
**PIC32MZ1025DAG176**
**PIC32MZ1025DAH176**
**PIC32MZ1064DAG176**
**PIC32MZ1064DAH176**
**PIC32MZ2025DAG176**
**PIC32MZ2025DAH176**
**PIC32MZ2064DAG176**
**PIC32MZ2064DAH176**

176

1

| Pin Number | Full Pin Name | Pin Number | Full Pin Name |
|---|---|---|---|
| 1 | VREF-/CVREF-/AN27/RA9 | 37 | VSS |
| 2 | VREF+/CVREF+/AN28/RA10 | 38 | VDDIO |
| 3 | AVDD | 39 | VDDCORE |
| 4 | AVDD | 40 | EBID0/PMD0/RE0 |
| 5 | AVSS | 41 | RPF2/SDA3/RF2 |
| 6 | AVSS | 42 | INT0/RH14 |
| 7 | AN3/C2INA/RPB15/OCFB/RB15 | 43 | EBID4/AN18/PMD4/RE4 |
| 8 | AN8/RPB3/RB3 | 44 | No Connect |
| 9 | AN48/CTPLS/RB13 | 45 | VBUS |
| 10 | EBID10/AN4/RPB8/PMD10/RB8 | 46 | VUSB3V3 |
| 11 | PGEC1/AN9/RPB1/CTED1/RB1 | 47 | VUSB3V3 |
| 12 | AN49/RB11 | 48 | VSS |
| 13 | PGEC2/RPB6/RB6 | 49 | VSS |
| 14 | EBID12/AN10/RPC2/PMD12/RC2 | 50 | D- |
| 15 | EBIWE/AN34/RPC3/PMWR/RC3 | 51 | D+ |
| 16 | EBIOE/AN19/RPC4/PMRD/RC4 | 52 | USBID |
| 17 | EBID5/AN12/RPC1/PMD5/RC1 | 53 | TMS/SDCD/RA0 |
| 18 | VDDCORE | 54 | TRCLK/SDCK/SQICLK/RA6 |
| 19 | VDDIO | 55 | TRD3/SDDATA3/SQID3/RA7 |
| 20 | No Connect | 56 | TRD1/SDDATA1/SQID1/RG12 |
| 21 | VSS | 57 | VDDR1V8(5) |
| 22 | VSS | 58 | VDDR1V8(5) |
| 23 | EBID6/AN16/PMD6/RE6 | 59 | VDDR1V8(5) |
| 24 | EBID7/AN15/PMD7/RE7 | 60 | VDDR1V8(5) |
| 25 | AN25/RPE8/RE8 | 61 | VDDR1V8(5) |
| 26 | AN26/RPE9/RE9 | 62 | VDDR1V8(5) |
| 27 | TDO/AN31/RPF12/RF12 | 63 | VDDR1V8(5) |
| 28 | TDI/AN17/SCK5/RF13 | 64 | TRD0/SDDATA0/SQID0/RG13 |
| 29 | VSS | 65 | TRD2/SDDATA2/SQID2/RG14 |
| 30 | AN14/C1IND/SCK2/RG6 | 66 | DDRVREF(6) |
| 31 | AN13/C1INC/RPG7/SDA4/RG7 | 67 | VDDR1V8(5) |
| 32 | AN30/C2IND/RPG8/SCL4/RG8 | 68 | VDDR1V8(5) |
| 33 | EBIA2/AN23/C2INC/RPG9/PMA2/RG9 | 69 | EBIA6/RPE5/PMA6/RE5 |
| 34 | AN21/RG15 | 70 | SDCMD/SQICS0/RPD4/RD4 |
| 35 | AN20/RH4 | 71 | SQICS1/RPD5/RD5 |
| 36 | EBID1/AN39/PMD1/RE1 | 72 | VDDR1V8(5) |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
**2:** Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
**3:** Shaded pins are 5V tolerant.
**4:** The metal plane at the bottom of the device is internally tied to VSS1V8 and should be connected to 1.8V ground externally.
**5:** This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
**6:** This pin is a No Connect in devices without DDR.
**7:** These pins are restricted to input functions only.

**TABLE 4-23: SYSTEM BUS TARGET PROTECTION GROUP 13 REGISTER MAP**

| Virtual Address (BF91_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 8420 | SBT13ELOG1 | 31:16 | MULTI | — | — | — | CODE<3:0> | | | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | INITID<7:0> | | | | | | | | REGION<3:0> | | | | — | CMD<2:0> | | | 0000 |
| 8424 | SBT13ELOG2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | GROUP<1:0> | | 0000 |
| 8428 | SBT13ECON | 31:16 | — | — | — | — | — | — | — | ERRP | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 8430 | SBT13ECLRS | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CLEAR | 0000 |
| 8438 | SBT13ECLRM | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CLEAR | 0000 |
| 8440 | SBT13REG0 | 31:16 | BASE<21:6> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | BASE<5:0> | | | | | | PRI | — | SIZE<4:0> | | | | | — | — | — | xxxx |
| 8450 | SBT13RD0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8458 | SBT13WR0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8460 | SBT13REG1 | 31:16 | BASE<21:6> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | BASE<5:0> | | | | | | PRI | — | SIZE<4:0> | | | | | — | — | — | xxxx |
| 8470 | SBT13RD1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8478 | SBT13WR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note:** For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

## 6.0 RESETS

**Note:** This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

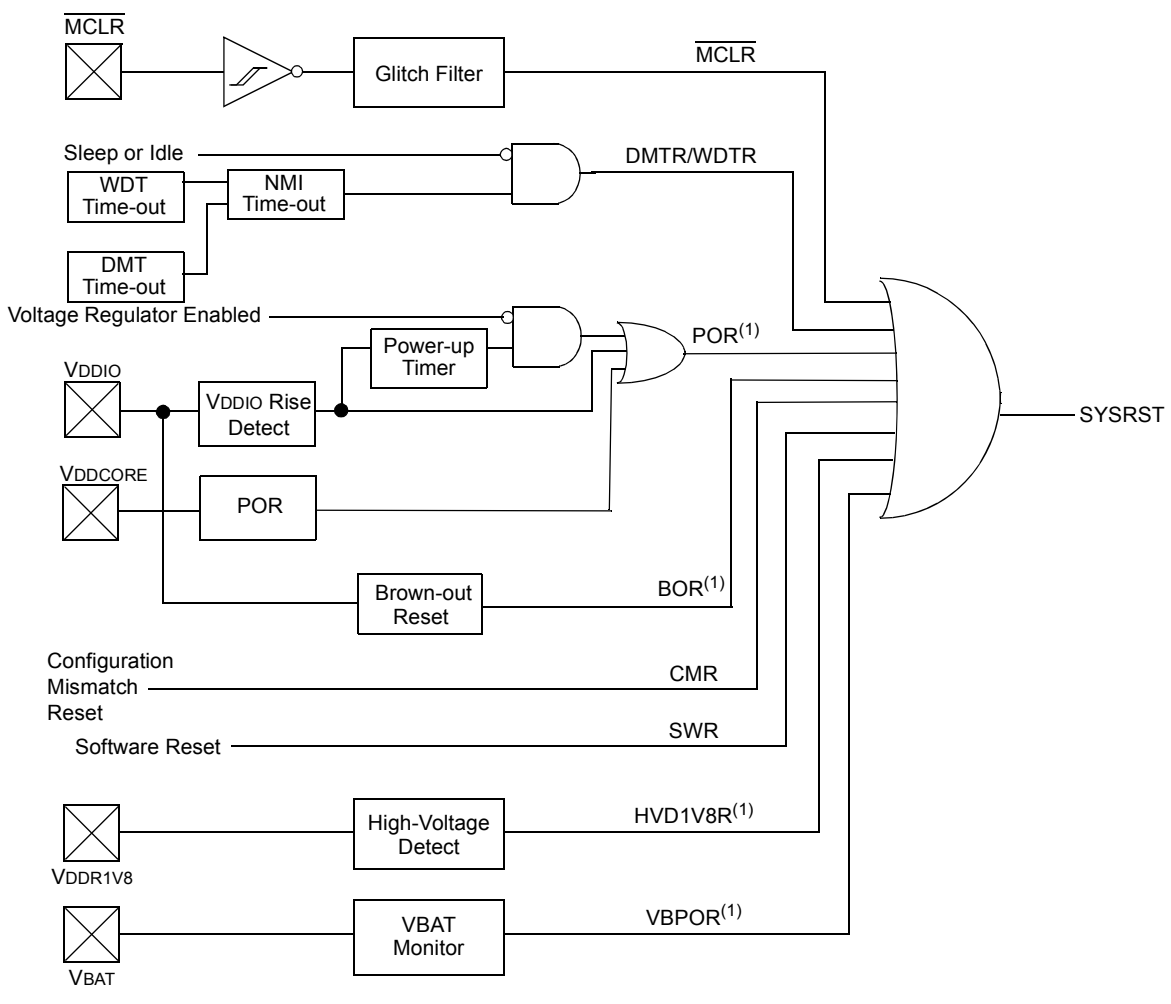
The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- VBAT Power-on Reset (VBPOR)
- High Voltage Detect Reset (HVD1V8R) on $V_{DDR1V8}$
- Master Clear Reset pin ($\overline{MCLR}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

All types of device Reset will set a corresponding Status bit in the RCON register (see Register 6-1) to indicate the type of reset.

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

**FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM**




**Note 1:** Refer to Table 44-4 for various RESET specifications.

## 10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

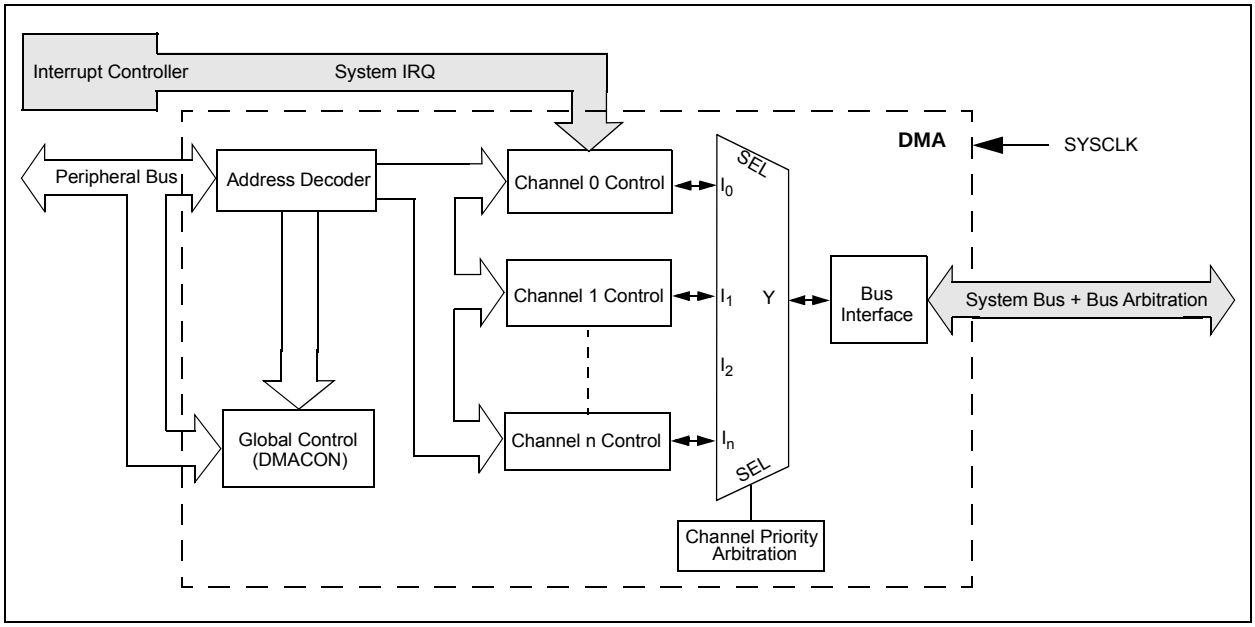
**Note:** This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the device such as SPI, UART, PMP, etc., or memory itself.

Following are some of the key features of the DMA Controller module:

- Eight identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Up to 2-byte Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent error address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

**FIGURE 10-1: DMA BLOCK DIAGRAM**



The timer source for each Input Capture module depends on the setting of the ICACLK bit in the CFGCON register. The available configurations are shown in Table 15-1.

**TABLE 15-1: TIMER SOURCE CONFIGURATIONS**

| Input Capture Module | Timerx | Timery |
|---|---|---|
| ICACLK (CFGCON<17>) = 0 | | |
| IC1<br>•<br>•<br>•<br>IC9 | Timer2<br>•<br>•<br>•<br>Timer 2 | Timer3<br>•<br>•<br>•<br>Timer 3 |
| ICACLK (CFGCON<17>) = 1 | | |
| IC1 | Timer4 | Timer5 |
| IC2 | Timer4 | Timer5 |
| IC3 | Timer4 | Timer5 |
| IC4 | Timer2 | Timer3 |
| IC5 | Timer2 | Timer3 |
| IC6 | Timer2 | Timer3 |
| IC7 | Timer6 | Timer7 |
| IC8 | Timer6 | Timer7 |
| IC9 | Timer6 | Timer7 |

## 17.1 Deadman Timer Control Registers

**TABLE 17-1: DEADMAN TIMER REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0A00 | DMTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 0A10 | DMTPRECLR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | STEP1<7:0> | | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| 0A20 | DMTCLR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | STEP2<7:0> | | | | | | | | 0000 |
| 0A30 | DMTSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BAD1 | BAD2 | DMTEVENT | — | — | — | — | WINOPN | 0000 |
| 0A40 | DMTCNT | 31:16 | COUNTER<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0A60 | DMTPSCNT | 31:16 | PSCNT<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0A70 | DMTPSINTV | 31:16 | PSINTV<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 17-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | PSINTV<31:24> | | | | | | | |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | PSINTV<23:16> | | | | | | | |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | PSINTV<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | PSINTV<7:0> | | | | | | | |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit |
| -n = Bit Value at POR: (‘0’, ‘1’, x = unknown) | P = Programmable bit | r = Reserved bit |

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits
This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

## 18.0 WATCHDOG TIMER (WDT)

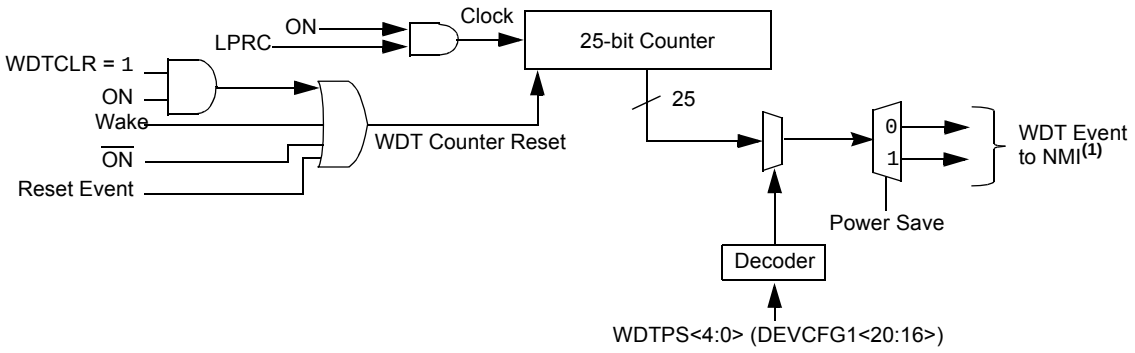
**Note:** This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

When enabled, the Watchdog Timer (WDT) operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

**FIGURE 18-1: WATCHDOG TIMER BLOCK DIAGRAM**




**Note 1:** Refer to **Section 6.0 "Resets"** for more information.

**REGISTER 22-26: SQI1XCON4: SQI XIP CONTROL REGISTER 4**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INIT2SCHECK | INIT2COUNT<1:0> | | INIT2TYPE<1:0> | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | INIT2CMD3<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | INIT2CMD2<7:0> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | INIT2CMD1<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT2SCHECK:** Flash Initialization 2 Command Status Check bit
1 = Check the status after executing the INIT2 commands
0 = Do not check the status

bit 27-26 **INIT2COUNT<1:0>:** Flash Initialization 2 Command Count bits
11 = INIT2CMD1, INIT2CMD2, and INIT2CMD3 are sent
10 = INIT2CMD1 and INIT2CMD2 are sent, but INIT2CMD3 is still pending
01 = INIT2CMD1 is sent, but INIT2CMD2 and INIT2CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT2TYPE<1:0>:** Flash Initialization 2 Command Type bits
11 = Reserved
10 = INIT2 commands are sent in Quad Lane mode
01 = INIT2 commands are sent in Dual Lane mode
00 = INIT2 commands are sent in Single Lane mode

bit 24-16 **INIT2CMD3<7:0>:** Flash Initialization Command 3 bits
Third command of the Flash initialization.

bit 15-8 **INIT2CMD2<7:0>:** Flash Initialization Command 2 bits
Second command of the Flash initialization.

bit 7-0 **INIT2CMD1<7:0>:** Flash Initialization Command 1 bits
First command of the Flash initialization.

**Note:** Some Flash devices require write enable and sector unprotect commands before write/read operations and this register is useful in working with those Flash types (XIP mode only)

Figure 24-2 and Figure 24-3 illustrate typical receive and transmit timing for the UART module.

**FIGURE 24-2: UART RECEPTION**

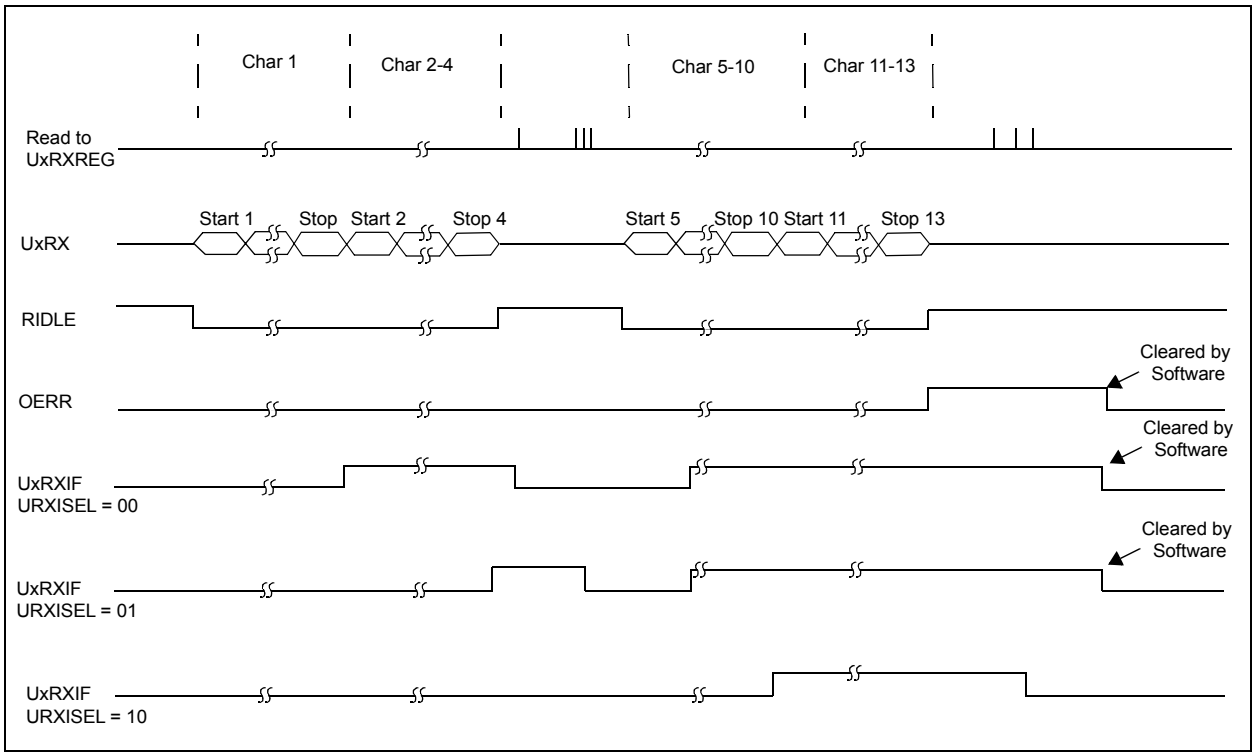
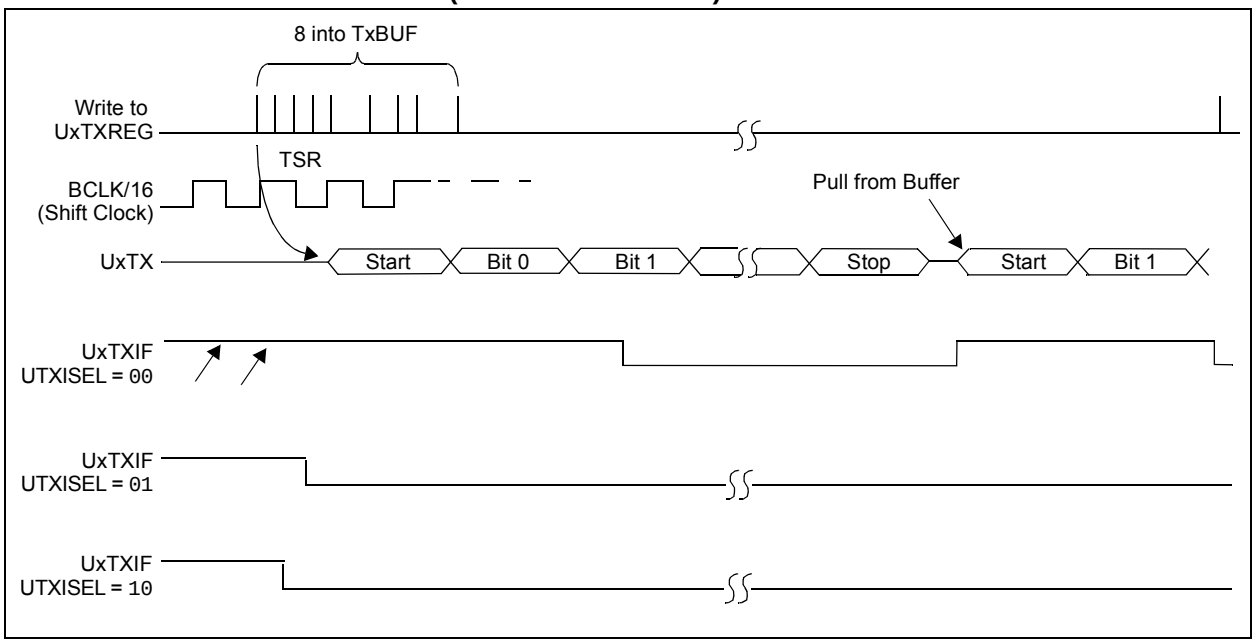



**FIGURE 24-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**



**REGISTER 26-1: EBICSx: EXTERNAL BUS INTERFACE CHIP SELECT REGISTER ('x' = 0-3)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSADDR<15:8> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSADDR<7:0> | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **CSADDR<15:0>:** Base Address for Device bits
Address in physical memory, which will select the external device.

bit 15-0 **Unimplemented:** Read as '0'

Table 27-12 shows the Security Association control word structure.

The Crypto Engine fetches different structures for different flows and ensures that hardware fetches minimum words from SA required for processing. The structure is ready for hardware optimal data fetches.

**FIGURE 27-12: FORMAT OF SA_CTRL**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31-24 | — | — | VERIFY | — | NO_RX | OR_EN | ICVONLY | IRFLAG |
| 23-16 | LNC | LOADIV | FB | FLAGS | — | — | — | ALGO<6> |
| 15-8 | ALGO<5:0> | | | | | | ENC | KEY SIZE<1> |
| 7-0 | KEY SIZE<0> | MULTITASK<2:0> | | | CRYPTOALGO<3:0> | | | |

bit 31-30 **Reserved:** Do not use

bit 29 **VERIFY:** NIST Procedure Verification Setting
1 = NIST procedures are to be used
0 = Do not use NIST procedures

bit 28 **Reserved:** Do not use

bit 27 **NO_RX:** Receive DMA Control Setting
1 = Only calculate ICV for authentication calculations
0 = Normal processing

bit 26 **OR_EN:** OR Register Bits Enable Setting
1 = OR the register bits with the internal value of the CSR register
0 = Normal processing

bit 25 **ICVONLY:** Incomplete Check Value Only Flag
This affects the SHA-1 algorithm only. It has no effect on the AES algorithm.
1 = Only three words of the HMAC result are available
0 = All results from the HMAC result are available

bit 24 **IRFLAG:** Immediate Result of Hash Setting
This bit is set when the immediate result for hashing is requested.
1 = Save the immediate result for hashing
0 = Do not save the immediate result

bit 23 **LNC:** Load New Keys Setting
1 = Load a new set of keys for encryption and authentication
0 = Do not load new keys

bit 22 **LOADIV:** Load IV Setting
1 = Load the IV from this Security Association
0 = Use the next IV

bit 21 **FB:** First Block Setting
This bit indicates that this is the first block of data to feed the IV value.
1 = Indicates this is the first block of data
0 = Indicates this is not the first block of data

bit 20 **FLAGS:** Incoming/Outgoing Flow Setting
1 = Security Association is associated with an outgoing flow
0 = Security Association is associated with an incoming flow

bit 19-17 **Reserved:** Do not use

**REGISTER 28-3: RNGPOLYx: RANDOM NUMBER GENERATOR POLYNOMIAL REGISTER 'x' ('x' = 1 OR 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | POLY<31:24> | | | | | | | |
| 23:16 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | POLY<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | POLY<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | POLY<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **POLY<31:0>:** PRNG LFSR Polynomial MSb/LSb bits (RNGPOLY1 = LSb, RNGPOLY2 = MSb)

**REGISTER 28-4: RNGNUMGENx: RANDOM NUMBER GENERATOR REGISTER 'x' ('x' = 1 OR 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | RNG<31:24> | | | | | | | |
| 23:16 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | RNG<23:16> | | | | | | | |
| 15:8 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | RNG<15:8> | | | | | | | |
| 7:0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | RNG<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **RNG<31:0>:** Current PRNG MSb/LSb Value bits (RNGNUMGEN1 = LSb, RNGNUMGEN2 = MSb)

**REGISTER 29-25: ADCDATAx: ADC OUTPUT DATA REGISTER 'x' ('x' = 0 THROUGH 43)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<31:24> | | | | | | | |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<23:16> | | | | | | | |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

**Note 1:** When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

**2:** Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

**REGISTER 30-9: CiRXMN: CAN ACCEPTANCE FILTER MASK N REGISTER (N = 0, 1, 2 OR 3)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SID<10:3> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | SID<2:0> | | | — | MIDE | — | EID<17:16> | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Include bit, SIDx, in filter comparison
0 = Bit SIDx is 'don't care' in filter operation

bit 20 **Unimplemented:** Read as '0'

bit 19 **MIDE:** Identifier Receive Mode bit
1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Include bit, EIDx, in filter comparison
0 = Bit EIDx is 'don't care' in filter operation

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

**REGISTER 31-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER (CONTINUED)**

bit 6 **TXBUSY:** Transmit Busy bit(2,6)

1 = TX logic is receiving data
0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

bit 5 **RXBUSY:** Receive Busy bit(3,6)

1 = RX logic is receiving data
0 = RX logic is idle

This bit indicates that a packet is currently being received. A change in this status bit is not necessarily reflected by the RXDONE interrupt, as RX packets may be aborted or rejected by the RX filter.

bit 4-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is only used for RX operations.
**2:** This bit is only affected by TX operations.
**3:** This bit is only affected by RX operations.
**4:** This bit is affected by TX and RX operations.
**5:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
**6:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

**REGISTER 31-26: EMAC1IPGR: ETHERNET CONTROLLER MAC NON-BACK-TO-BACK INTERPACKET GAP REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| | — | NB2BIPKTGP1<6:0> | | | | | | |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 |
| | — | NB2BIPKTGP2<6:0> | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14-8 **NB2BIPKTGP1<6:0>:** Non-Back-to-Back Interpacket Gap Part 1 bits

This is a programmable field representing the optional carrierSense window referenced in section 4.2.3.2.1 "Deference" of the IEEE 80.23 Specification. If carrier is detected during the timing of IPGR1, the MAC defers to carrier. If, however, carrier becomes after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to medium. Its range of values is 0x0 to IPGR2. Its recommend value is 0xC (12d).

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **NB2BIPKTGP2<6:0>:** Non-Back-to-Back Interpacket Gap Part 2 bits

This is a programmable field representing the non-back-to-back Inter-Packet-Gap. Its recommended value is 0x12 (18d), which represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps).

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 39-3: SDHCMODE: SDHC MODE REGISTER (CONTINUED)**

bit 4 **DTXDSEL:** Data Transfer Direction Select bit
1 = Read (card to SDHC)
0 = Write (SDHC to card)

bit 3-2 **ACEN<1:0>:** Auto CMD12 Enable bits
Auto CMD12 is used to stop multiple-block read/write operations.
11 = Reserved
10 = Reserved
01 = Auto CMD12 is enabled
00 = Auto CMD 12 is disabled

bit 1 **BCEN:** Block Count Enable Bit
1 = Block count is enabled
0 = Block count is disabled

bit 0 **DMAEN:** DMA Enable bit
1 = DMA (ADMA) is used to transfer data
0 = CPU is used to transfer data

**Note 1:** Refer to bits 45-40 of the command format in the *"SD Host Controller Simplified Specification"* (version 2.00).

**2:** If these bits are set to '1', the SDHC will check the index field in the response to see if it has the same value as the CIDX<5:0> bits, if not, it will be reported as a command index error.

**3:** If these bits are set to '1', the SDHC will check the CRC field in the response and reports a command CRC error upon a CRC error detection.

**FIGURE 44-20: CANx MODULE I/O TIMING CHARACTERISTICS**

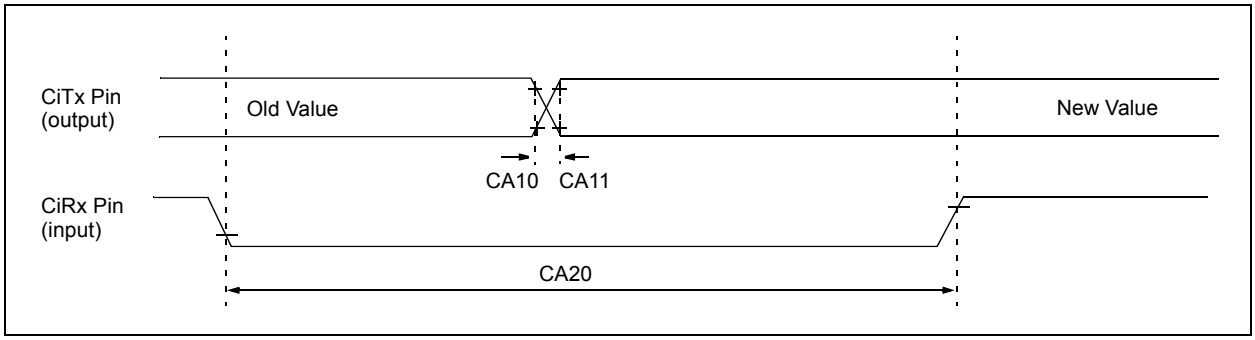



**TABLE 44-44: CANx MODULE I/O TIMING REQUIREMENTS**

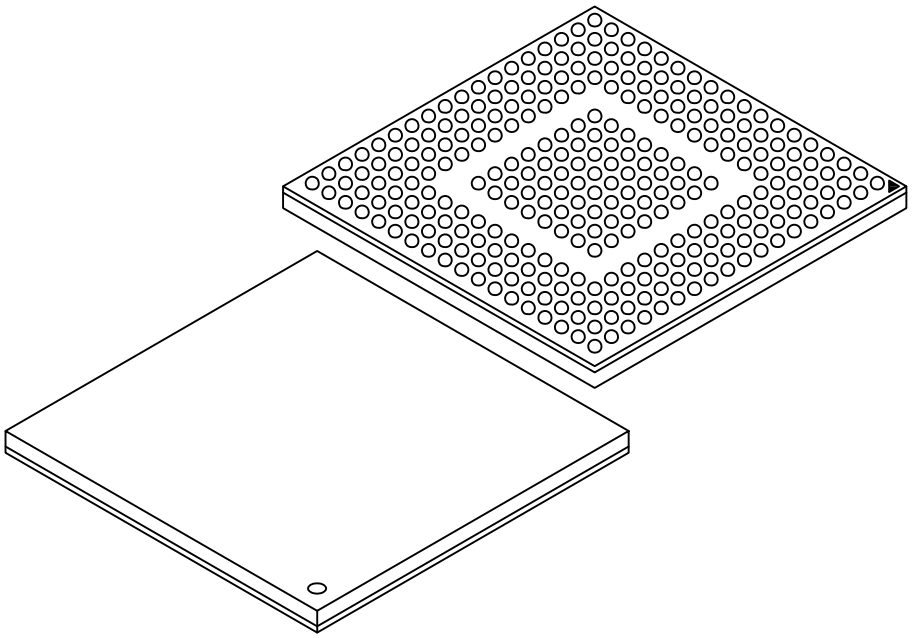
| AC CHARACTERISTICS | | | Standard Operating Conditions: $V_{DDIO}$ = 2.2V to 3.6V, $V_{DDCORE}$ = 1.7V to 1.9V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| CA10 | TioF | Port Output Fall Time | — | — | — | ns | See parameter DO32 |
| CA11 | TioR | Port Output Rise Time | — | — | — | ns | See parameter DO31 |
| CA20 | Tcwf | Pulse Width to Trigger CAN Wake-up Filter | 700 | — | — | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

### 288 Ball Low Profile Fine Pitch Ball Grid Array (4J) - 15x15x1.4 mm Body [LFBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals (Balls) | N | | 288 | |
| Pitch | e | | 0.80 BSC | |
| Overall Height | A | - | - | 1.40 |
| Terminal (Ball) Height | A1 | 0.30 | 0.35 | 0.40 |
| Mold Cap Height | (A2) | | 0.70 REF | |
| Substrate Thickness | (A3) | | 0.26 REF | |
| Overall Length | D | | 15.00 BSC | |
| Overall Ball Pitch | D1 | | 13.60 BSC | |
| Overall Width | E | | 15.00 BSC | |
| Overall Ball Pitch | E1 | | 13.60 BSC | |
| Ball Diameter | b | 0.40 | 0.45 | 0.50 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-366B Sheet 2 of 2