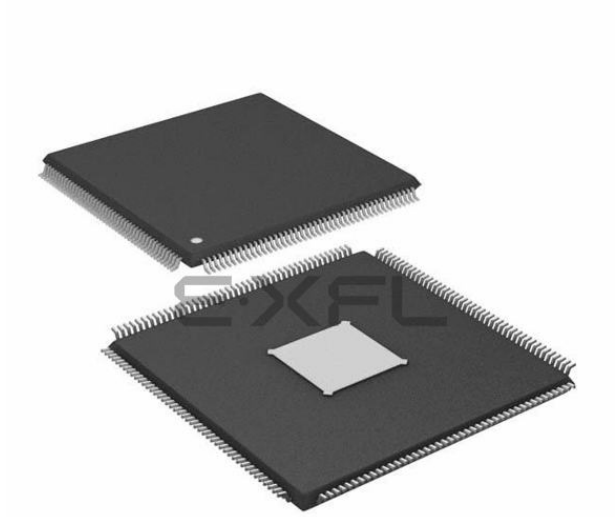

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What is "Embedded - Microcontrollers"?

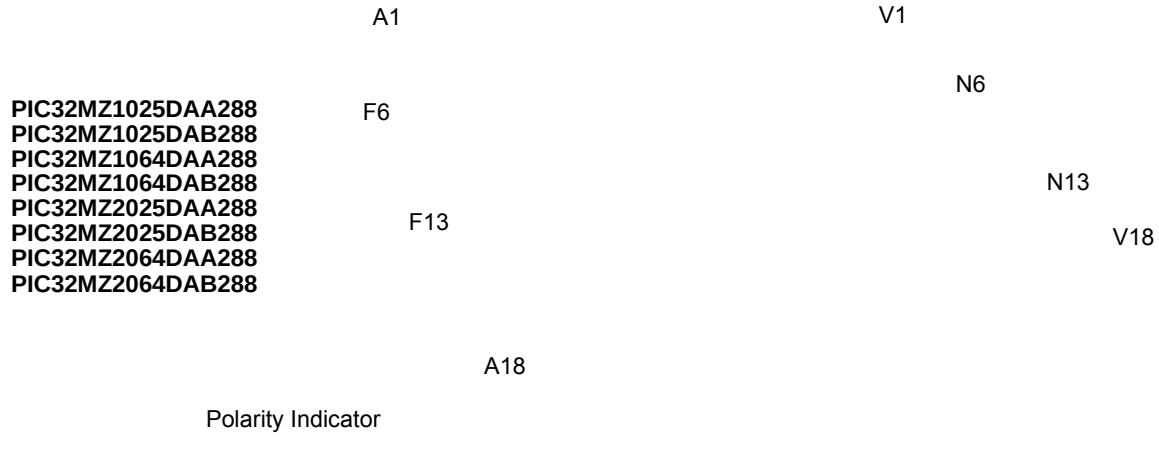
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025dab176t-i-2j

TABLE 7: PIN NAMES FOR 288-PIN DEVICES

288-PIN LFBGA (BOTTOM VIEW)



PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288

Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
A1	No Connect	B17	AN2/C1INB/RB4
A2	$\overline{\text{DDRUDQS}}$	B18	EBIA5/AN7/PMA5/RA5
A3	DDRDM1	C1	DDRDQ8
A4	D-	C2	DDRDQ15
A5	VSS	C3	DDRDQ9
A6	INT0/RH14	C4	VUSB3V3
A7	RPF2/SDA3/RF2	C5	VBUS
A8	AN21/RG15	C6	USBID
A9	AN14/C1IND/SCK2/RG6	C7	VSS
A10	TDI/AN17/SCK5/RF13	C8	No Connect
A11	TDO/AN31/RPF12/RF12	C9	AN30/C2IND/RPG8/SCL4/RG8
A12	EBID5/AN12/RPC1/PMD5/RC1	C10	AN25/RPE8/RE8
A13	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	C11	EBID6/AN16/PMD6/RE6
A14	PGEC1/AN9/RPB1/CTED1/RB1	C12	No Connect
A15	EBID10/AN4/RPB8/PMD10/RB8	C13	EBID12/AN10/RPC2/PMD12/RC2
A16	AN8/RPB3/RB3	C14	AN49/RB11
A17	VREF-/CVREF-/AN27/RA9	C15	VREF+/CVREF+/AN28/RA10
A18	No Connect	C16	VDDIO
B1	No Connect	C17	AN1/C2INB/RPB2/RB2
B2	DDRUDQS	C18	AN6/RB12
B3	DDRDQ14	D1	DDRDQ13
B4	D+	D2	DDRDQ10
B5	VSS	D3	VSS1V8
B6	EBID4/AN18/PMD4/RE4	D4	TMS/$\overline{\text{SDCD}}$/RA0
B7	EBID0/PMD0/RE0	D5	VUSB3V3
B8	AN20/RH4	D6	No Connect
B9	EBIA2/AN23/C2INC/RPG9/PMA2/RG9	D7	VDDCORE
B10	AN26/RPE9/RE9	D8	EBID1/AN39/PMD1/RE1
B11	EBID7/AN15/PMD7/RE7	D9	AN13/C1INC/RPG7/SDA4/RG7
B12	No Connect	D10	VSS
B13	$\overline{\text{EBIWE}}$/AN34/RPC3/PMWR/RC3	D11	VSS
B14	PGEC2/RPB6/RB6	D12	VSS
B15	AN48/CTPLS/RB13	D13	VSS
B16	AN3/C2INA/RPB15/OCFB/RB15	D14	VDDCORE

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.

5: This pin is a No Connect when DDR is not connected in the system.

6: These pins are restricted to input functions only.

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Analog-to-Digital Converter						
AN0	C12	169	D18	I	Analog	Analog Input Channels
AN1	A13	172	C17	I	Analog	
AN2	A12	175	B17	I	Analog	
AN3	B10	7	B16	I	Analog	
AN4	A9	10	A15	I	Analog	
AN5	C11	168	E18	I	Analog	
AN6	B13	171	C18	I	Analog	
AN7	A11	174	B18	I	Analog	
AN8	A10	8	A16	I	Analog	
AN9	B9	11	A14	I	Analog	
AN10	A8	14	C13	I	Analog	
AN11	H11	135	R17	I	Analog	
AN12	B7	17	A12	I	Analog	
AN13	D5	31	D9	I	Analog	
AN14	E5	30	A9	I	Analog	
AN15	C7	24	B11	I	Analog	
AN16	F6	23	C11	I	Analog	
AN17	A6	28	A10	I	Analog	
AN18	B3	43	B6	I	Analog	
AN19	B8	16	A13	I	Analog	
AN20	D4	35	B8	I	Analog	
AN21	A5	34	A8	I	Analog	
AN22	E9	158	J18	I	Analog	
AN23	C5	33	B9	I	Analog	
AN24	E11	160	H16	I	Analog	
AN25	E6	25	C10	I	Analog	
AN26	D6	26	B10	I	Analog	
AN27	B11	1	A17	I	Analog	
AN28	C10	2	C15	I	Analog	
AN29	E10	159	J17	I	Analog	
AN30	B5	32	C9	I	Analog	
AN31	C6	27	A11	I	Analog	
AN32	F10	152	K16	I	Analog	
AN33	F11	157	J16	I	Analog	
AN34	A7	15	B13	I	Analog	
AN35	J13	140	P18	I	Analog	
AN36	J12	139	N15	I	Analog	
AN37	K13	138	P17	I	Analog	
AN38	J11	136	R18	I	Analog	
AN39	A4	36	D8	I	Analog	
AN45	D11	167	E17	I	Analog	
AN46	D12	170	D17	I	Analog	
AN47	B12	173	E16	I	Analog	
AN48	F7	9	B15	I	Analog	
AN49	E7	12	C14	I	Analog	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MZ DA family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDDIO, VDDCORE, and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VBAT pin (see **2.2 "Decoupling Capacitors"**)
- All VDDR1V8 and VSS1V8 pins (see **2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **2.3 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming (ICSP™) and debugging purposes (see **2.4 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **2.7 "External Oscillator Pins"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

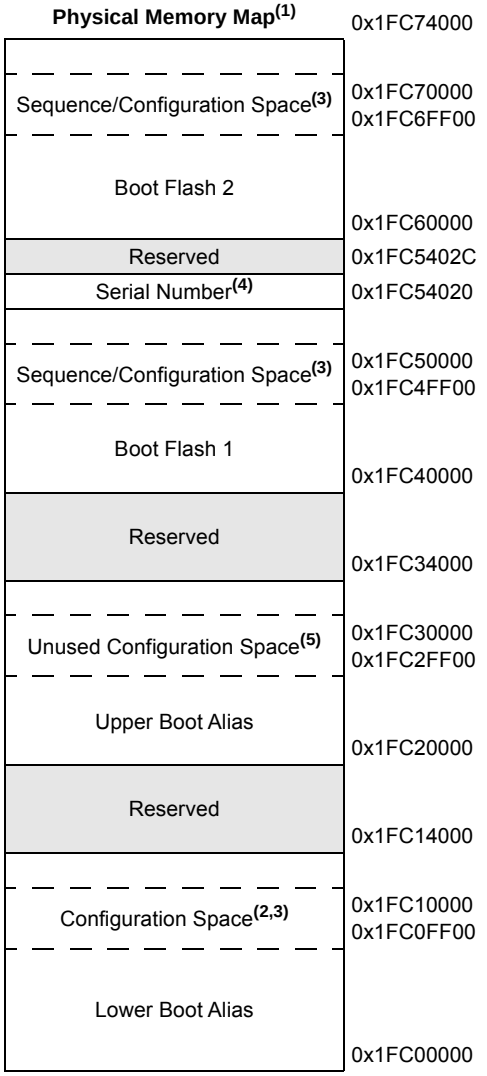
2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDDIO, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** It is recommended that two parallel capacitors with a value of 0.1 µF (100 nF, 10-20V) and a value of 0.01 µF be used. The 0.1 µF capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. Place both capacitors in close proximity and consider implementing the pair of capacitances as close to the power and ground pins as possible. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 4-2: BOOT AND ALIAS MEMORY MAP



Note 1: Memory areas are not shown to scale.

2: Memory locations 0x1FC0FF40 through 0x1FC0FFFC are used to initialize Configuration registers (see **Section 41.0 "Special Features"**).

3: Refer to **Section 4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

4: Memory location 0x1FC54020 contains a unique device serial number (see **Section 41.0 "Special Features"**).

5: This configuration space cannot be used for executing code in the upper boot alias.

TABLE 4-2: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
System Bus(1)	0xBF8F0000	0x0000
SDHC	0xBF8E0000	0xC000
GPU		0xB000
GLCD		0xA000
DDRPHY		0x9100
DDRC		0x8000
RNG		0x6000
Crypto		0x5000
USB		0x3000
SQI1		0x2000
EBI		0x1000
Prefetch		0x0000
DSCTRL	0xBF8C0000	0x0200
RTCC		0x0000
USBCR	0xBF880000	0x4000
Ethernet		0x2000
CAN1 and CAN2		0x0000
PORTA-PORTK	0xBF860000	0x0000
CTMU	0xBF840000	0xC200
Comparator 1, 2		0xC000
ADC		0xB000
OC1-OC9		0x4000
IC1-IC9		0x2000
Timer1-Timer9		0x0000
PMP	0xBF820000	0xE000
UART1-UART6		0x2000
SPI1-SPI6		0x1000
I2C1-I2C5		0x0000
DMA	0xBF810000	0x1000
Interrupt Controller		0x0000
HLVD	0xBF800000	0x1800
PPS		0x1400
Oscillator		0x1200
CVREF		0x0E00
Deadman Timer		0x0A00
Watchdog Timer		0x0800
Flash Controller		0x0600
Configuration		0x0000

Note 1: Refer to **4.4 "System Bus Arbitration"** for important legal information.

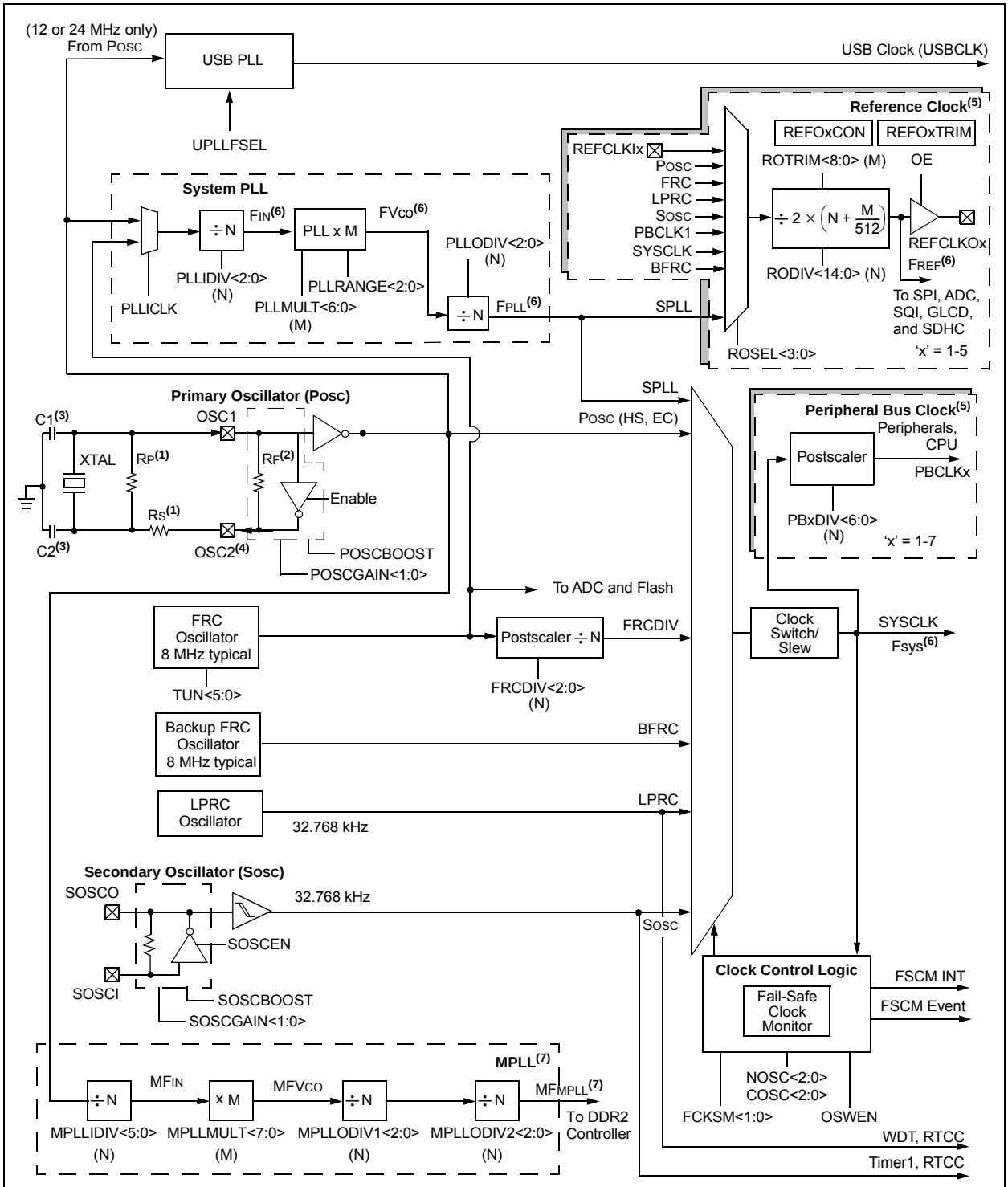
TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Analog Circuit Ready	_ADC_ARDY_VECTOR	197	OFF197<17:1>	IFS6<5>	IEC6<5>	IPC49<12:10>	IPC49<9:8>	Yes
ADC Update Ready	_ADC_URDY_VECTOR	198	OFF198<17:1>	IFS6<6>	IE6<6>	IPC49<20:18>	IPC49<17:16>	Yes
ADC0 Early Interrupt	_ADC0_EARLY_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
ADC1 Early Interrupt	_ADC1_EARLY_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
ADC2 Early Interrupt	_ADC2_EARLY_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes
ADC3 Early Interrupt	_ADC3_EARLY_VECTOR	202	OFF202<17:1>	IFS6<10>	IEC6<10>	IPC50<20:18>	IPC50<17:16>	Yes
ADC4 Early Interrupt	_ADC4_EARLY_VECTOR	203	OFF203<17:1>	IFS6<11>	IEC6<11>	IPC50<28:26>	IPC50<25:24>	Yes
Reserved	—	—	—	—	—	—	—	—
ADC Group Early Interrupt Request	_ADC_EARLY_VECTOR	205	OFF205<17:1>	IFS6<13>	IEC6<13>	IPC51<12:10>	IPC51<9:8>	Yes
ADC7 Early Interrupt	_ADC7_EARLY_VECTOR	206	OFF206<17:1>	IFS6<14>	IEC6<14>	IPC51<20:18>	IPC51<17:16>	Yes
ADC0 Warm Interrupt	_ADC0_WARM_VECTOR	207	OFF207<17:1>	IFS6<15>	IEC6<15>	IPC51<28:26>	IPC51<25:24>	Yes
ADC1 Warm Interrupt	_ADC1_WARM_VECTOR	208	OFF208<17:1>	IFS6<16>	IEC6<16>	IPC52<4:2>	IPC52<1:0>	Yes
ADC2 Warm Interrupt	_ADC2_WARM_VECTOR	209	OFF209<17:1>	IFS6<17>	IEC6<17>	IPC52<12:10>	IPC52<9:8>	Yes
ADC3 Warm Interrupt	_ADC3_WARM_VECTOR	210	OFF210<17:1>	IFS6<18>	IEC6<18>	IPC52<20:18>	IPC52<17:16>	Yes
ADC4 Warm Interrupt	_ADC4_WARM_VECTOR	211	OFF211<17:1>	IFS6<19>	IEC6<19>	IPC52<28:26>	IPC52<25:24>	Yes
Reserved	—	—	—	—	—	—	—	—
Reserved	—	—	—	—	—	—	—	—
ADC7 Warm Interrupt	_ADC7_WARM_VECTOR	214	OFF214<17:1>	IFS6<22>	IEC6<22>	IPC53<20:18>	IPC53<17:16>	Yes
MPLL Fault Interrupt	_MPLL_FAULT_VECTOR	215	OFF215<17:1>	IFS6<23>	IEC6<23>	IPC53<28:26>	IPC53<25:24>	Yes
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

FIGURE 8-1: PIC32MZ DA FAMILY OSCILLATOR DIAGRAM



Notes:
1. A series resistor, RS, may be required for AT strip cut crystals, or to eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.
2. The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
3. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the "*PIC32 Family Reference Manual*" for help in determining the best oscillator components.
4. PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.
5. Shaded regions indicate multiple instantiations of a peripheral or feature.
6. Refer to Table 44-25 in **Section 44.0 "Electrical Characteristics"** for frequency limitations.
7. Memory Phase-Locked Loop (MPLL) is controlled through the CFGMPLL register (see **41.0 "Special Features"** for details). MFMPLL drives the DDR2 PHY and is the source clock (DDRCK, $\overline{\text{DDRCK}}$) for DDR2 SDRAM.

NOTES:

REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXINTERV<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **RXFIFOSZ<3:0>:** Receive FIFO Size bits
1111 = Reserved
1110 = Reserved
1101 = 8192 bytes
1100 = 4096 bytes
•
•
•
0011 = 8 bytes
0010 = Reserved
0001 = Reserved
0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 27-24 **TXFIFOSZ<3:0>:** Transmit FIFO Size bits
1111 = Reserved
1110 = Reserved
1101 = 8192 bytes
1100 = 4096 bytes
•
•
•
0011 = 8 bytes
0010 = Reserved
0001 = Reserved
0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 23-16 **Unimplemented:** Read as '0'

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R/W-1, HS
	—	—	—	—	—	USBIF	USBRF	USBWKUP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	r-1	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	USB IDOVEN	USB IDVAL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **USBIF:** USB General Interrupt Flag bit
1 = An event on the USB Bus has occurred
0 = No interrupt from USB module or interrupts have not been enabled

bit 25 **USBRF:** USB Resume Flag bit
1 = Resume from Suspend state. Device wake-up activity can be started.
0 = No Resume activity detected during Suspend, or not in Suspend state

bit 24 **USBWKUP:** USB Activity Status bit
1 = Connect, disconnect, or other activity on USB detected since last cleared
0 = No activity detected on USB

Note: This bit should be cleared just prior to entering sleep, but it should be checked that no activity has already occurred on USB before actually entering sleep.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **Reserved:** Read as '1'

bit 14-10 **Unimplemented:** Read as '0'

bit 9 **USBIDOVEN:** USB ID Override Enable bit
1 = Enable use of USBIDVAL bit
0 = Disable use of USBIDVAL and instead use the PHY value

bit 8 **USBIDVAL:** USB ID Value bit
1 = ID override value is 1
0 = ID override value is 0

bit 7 **PHYIDEN:** PHY ID Monitoring Enable bit
1 = Enable monitoring of the ID bit from the USB PHY
0 = Disable monitoring of the ID bit from the USB PHY

bit 6 **VBUSMONEN:** VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in VBUS Valid range (between 4.4V and 4.75V)
0 = Disable monitoring for VBUS in VBUS Valid range

bit 5 **ASVALMONEN:** A-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for A-device (between 0.8V and 2.0V)
0 = Disable monitoring for VBUS in Session Valid range for A-device

bit 4 **BSVALMONEN:** B-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for B-device (between 0.8V and 4.0V)
0 = Disable monitoring for VBUS in Session Valid range for B-device

TABLE 22-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2044	SQI1BD STAT	31:16	—	—	—	—	—	—	—	—	—	—	BDSTATE<3:0>				DMA START	DMAACTV	0000
		15:0	BDCON<15:0>																0000
2048	SQI1BD POLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	POLLCON<15:0>																0000
204C	SQI1BD TXDSTAT	31:16	—	—	—	TXSTATE<3:0>				—	—	—	TXBUFCNT<5:0>						0000
		15:0	—	—	—	—	—	—	—	TXCURBUFLEN<8:0>									0000
2050	SQI1BD RXDSTAT	31:16	—	—	—	RXSTATE<3:0>				—	—	—	RXBUFCNT<5:0>						0000
		15:0	—	—	—	—	—	—	—	RXCURBUFLEN<8:0>									0000
2054	SQI1THR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THRES<3:0>				0000
2058	SQI1INT SIGEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE	0000
205C	SQI1 TAPCON	31:16	—	—	DDRCLKINDLY<5:0>						SDRDATINDLY<3:0>				DDRDATINDLY<3:0>				0000
		15:0	—	—	SDRCLKINDLY<5:0>						DATAOUTDLY<3:0>				CLKOUTDLY<3:0>				0000
2060	SQI1 MEMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	STATPOS	TYPESTAT<1:0>		STATBYTES<1:0>		0000
		15:0	STATCMD<15:0>																0000
2064	SQI1 XCON3	31:16	—	—	—	INIT1 SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>		INIT1CMD3<7:0>								0000
		15:0	INIT1CMD2<7:0>								INIT1CMD1<7:0>								0000
2068	SQI1 XCON4	31:16	—	—	—	INIT2 SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>		INIT2CMD3<7:0>								0000
		15:0	INIT2CMD2<7:0>								INIT2CMD1<7:0>								0000

REGISTER 25-6: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<15:14>(1)		PTEN<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<7:2>						PTEN<1:0>(2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Write '0'; ignore read

bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits
- 1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1(1)
- 0 = PMA15 and PMA14 function as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
- 1 = PMA<13:2> function as PMP address lines
- 0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits
- 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
- 0 = PMA1 and PMA0 pads function as port I/O

Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

REGISTER 27-2: CECON: CRYPTO ENGINE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **SWAPOEN:** Swap Output Data Enable bit
- 1 = Output data is byte swapped when written by dedicated DMA
- 0 = Output data is not byte swapped when written by dedicated DMA

bit 6 **SWRST:** Software Reset bit
- 1 = Initiate a software reset of the Crypto Engine
- 0 = Normal operation

bit 5 **SWAPEN:** I/O Swap Enable bit
- 1 = TFDMA inputs and RFDMA outputs are swapped
- 0 = TFDMA inputs and RFDMA outputs are not swapped

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **BDPCHST:** Buffer Descriptor Processor (BDP) Fetch Enable bit

This bit should be enabled only after all DMA descriptor programming is completed.
- 1 = BDP descriptor fetch is enabled
- 0 = BDP descriptor fetch is disabled

bit 1 **BDPPLEN:** Buffer Descriptor Processor Poll Enable bit

This bit should be enabled only after all DMA descriptor programming is completed.
- 1 = Poll for descriptor until valid bit is set
- 0 = Do not poll

bit 0 **DMAEN:** DMA Enable bit
- 1 = Crypto Engine DMA is enabled
- 0 = Crypto Engine DMA is disabled

REGISTER 28-5: RNGSEEDx: TRUE RANDOM NUMBER GENERATOR SEED REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SEED<31:0>:** TRNG MSb/LSb Value bits (RNGSEED1 = LSb, RNGSEED2 = MSb)

REGISTER 28-6: RNGCNT: TRUE RANDOM NUMBER GENERATOR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **RCNT<6:0>:** Number of Valid TRNG MSB 32 bits

29.0 12-BIT HIGH-SPEED SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MZ DA family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The 12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) includes the following features:

- 12-bit resolution
- Six ADC modules with dedicated Sample and Hold (S&H) circuits
- Two dedicated ADC modules can be combined in Turbo mode to provide double conversion rate (clock sources for combined ADCs must be synchronous)
- Up to 45 analog input sources, in addition to the internal CTMU, VBAT, internal voltage reference and internal temperature sensor
- Single-ended and/or differential inputs
- Can operate during Sleep mode
- Supports touch sense applications
- Six digital comparators
- Six digital filters supporting two modes:
  - Oversampling mode
  - Averaging mode
- 16-word FIFO on ADC0 through ADC4 for increased throughput
- Early interrupt generation resulting in faster processing of converted data
- Designed for motor control, power conversion, and general purpose applications
- Operation during Sleep and Idle modes

A simplified block diagram of the ADC module is illustrated in Figure 29-1.

The 12-bit HS SAR ADC has up to five dedicated ADC modules (ADC0-ADC4) and one shared ADC module (ADC7). The dedicated ADC modules use a single input (or its alternate) and are intended for high-speed and precise sampling of time-sensitive or transient inputs. The the shared ADC module incorporates a multiplexer on the input to facilitate a larger group of inputs, with slower sampling, and provides flexible automated scanning option through the input scan logic.

For each ADC module, the analog inputs are connected to the S&H capacitor. The clock, sampling time, and output data resolution for each ADC module can be set independently. The ADC module performs the conversion of the input analog signal based on the configurations set in the registers. When conversion is complete, the final result is stored in the result buffer for the specific analog input and is passed to the digital filter and digital comparator if configured to use data from this particular sample. Input to ADCx mapping is illustrated in Figure 29-2.

29.1 Activation Sequence

Step 1: Initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00. Then, configure the AICPMPEN bit (ADCCON1<12> and the IOANCPEN bit (CFGCON<7>) = 1 if and only if VDD is less than 2.5V. The default is '0', which assumes VDD is greater than or equal to 2.5V.

Step 2: The user writes all the essential ADC configuration SFRs including the ADC control clock and all ADC core clocks setup:

- ADCCON1, keeping the ON bit = 0
- ADCCON2, especially paying attention to ADCDIV<6:0> and SAMC<9:0>
- ADCANCON, keeping all analog enables ANENx bit = 0, WKUPCLKCNT bit = 0xA
- ADCCON3, keeping all DIGEN5x = 0, especially paying attention to ADCSEL<1:0>, CONCLKDIV <5:0>, and VREFSEL<2:0>
- ADCxTIME, ADCDIVx<6:0>, and SAMCx<9:0>
- ADCTRGMODE, ADCIMCONx, ADCTRGSNS, ADCCSSx, ADCGIRQENx, ADCTRGx, ADCBASE
- Comparators, filters, and so on

Step 3: The user sets the ANENx bit to '1' for the ADC SAR Cores needed (which internally in the ADC module enables the control clock to generate by division the core clocks for the desired ADC SAR Cores, which in turn enables the bias circuitry for these ADC SAR Cores).

REGISTER 29-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 10 **FSSCLKEN:** Fast Synchronous System Clock to ADC Control Clock bit
1 = Fast synchronous system clock to ADC control clock is enabled
0 = Fast synchronous system clock to ADC control clock is disabled

bit 9 **FSPBCLKEN:** Fast Synchronous Peripheral Clock to ADC Control Clock bit
1 = Fast synchronous peripheral clock to ADC control clock is enabled
0 = Fast synchronous peripheral clock to ADC control clock is disabled

bit 8-7 **Unimplemented:** Read as '0'

bit 6-4 **IRQVS<2:0>:** Interrupt Vector Shift bits
To determine interrupt vector address, this bit specifies the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with the ADCBASE register.
Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).
111 = Shift x left 7 bit position
110 = Shift x left 6 bit position
101 = Shift x left 5 bit position
100 = Shift x left 4 bit position
011 = Shift x left 3 bit position
010 = Shift x left 2 bit position
001 = Shift x left 1 bit position
000 = Shift x left 0 bit position

bit 3 **STRGLVL:** Scan Trigger High Level/Positive Edge Sensitivity bit
1 = Scan trigger is high level sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), the scan trigger will continue for all selected analog inputs, until the STRIG option is removed.
0 = Scan trigger is positive edge sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), only a single scan trigger will be generated, which will complete the scan of all selected analog inputs.

bit 2-0 **Unimplemented:** Read as '0'

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 "Output Compare"** and Figure 32-1 in **32.0 "Comparator"** for more information.

REGISTER 29-11: ADCCSS2: ADC COMMON SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CSS43	CSS42	CSS41	CSS40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS39	CSS38	CSS37	CSS36	CSS35	CSS34	CSS33	CSS32

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-0 **CSS43:CSS32:** Analog Common Scan Select bits
Analog inputs 43 to 32 are always Class 3, as there are only 32 triggers available.
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

REGISTER 31-31: EMAC1MCFG: ETHERNET CONTROLLER MAC MII MANAGEMENT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RESETMGMT	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKSEL<3:0>(1)				NOPRE	SCANINC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RESETMGMT:** Test Reset MII Management bit
1 = Reset the MII Management module
0 = Normal Operation

bit 14-6 **Unimplemented:** Read as '0'

bit 5-2 **CLKSEL<3:0>:** MII Management Clock Select 1 bits(1)
These bits are used by the clock divide logic in creating the MII Management Clock (MDC), which the IEEE 802.3 Specification defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz.

bit 1 **NOPRE:** Suppress Preamble bit
1 = The MII Management will perform read/write cycles without the 32-bit preamble field. Some PHYs support suppressed preamble
0 = Normal read/write cycles are performed

bit 0 **SCANINC:** Scan Increment bit
1 = The MII Management module will perform read cycles across a range of PHYs. The read cycles will start from address 1 through the value set in EMAC1MADR<PHYADDR>
0 = Continuous reads of the same PHY

Note 1: Table 31-5 provides a description of the clock divider encoding.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 31-5: MIIM CLOCK SELECTION

MIIM Clock Select	EMAC1MCFG<5:2>
TPBCLK5 divided by 4	000x
TPBCLK5 divided by 6	0010
TPBCLK5 divided by 8	0011
TPBCLK5 divided by 10	0100
TPBCLK5 divided by 14	0101
TPBCLK5 divided by 20	0110
TPBCLK5 divided by 28	0111
TPBCLK5 divided by 40	1000
TPBCLK5 divided by 48	1001
TPBCLK5 divided by 50	1010
Undefined	Any other combination

REGISTER 38-6: DDRMEMCFG0: DDR MEMORY CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	APCHRGEN	—	CLHADDR<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CSADDR<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	BNKADDR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RWADDR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30 **APCHRGEN:** Automatic Precharge Enable bit

When set, this bit issues an auto-precharge command to close the bank at the end of every user command. If the command accesses more than one bank before completing, all banks accessed are auto-precharged.

1 = Issue an auto-precharged command

0 = Do not issue an auto-precharged command

bit 29 **Unimplemented:** Read as '0'

bit 28-24 **CLHADDR<4:0>:** Column Address Shift bits

These bits specify how many bits the controller address must be right-shifted to put the high part of the column address to the immediate left of the low part of the column address. Used in conjunction with CLADDRHMSK (DDRMEMCFG2<26:0>) and CLADDRLMASK (DDRMEMCFG3<26:0>).

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **CSADDR<4:0>:** Chip Select Shift bits

These bits specify which bits of user address space are used to derive the Chip Select address for the DDR memory. Used in conjunction with CSADDRMASK (DDRMEMCFG4<10:8>).

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **BNKADDR<4:0>:** Bank Address Select Shift bits

These bits specify which bits of user address space are used to derive the bank address for the DDR memory. Used in conjunction with BNKADDRMASK (DDRMEMCFG4<2:0>).

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RWADDR<4:0>:** Row Address Select Shift bits

These bits specify which bits of user address space are used to derive the row address for the DDR memory. Used in conjunction with RWADDRMSK (DDRMEMCFG1<12:0>).

41.2 Registers

TABLE 41-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FFBC	DEVCFG4	31:16	—	—	—	SWDTPS<4;0>					—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFC0	DEVCFG3	31:16	—	—	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN	—	—	—	—	EXTDDRSIZE<3:0>				xxxx
		15:0	USERID<15:0>																xxxx
FFC4	DEVCFG2	31:16	—	UPLLFSEL	—	FDSEN	DSWDTEN	DSWDTOSC	DSWDTPS<4:0>					DSBOREN	VBATBOREN	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
FFC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
FFCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	POSCAGC	—	POSCTYPE<1:0>		—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>		—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
FFD0	DEVCP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD4	DEVCP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD8	DEVCP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFDC	DEVCP0	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE0	DEVSIGN3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE4	DEVSIGN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE8	DEVSIGN1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFEC	DEVSIGN0	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.