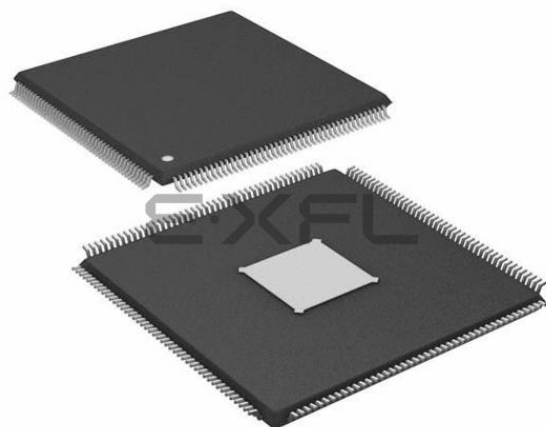




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025dag176-i-2j

PIC32MZ Graphics (DA) Family

TABLE 6: PIN NAMES FOR 176-PIN DEVICES (CONTINUED)

176-PIN LQFP (TOP VIEW) PIC32MZ1025DAA176 PIC32MZ1025DAB176 PIC32MZ1064DAA176 PIC32MZ1064DAB176 PIC32MZ2025DAA176 PIC32MZ2025DAB176 PIC32MZ2064DAA176 PIC32MZ2064DAB176 PIC32MZ1025DAG176 PIC32MZ1025DAH176 PIC32MZ1064DAG176 PIC32MZ1064DAH176 PIC32MZ2025DAG176 PIC32MZ2025DAH176 PIC32MZ2064DAG176 PIC32MZ2064DAH176		176	1
Pin Number	Full Pin Name	Pin Number	Full Pin Name
145	GD9/EBIBS0/RJ12	161	SOSCO/RPC14 ⁽⁷⁾ /T1CK/RC14 ⁽⁷⁾
146	GD18/EBIBS1/RJ10	162	SOSCI/RPC13 ⁽⁷⁾ /RC13 ⁽⁷⁾
147	GEN/EBICS3/RJ7	163	OSC2/CLKO/RC15
148	GCLK/EBICS2/RJ6	164	OSC1/CLKI/RC12
149	HSYNC/EBICS1/RJ5	165	VDDIO
150	VSYNC/EBICS0/RJ4	166	VBAT
151	GD20/EBIA22/RJ3	167	AN45/RPB5/RB5
152	EBIRDY3/AN32/RJ2	168	AN5/RPB10/RB10
153	Vss	169	PGED1/AN0/RPB0/CTED2/RB0
154	Vss	170	PGED2/C1INA/AN46/RPB7/RB7
155	VDDIO	171	AN6/RB12
156	VDDIO	172	AN1/C2INB/RPB2/RB2
157	AN33/SCK6/RD15	173	EBIA7/AN47/HLVDIN/RPB9/PMA7/RB9
158	AN22/RPD14/RD14	174	EBIA5/AN7/PMA5/RA5
159	AN29/SCK3/RB14	175	AN2/C1INB/RB4
160	TCK/AN24/RA1	176	No Connect

- Note** 1: The RPN pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and 12.4 "Peripheral Pin Select (PPS)" for restrictions.
- 2: Every I/O port pin (RAX-RKx) can be used as a change notification pin (CNAX-CNKx). See 12.0 "I/O Ports" for more information.
- 3: Shaded pins are 5V tolerant.
- 4: The metal plane at the bottom of the device is internally tied to Vss1v8 and should be connected to 1.8V ground externally.
- 5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
- 6: This pin is a No Connect in devices without DDR.
- 7: These pins are restricted to input functions only.

TABLE 4-8: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS (CONTINUED)

Target Protection Number	Target Description (see Note 5)	SBTxREGy Register (see Note 7)							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
6	External Memory via EBI and EBI Module ⁽⁶⁾	SBT6REG0	R	0x20000000	R	64 MB	—	0	SBT6RD0	R/W ⁽¹⁾	SBT6WR0	R/W ⁽¹⁾
		SBT6REG2	R	0x1F8EC000	R	4 KB	0	1	SBT6RD2	R/W ⁽¹⁾	SBT6WR2	R/W ⁽¹⁾
7	System Controller	SBT7REG0	R	0x1F800000	R	—	—	0	SBT7RD0	R/W ⁽¹⁾	SBT7WR0	R/W ⁽¹⁾
	Flash Controller	SBT7REG1	R/W	R/W	R/W	R/W	—	3	SBT7RD1	R/W ⁽¹⁾	SBT7WR1	R/W ⁽¹⁾
	DMT/WDT CVREF PPS Input PPS Output Interrupts DMA	SBT7REG2	R/W	R/W	R/W	R/W	0	1	SBT7RD2	R/W ⁽¹⁾	SBT7WR2	R/W ⁽¹⁾
8	SPI1-SPI6	SBT8REG0	R	0x1F820000	R	64 KB	—	0	SBT8RD0	R/W ⁽¹⁾	SBT8WR0	R/W ⁽¹⁾
	I2C1-I2C5 UART1-UART6 PMP	SBT8REG1	R/W	R/W	R/W	R/W	—	3	SBT8RD1	R/W ⁽¹⁾	SBT8WR1	R/W ⁽¹⁾
9	Timer1-Timer9	SBT9REG0	R	0x1F840000	R	64 KB	—	0	SBT9RD0	R/W ⁽¹⁾	SBT9WR0	R/W ⁽¹⁾
	IC1-IC9 OC1-OC9 ADC Comparator 1 Comparator 2	SBT9REG1	R/W	R/W	R/W	R/W	—	3	SBT9RD1	R/W ⁽¹⁾	SBT9WR1	R/W ⁽¹⁾
10	PORTA-PORTK	SBT10REG0	R	0x1F860000	R	64 KB	—	0	SBT10RD0	R/W ⁽¹⁾	SBT10WR0	R/W ⁽¹⁾
		SBT10REG1	R/W	R/W	R/W	R/W	—	3	SBT10RD1	R/W ⁽¹⁾	SBT10WR1	R/W ⁽¹⁾
11	CAN1	SBT11REG0	R	0x1F880000	R	64 KB	—	0	SBT11RD0	R/W ⁽¹⁾	SBT11WR0	R/W ⁽¹⁾
	CAN2 Ethernet	SBT11REG1	R/W	R/W	R/W	R/W	—	3	SBT11RD1	R/W ⁽¹⁾	SBT11WR1	R/W ⁽¹⁾
12	GLCD	SBT12REG0	R	0x1F8EA000	R	4 KB	—	0	SBT12RD0	R/W ⁽¹⁾	SBT12WR0	R/W ⁽¹⁾
	GPU		R	0x1F8EB000	R	4 KB	—	0		R/W ⁽¹⁾		R/W ⁽¹⁾
	DDR2PHY		R	0x1F8E9000	R	4 KB	—	0		R/W ⁽¹⁾		R/W ⁽¹⁾
	DDR2SFR		R	0x1F8E8000	R	4 KB	—	0		R/W ⁽¹⁾		R/W ⁽¹⁾
13	External Memory via SQ1 and SQ11	SBT13REG0	R	0x30000000	R	64 MB	—	0	SBT13RD0	R/W ⁽¹⁾	SBT13WR0	R/W ⁽¹⁾
		SBT13REG1	R	0x1F8E2000	R	4 KB	—	3	SBT13RD1	R/W ⁽¹⁾	SBT13WR1	R/W ⁽¹⁾

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

- Note**
- Reset values for these bits are '0', '1', '1', '1', respectively.
 - The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.
 - The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)} \times 1024$ bytes. For read-only bits, this value is set by hardware on Reset.
 - Refer to the Device Memory Map (Figure 4-1) for specific device memory sizes and start addresses.
 - See Table 4-2 for information on specific target memory size and start addresses.
 - The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.
 - The 'x' in the SBTxREGy, SBTxRDy, and SBTxWRy registers represents the target protection number and not the actual target number (e.g., for SQ1 'x' = 13 and not 11, whereas 11 is the actual target number).

TABLE 4-18: SYSTEM BUS TARGET PROTECTION GROUP 8 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
8820	SBT8ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
8824	SBT8ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8828	SBT8ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT8ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT8ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT8REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8850	SBT8RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8858	SBT8WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8860	SBT8REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8870	SBT8RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8878	SBT8WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

TABLE 4-20: SYSTEM BUS TARGET PROTECTION GROUP 10 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
9020	SBT10ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
9024	SBT10ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000
9028	SBT10ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9030	SBT10ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9038	SBT10ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9040	SBT10REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9050	SBT10RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9058	SBT10WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9060	SBT10REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9070	SBT10RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9078	SBT10WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	NVMCON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	PFSWAP	BFSWAP	—	—	NVMOP<3:0>				0000
0610	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
0620	NVMADDR ⁽¹⁾	31:16	NVMADDR<31:0>																0000
		15:0																	0000
0630	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
0640	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
0650	NVMDATA2	31:16	NVMDATA2<31:0>																0000
		15:0																	0000
0660	NVMDATA3	31:16	NVMDATA3<31:0>																0000
		15:0																	0000
0670	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
0680	NVMPWP ⁽¹⁾	31:16	PWPLOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
0690	NVMBWP ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LBWPLOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPLOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF
06A0	NVMCON2 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00xx
		15:0	—	—	—	—	—	—	—	—	SWAPLOCK<1:0>			—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMTO	WDTO
23:16	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	SWNMI	—	—	—	GNMI	HLVD	CF	WDTS
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMTO:** Deadman Timer Time-out Flag bit

1 = DMT time-out has occurred and caused a NMI

0 = DMT time-out has not occurred

Setting this bit will cause a DMT NMI event, and NMICNT will begin counting.

bit 24 **WDTO:** Watchdog Timer Time-Out Flag bit

1 = WDT time-out has occurred and caused a NMI

0 = WDT time-out has not occurred

Setting this bit will cause a WDT NMI event, and NMICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger.

1 = An NMI will be generated

0 = An NMI will not be generated

bit 22-20 **Unimplemented:** Read as '0'

bit 19 **GNMI:** General NMI bit

1 = A general NMI event has been detected or a user-initiated NMI event has occurred

0 = A general NMI event has not been detected

Setting GNMI to a '1' causes a user-initiated NMI event. This bit is also set by writing 0x4E to the NMIKEY<7:0> (INTCON<31:24>) bits.

bit 18 **HLVD:** High/Low-Voltage Detect bit

1 = HLVD has detected a low-voltage condition and caused an NMI

0 = HLVD has not detected a low-voltage condition

bit 17 **CF:** Clock Fail Detect bit

1 = FSCM has detected clock failure and caused an NMI

0 = FSCM has not detected clock failure

Setting this bit will cause a CF NMI event, but will not cause a clock switch to the BFRC.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit

1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep

0 = WDT time-out has not occurred during Sleep mode

Setting this bit will cause a WDT NMI.

Note 1: If a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is cleared before this counter reaches '0', no device Reset is asserted. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the "PIC32 Family Reference Manual" for details.

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REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

bit 15-0 **NMICNT<15:0>**: NMI Reset Counter Value bits

These bits specify the reload value used by the NMI reset counter.

1111111111111111-0000000000000001 = Number of SYSCLK cycles before a device Reset occurs⁽¹⁾

0000000000000000 = No delay between NMI assertion and device Reset event

Note 1: If a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is cleared before this counter reaches '0', no device Reset is asserted. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit can be written. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the <i>"PIC32 Family Reference Manual"</i> for details.
--

13.2 Timer1 Control Register

TABLE 13-1: TIMER1 REGISTER MAP

Virtual Address (BF84_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>		TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

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NOTES:

18.1 Watchdog Timer Control Registers

TABLE 18-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
0800	WDTCON ⁽¹⁾	31:16	WDTCLRKEY<15:0>															0000
		15:0	ON	—	—	RUNDIV<4:0>				—	—	SLPDIV<4:0>				WDTWINEN	xxxx	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

TABLE 21-1: SPI1 THROUGH SPI6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
1600	SPI4CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1610	SPI4STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1620	SPI4BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1630	SPI4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	BRG<8:0>										0000
1640	SPI4CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000
1800	SPI5CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1810	SPI5STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1820	SPI5BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1830	SPI5BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	BRG<8:0>										0000
1840	SPI5CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000
1A00	SPI6CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1A10	SPI6STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1A20	SPI6BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1A30	SPI6BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	BRG<8:0>										0000
1A40	SPI6CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Graphics (DA) Family

REGISTER 22-6: SQI1CMDTHR: SQI COMMAND THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TXCMDTHR<5:0>					
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RXCMDTHR<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **TXCMDTHR<5:0>:** Transmit Command Threshold bits

In transmit initiation mode, the SQI module performs a transmit operation when transmit command threshold bytes are present in the TX buffer. These bits should usually be set to '1' for normal Flash commands, and set to a higher value for page programming. For 16-bit mode, the value should be a multiple of 2.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RXCMDTHR<5:0>:** Receive Command Threshold bits⁽¹⁾

In receive initiation mode, the SQI module attempts to perform receive operations to fetch the receive command threshold number of bytes in the receive buffer. If space for these bytes is not present in the buffer, the SQI will not initiate a transfer. For 16-bit mode, the value should be a multiple of 2.

If software performs any reads, thereby reducing the buffer count, hardware would initiate a receive transfer to make the buffer count equal to the value in these bits. If software would not like any more words latched into the buffer, command initiation mode needs to be changed to Idle before any buffer reads by software.

In the case of Boot/XIP mode, the SQI module will use the System Bus burst size, instead of the receive command threshold value.

Note 1: These bits should only be programmed when a receive is not active (i.e., during Idle mode or a transmit).

PIC32MZ Graphics (DA) Family

REGISTER 22-24: SQI1MEMSTAT: SQI MEMORY STATUS CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	R/W-0 STATPOS	R/W-0 STATTYPE<1:0>	R/W-0 STATBYTES<1:0>	R/W-0	R/W-0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATCMD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATCMD<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **STATPOS:** Status Bit Position in Flash bit

Indicates the BUSY bit position in the Flash Status register. This bit is added to support all Flash types (with BUSY bit at 0 and at 7).

1 = BUSY bit position is bit 7 in status register

0 = BUSY bit position is bit 0 in status register

bit 19-18 **STATTYPE<1:0>:** Status Command Lane Mode bits

11 = Reserved

10 = Status command and read are executed in Quad Lane mode

01 = Status command and read are executed in Dual Lane mode

00 = Status command and read are executed in Single Lane mode

bit 17-16 **STATBYTES<1:0>:** Number of Status Bytes bits

11 = Reserved

10 = Status command is 2 bytes long

01 = Status command is 1 byte long

00 = Reserved

bit 15-0 **STATCMD<15:0>:** Status Command bits

The status check command is written into these bits

PIC32MZ Graphics (DA) Family

FIGURE 27-11: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	23:16	ENCKEY<23:16>						
	15:8	ENCKEY<15:8>						
	7:0	ENCKEY<7:0>						
SA_ENCKEY3	31:24	ENCKEY<31:24>						
	23:16	ENCKEY<23:16>						
	15:8	ENCKEY<15:8>						
SA_ENCKEY4	7:0	ENCKEY<7:0>						
	31:24	ENCKEY<31:24>						
	23:16	ENCKEY<23:16>						
SA_ENCKEY5	15:8	ENCKEY<15:8>						
	7:0	ENCKEY<7:0>						
	31:24	ENCKEY<31:24>						
SA_ENCKEY6	23:16	ENCKEY<23:16>						
	15:8	ENCKEY<15:8>						
	7:0	ENCKEY<7:0>						
SA_ENCKEY7	31:24	ENCKEY<31:24>						
	23:16	ENCKEY<23:16>						
	15:8	ENCKEY<15:8>						
SA_ENCKEY8	7:0	ENCKEY<7:0>						
	31:24	ENCKEY<31:24>						
	23:16	ENCKEY<23:16>						
SA_AUTHIV1	15:8	ENCKEY<15:8>						
	7:0	ENCKEY<7:0>						
	31:24	AUTHIV<31:24>						
SA_AUTHIV2	23:16	AUTHIV<23:16>						
	15:8	AUTHIV<15:8>						
	7:0	AUTHIV<7:0>						
SA_AUTHIV3	31:24	AUTHIV<31:24>						
	23:16	AUTHIV<23:16>						
	15:8	AUTHIV<15:8>						
SA_AUTHIV4	7:0	AUTHIV<7:0>						
	31:24	AUTHIV<31:24>						
	23:16	AUTHIV<23:16>						
SA_AUTHIV5	15:8	AUTHIV<15:8>						
	7:0	AUTHIV<7:0>						
	31:24	AUTHIV<31:24>						
SA_AUTHIV6	23:16	AUTHIV<23:16>						
	15:8	AUTHIV<15:8>						
	7:0	AUTHIV<7:0>						
SA_AUTHIV7	31:24	AUTHIV<31:24>						
	23:16	AUTHIV<23:16>						
	15:8	AUTHIV<15:8>						
SA_AUTHIV8	7:0	AUTHIV<7:0>						
	31:24	AUTHIV<31:24>						
	23:16	AUTHIV<23:16>						
	15:8	AUTHIV<15:8>						
	7:0	AUTHIV<7:0>						

PIC32MZ Graphics (DA) Family

REGISTER 29-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

- bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled
- bit 5-6 **Unimplemented:** Read as '0'
- bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

PIC32MZ Graphics (DA) Family

REGISTER 31-23: EMAC1CFG1: ETHERNET CONTROLLER MAC CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	RW-1	RW-0	U-0	U-0	RW-0	RW-0	RW-0	RW-0
	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN
7:0	U-0	U-0	U-0	RW-0	RW-1	RW-1	RW-0	RW-1
	—	—	—	LOOPBACK	TX PAUSE	RX PAUSE	PASSALL	RX ENABLE

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SOFTRESET:** Soft Reset bit

Setting this bit will put the MACMII in reset. Its default value is '1'.

bit 14 **SIMRESET:** Simulation Reset bit

Setting this bit will cause a reset to the random number generator within the Transmit Function.

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMCS:** Reset MCS/RX bit

Setting this bit will put the MAC Control Sub-layer/Receive domain logic in reset.

bit 10 **RESETRFUN:** Reset RX Function bit

Setting this bit will put the MAC Receive function logic in reset.

bit 9 **RESETTMCS:** Reset MCS/TX bit

Setting this bit will put the MAC Control Sub-layer/TX domain logic in reset.

bit 8 **RESETTFUN:** Reset TX Function bit

Setting this bit will put the MAC Transmit function logic in reset.

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **LOOPBACK:** MAC Loopback mode bit

1 = MAC Transmit interface is loop backed to the MAC Receive interface

0 = MAC normal operation

bit 3 **TXPAUSE:** MAC TX Flow Control bit

1 = PAUSE Flow Control frames are allowed to be transmitted

0 = PAUSE Flow Control frames are blocked

bit 2 **RXPAUSE:** MAC RX Flow Control bit

1 = The MAC acts upon received PAUSE Flow Control frames

0 = Received PAUSE Flow Control frames are ignored

bit 1 **PASSALL:** MAC Pass all Receive Frames bit

1 = The MAC will accept all frames regardless of type (Normal vs. Control)

0 = The received Control frames are ignored

bit 0 **RXENABLE:** MAC Receive Enable bit

1 = Enable the MAC receiving of frames

0 = Disable the MAC receiving of frames

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MZ Graphics (DA) Family

REGISTER 31-32: EMAC1MCMD: ETHERNET CONTROLLER MAC MII MANAGEMENT COMMAND REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SCAN	READ

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-2 **Unimplemented:** Read as '0'

bit 1 **SCAN:** MII Management Scan Mode bit

1 = The MII Management module will perform read cycles continuously (for example, useful for monitoring the Link Fail)

0 = Normal Operation

bit 0 **READ:** MII Management Read Command bit

1 = The MII Management module will perform a single read cycle. The read data is returned in the EMAC1MRDD register

0 = The MII Management module will perform a write cycle. The write data is taken from the EMAC1MWTD register

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MZ Graphics (DA) Family

REGISTER 38-11: DDRREFCFG: DDR REFRESH CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0
	MAXREFS<2:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFDLY<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **MAXREFS<2:0>:** Maximum Pending Refreshes bits

These bits specify the maximum number of refreshes that may be pending at any time. If there is any idle time when one or more refreshes are pending, the pending refreshes are issued continuously until a new request is received. If there is no idle time while MAXREFS <2:0> refreshes are pending, subsequent requests are stopped until at least one burst of pending refreshes can be issued.

bit 23-16 **REFDLY<7:0>:** Minimum Refresh-to-Refresh Delay bits

These bits specify the minimum number of clocks required between refreshes.

bit 15-0 **REFCNT<15:0>:** Refresh Count bits

These bits specify the number of clock cycles corresponding to the average periodic refresh interval.

PIC32MZ Graphics (DA) Family

43.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

43.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

43.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

43.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

43.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDIOMIN and VDDIOMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

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