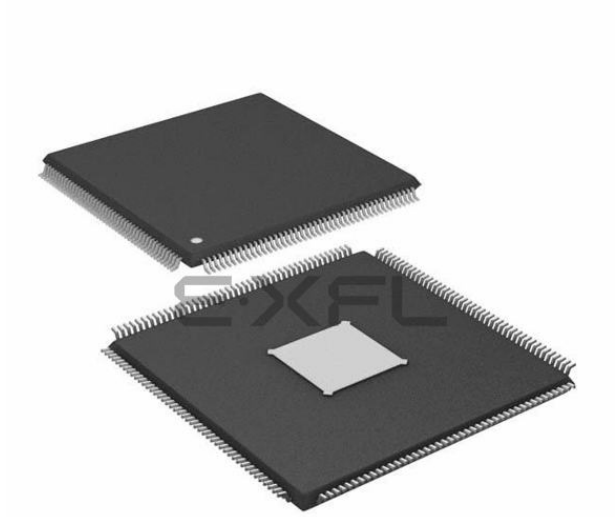

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Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025dag176t-i-2j

REGISTER 4-9: SBTxECLRS: SYSTEM BUS TARGET 'x' SINGLE ERROR CLEAR REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Single Error on Read bit
A single error as reported via SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-8 for the list of available targets and their descriptions.

REGISTER 4-10: SBTxECLRM: SYSTEM BUS TARGET 'x' MULTIPLE ERROR CLEAR REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Multiple Errors on Read bit
Multiple errors as reported via SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-8 for the list of available targets and their descriptions.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits

111 = System PLL (SPLL)
110 = Reserved
101 = Internal Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Reserved
010 = Primary Oscillator (POSC) (HS or EC)
001 = System PLL (SPLL)
000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit

1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit

1 = Device will enter Sleep mode when a WAIT instruction is executed
0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit

1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit

1 = Enable Secondary Oscillator
0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit**(1)**

1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note:	Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPIGN<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
	CHBUSY	—	CHIPGNEN	—	CHPATLEN	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **CHPIGN<7:0>:** Channel Register Data bits
Pattern Terminate mode:
Any byte matching these bits during a pattern match may be ignored during the pattern match determination when the CHPIGNEN bit is set. If a byte is read that is identical to this data byte, the pattern match logic will treat it as a "don't care" when the pattern matching logic is enabled and the CHPIGEN bit is set.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CHPIGNEN:** Enable Pattern Ignore Byte bit
1 = Treat any byte that matches the CHPIGN<7:0> bits as a "don't care" when pattern matching is enabled
0 = Disable this feature

bit 12 **Unimplemented:** Read as '0'

bit 11 **CHPATLEN:** Pattern Length bit
1 = 2 byte length
0 = 1 byte length

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit 5 **CHCHN:** Channel Chain Enable bit
1 = Allow channel to be chained
0 = Do not allow channel to be chained

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
- 1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
- 0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
- 1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
- 0 = No interrupt is pending

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF
15:8	R/W-0	R/W-0	R/W-1	R-0, HS	R-0	R/W-0	R-0, HC	R/W-0
	ISOUPD	SOFTCONN	HSEN	HSMODE	RESET	RESUME	SUSPMODE	SUSPEN
	—	—						
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	FUNC<6:0>						
		—	—	—	—	—	—	—

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIF:EP1TXIF:** Endpoint 'n' TX Interrupt Flag bit
1 = Endpoint has a transmit interrupt to be serviced
0 = No interrupt event

bit 16 **EP0IF:** Endpoint 0 Interrupt bit
1 = Endpoint 0 has an interrupt to be serviced
0 = No interrupt event

All EPxTX and EP0 bits are cleared when the byte is read. Therefore, these bits must be read independently from the remaining bits in this register to avoid accidental clearing.

bit 15 **ISOUPD:** ISO Update bit (*Device mode only; unimplemented in Host mode*)
1 = USB module will wait for a SOF token from the time TXPKTRDY is set before sending the packet
0 = No change in behavior

This bit only affects endpoints performing isochronous transfers when in *Device mode*. This bit is unimplemented in *Host mode*.

bit 14 **SOFTCONN:** Soft Connect/Disconnect Feature Selection bit
1 = The USB D+/D- lines are enabled and active
0 = The USB D+/D- lines are disabled and are tri-stated

This bit is only available in *Device mode*.

bit 13 **HSEN:** Hi-Speed Enable bit
1 = The USB module will negotiate for Hi-Speed mode when the device is reset by the hub
0 = Module only operates in Full-Speed mode

bit 12 **HSMODE:** Hi-Speed Mode Status bit
1 = Hi-Speed mode successfully negotiated during USB reset
0 = Module is not in Hi-Speed mode

In *Device mode*, this bit becomes valid when a USB reset completes. In *Host mode*, it becomes valid when the RESET bit is cleared.

bit 11 **RESET:** Module Reset Status bit
1 = Reset signaling is present on the bus
0 = Normal module operation

In *Device mode*, this bit is read-only. In *Host mode*, this bit is read/write.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 26 **DATATWEN:** Data Toggle Write Enable Control bit (*Host mode*)
1 = DATATGGL can be written
0 = DATATGGL is not writable

bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)
When read, this bit indicates the current state of the endpoint data toggle.
If DATATWEN = 1, this bit may be written with the required setting of the data toggle.
If DATATWEN = 0, any value written to this bit is ignored.

bit 24 **INCOMPRX:** Incomplete Packet Status bit
1 = The packet in the RX FIFO during a high-bandwidth Isochronous/Interrupt transfer is incomplete because parts of the data were not received
0 = Written by then software to clear this bit
In anything other than Isochronous transfer, this bit will always return 0.

bit 23 **CLRDT:** Clear Data Toggle Control bit
1 = Reset the endpoint data toggle to 0
0 = Leave endpoint data toggle alone

bit 22 **SENTSTALL:** STALL Handshake Status bit (*Device mode*)
1 = STALL handshake is transmitted
0 = Written by the software to clear this bit

RXSTALL: STALL Handshake Receive Status bit (*Host mode*)
1 = A STALL handshake has been received. An interrupt is generated.
0 = Written by the software to clear this bit

bit 21 **SENDSTALL:** STALL Handshake Control bit (*Device mode*)
1 = Issue a STALL handshake
0 = Terminate stall condition

REQPKT: IN Transaction Request Control bit (*Host mode*)
1 = Request an IN transaction.
0 = No request
This bit is cleared when RXPKTRDY is set.

bit 20 **FLUSH:** Flush FIFO Control bit
1 = Flush the next packet to be read from the endpoint RX FIFO. The FIFO pointer is reset and the RXPKTRDY bit is cleared. This should only be used when RXPKTRDY is set. If the FIFO is double-buffered, FLUSH may need to be set twice to completely clear the FIFO.
0 = Normal FIFO operation
This bit is automatically cleared.

bit 19 **DATAERR:** Data Packet Error Status bit (*Device mode*)
1 = The data packet has a CRC or bit-stuff error.
0 = No data error
This bit is cleared when RXPKTRDY is cleared. This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

DERRNAKT: Data Error/NAK Time-out Status bit (*Host mode*)
1 = The data packet has a CRC or bit-stuff error. In Bulk mode, the RX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK limit.
0 = No data or NAK time-out error

TABLE 12-8: PORTF REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0500	ANSELF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSF13	ANSF12	—	—	—	—	—	—	—	—	—	—	—	—	3000
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPUF13	CNPUF12	—	—	—	CNPUF8	—	—	CNPUF5	CNPUF4	CNPUF3	CNPUF2	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPDF13	CNPDF12	—	—	—	CNPDF8	—	—	CNPDF5	CNPDF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNIEF13	CNIEF12	—	—	—	CNIEF8	—	—	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CN STATF13	CN STATF12	—	—	—	CN STATF8	—	—	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	0000
05A0	CNNEF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNNEF13	CNNEF12	—	—	—	CNNEF8	—	—	CNNEF5	CNNEF4	CNNEF3	CNNEF2	CNNEF1	CNNEF0	0000
05B0	CNFF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNFF13	CNFF12	—	—	—	CNFF8	—	—	CNFF5	CNFF4	CNFF3	CNFF2	CNFF1	CNFF0	0000
05C0	SRCON0F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SR1F13	SR1F12	—	—	—	SR1F8	—	—	SR1F5	SR1F4	SR1F3	SR1F2	SR1F1	SR1F0	0000
05D0	SRCON1F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SR0F13	SR0F12	—	—	—	SR0F8	—	—	SR0F5	SR0F4	SR0F3	SR0F2	SR0F1	SR0F0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 16-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT(1)	OCTSEL(2)	OCM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit
- 1 = Output Compare peripheral is enabled
- 0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when CPU enters Idle mode
- 0 = Continue operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisions to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(1)
- 1 = PWM Fault condition has occurred (cleared in HW only)
- 0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit(2)
- 1 = Timery is the clock source for this Output Compare module
- 0 = Timerx is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

Note 1: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

2: Refer to Table 16-1 for Timerx and Timery selections.

20.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

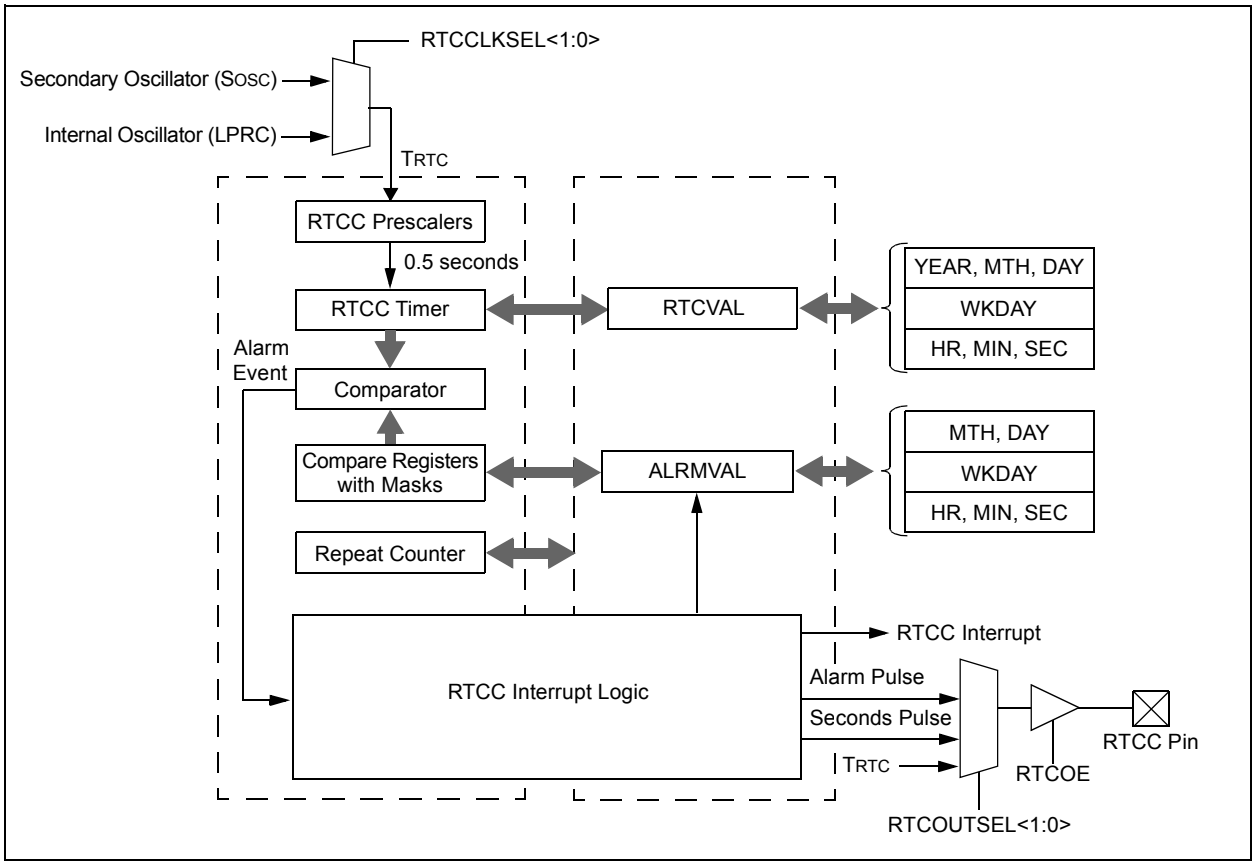
The RTCC module can operate in VBAT mode when there is a power loss on the VDDIO pin. The RTCC will continue to operate if the VBAT pin is powered on (it is usually connected to the battery).

Key features of the RTCC module include:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external crystal or internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

Note: RTCC pin function is not available during VBAT operation.

FIGURE 20-1: RTCC BLOCK DIAGRAM



REGISTER 20-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **HR10<3:0>:** Binary Coded Decimal value of hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary Coded Decimal value of minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary Coded Decimal value of seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B0AC	ADCCMPCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B0	ADCCMPCON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B4	ADCCMPCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B8	ADCFSTAT	31:16	FEN	—	—	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	FIEN	FRDY	FWROVERR	—	—	—	—	—	0000
		15:0	FCNT<7:0>								FSIGN	—	—	—	—	ADCID<2:0>			0000
B0BC	ADCFIFO	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B0C0	ADCBASE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADCBASE<15:0>																0000
B0D0	ADCTRGSNS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LVL11	LVL10	LVL9	LVL8	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	0000
B0D4	ADC0TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0D8	ADC1TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0DC	ADC2TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0E0	ADC3TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0E4	ADC4TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0F0	ADCEIEN1	31:16	EIEN31	EIEN30	EIEN29	EIEN28	EIEN27	EIEN26	EIEN25	EIEN24	EIEN23	EIEN22	EIEN21	EIEN20	EIEN19	EIEN18	EIEN17	EIEN16	0000
		15:0	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0	0000
B0F4	ADCEIEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	EIEN43	EIEN42	EIEN41	EIEN40	EIEN39	EIEN38	EIEN37	EIEN36	EIEN35	EIEN34	EIEN33	EIEN32	0000
B0F8	ADCEISTAT1	31:16	EIRDY31	EIRDY30	EIRDY29	EIRDY28	EIRDY27	EIRDY26	EIRDY25	EIRDY24	EIRDY23	EIRDY22	EIRDY21	EIRDY20	EIRDY19	EIRDY18	EIRDY17	EIRDY16	0000
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000
B0FC	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	EIRDY43	EIRDY42	EIRDY41	EIRDY40	EIRDY39	EIRDY38	EIRDY37	EIRDY36	EIRDY35	EIRDY34	EIRDY33	EIRDY32	0000
B100	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>				WKIEN7	—	—	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	—	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	—	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000
B600	ADC0CFG(1)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B604	ADC1CFG1)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 29-24: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Unimplemented:** Read as '0'

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

REGISTER 31-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **PMCS<15:8>:** Pattern Match Checksum 1 bits

bit 7-0 **PMCS<7:0>:** Pattern Match Checksum 0 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 31-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PMO<15:0>:** Pattern Match Offset 1 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 38-13: DDRDLYCFG0: DDR DELAY CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RMWDLY<3:0>				R2WDLY<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2WCSDLY<3:0>				W2WDLY<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	R2RCSDLY<3:0>				R2RDLY<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2RCSDLY<3:0>				W2RDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **RMWDLY<3:0>:** Read-Modify-Write Delay bits

These bits specify the minimum number of clocks required between the read and write commands issued for a read-modify-write operation.

bit 27-24 **R2WDLY<3:0>:** Read-to-Write Delay bits

These bits specify the minimum number of clocks required between a read command and write command. Commands may be to the same or different Chip Selects.

bit 23-20 **W2WCSDLY<3:0>:** Write-to-Write Chip Select Delay bits

These bits specify the minimum number of clocks required between two write commands to different Chip Selects.

bit 19-16 **W2WDLY<3:0>:** Write-to-Write Delay bits

These bits specify the minimum number of clocks required between two write commands to the same Chip Select.

bit 15-12 **R2RCSDLY<3:0>:** Read-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between two read commands to different Chip Selects.

bit 11-8 **R2RDLY<3:0>:** Read-to-Read Delay bits

These bits specify the minimum number of clocks required between two read commands to the same Chip Select.

bit 7-4 **W2RCSDLY<3:0>:** Write-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between a write command and a read command to different Chip Selects.

bit 3-0 **W2RDLY<3:0>:** Write-to-Read Delay bits

These bits specify the minimum number of clocks required between a write command and a read command to the same Chip Select.

REGISTER 38-20: DDRODTENCFG: DDR ON-DIE TERMINATION ENABLE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ODTWEN
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ODTREN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-17 **Unimplemented:** Read as '0'

bit 16 **ODTWEN:** On-Die Termination Write Enable bit

1 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT enabled for data reads

0 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT disabled for data reads

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ODTREN:** On-Die Termination Read Enable bit

1 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT enabled for data writes

0 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT disabled for data writes

REGISTER 39-10: SDHCINTEN: SDHC INTERRUPT FLAG ENABLE REGISTER (CONTINUED)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CARDIE:** Card Interrupt Flag Enable bit
1 = Card interrupt flag is enabled
0 = Card interrupt flag is masked

bit 7 **CARDRIE:** Card Removal Interrupt Flag Enable bit
1 = Card removal interrupt flag is enabled
0 = Card removal interrupt flag is masked

bit 6 **CARDIIE:** Card Insertion Interrupt Flag Enable bit
1 = Card insertion interrupt flag is enabled
0 = Card insertion interrupt flag is masked

bit 5 **BRRDYIE:** Buffer Read Ready Interrupt Flag Enable bit
1 = Buffer read ready interrupt flag is enabled
0 = Buffer read ready interrupt flag is masked

bit 4 **BWRDYIE:** Buffer Write Ready Interrupt Flag Enable bit
1 = Buffer write ready interrupt flag is enabled
0 = Buffer write ready interrupt flag is masked

bit 3 **DMAIE:** DMA Interrupt Flag Enable bit
1 = DMA interrupt flag is enabled
0 = DMA interrupt flag is masked

bit 2 **BGIE:** Block Gap Interrupt Flag Enable bit
1 = Block gap event interrupt flag is enabled
0 = Block gap event interrupt flag is masked

bit 1 **TXEIE:** Transfer Complete Interrupt Flag Enable bit
1 = Transfer complete interrupt flag is enabled
0 = Transfer complete interrupt flag is masked

bit 0 **CEIE:** Command Complete Interrupt Flag Enable bit
1 = Command complete interrupt flag is enabled
0 = Command complete interrupt flag is masked

40.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MZ DA devices include two features to prevent alterations to enabled or disabled peripherals:

- Control Register Lock Sequence
- Configuration Bit Select Lock

40.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting the PMDLOCK bit prevents writes to the control registers and clearing the PMDLOCK bit allows writes.

To set or clear the PMDLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

40.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If the PMDLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

TABLE 44-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO10	VOL	**Output Low Voltage** I/O Pins 4x Sink Driver Pins - RA0-RA3, RA9, RA10, RA14, RA15 RB0, RB4, RB6, RB7, RB10, RB11, RB12, RB14 RC12-RC15 RD6, RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8, RF12 RG15 RH0, RH1, RH4-RH14 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	0.4	V	I_{OL} ≤ 10 mA, V_{DDIO} = 3.3V
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA4, RA5 RB2, RB3, RB5, RB8, RB9, RB13, RB14, RB15 RC1-RC4 RD0-RD3, RD9, RD10, RD12, RD13 RE0-RE7 RF0, RF1, RF4, RF5, RF13 RG0, RG1, RG6, RG7, RG8, RG9 RH2, RH3, RH7, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	0.4	V	I_{OL} ≤ 15 mA, V_{DDIO} = 3.3V
		Output Low Voltage I/O Pins: 12x Sink Driver Pins - RA6, RA7 RD4, RD5 RG12-RG14	—	—	0.4	V	I_{OL} ≤ 20 mA, V_{DDIO} = 3.3V

Note 1: Parameters are characterized, but not tested.

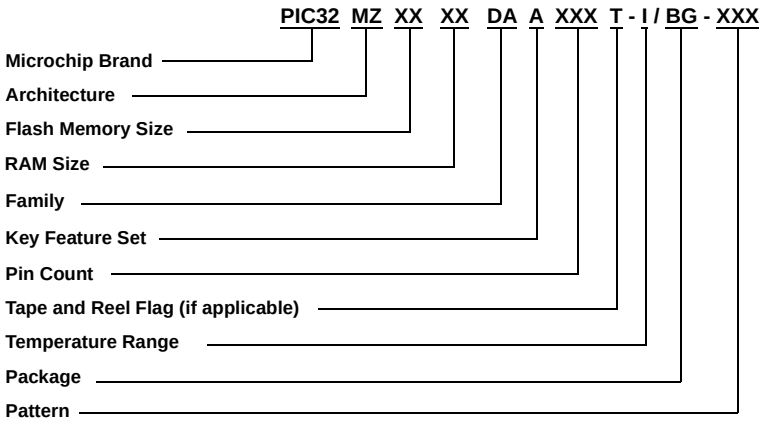
TABLE 44-48: TEMPERATURE SENSOR SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TS10	VTS	Rate of Change	—	5	—	mV/ºC	—
TS11	TR	Resolution	-2	—	+2	ºC	—
TS12	IVTEMP	Voltage Range	0.5	—	1.5	V	—
TS13	TMIN	Minimum Temperature	—	-40	—	ºC	IVTEMP = 0.5V
TS14	TMAX	Maximum Temperature	—	160	—	ºC	IVTEMP = 1.5V

Note 1: The temperature sensor is functional at VBORIOMIN < VDDIO < VDDIOMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

PIC32MZ0512DAA176-I/2J: Graphics MCU Family, PIC32, MIPS32® microAptiv™ MPU core, 512 KB program memory, 176-pin, Industrial temperature, LQFP package.

Flash Memory Family

Architecture	MZ	= MIPS32® microAptiv™ MPU Core
Flash Memory Size	10	= 1024 KB
	20	= 2048 KB
RAM Size	25	= 256 KB
	64	= 640 KB
Family	DA	= Graphics MCU Family
Key Feature	A	= PIC32 DA Family Features, no Crypto, no DDR memory
	B	= PIC32 DA Family Features, with Crypto, no DDR memory
	G	= PIC32 DA Family Features, no Crypto, with DDR memory
	H	= PIC32 DA Family Features, with Crypto, with DDR memory
Pin Count	169	= 169-pin
	176	= 176-pin
	288	= 288-pin
Temperature Range	I	= -40°C to +85°C (Industrial)
Package	HF	= 169-Lead (11x11x1.4 mm) LFBGA (Low Profile Fine Pitch Ball Grid Array)
	6J	= 169-Lead (11x11x1.56 mm) LFBGA (Low Profile Fine Pitch Ball Grid Array)
	2J	= 176-Lead (22x22x1.4 mm) LQFP (Low Profile Quad Flat Pack)
	4J	= 288-Lead (15x15x1.4 mm) LFBGA (Low Profile Fine Pitch Ball Grid Array)
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample