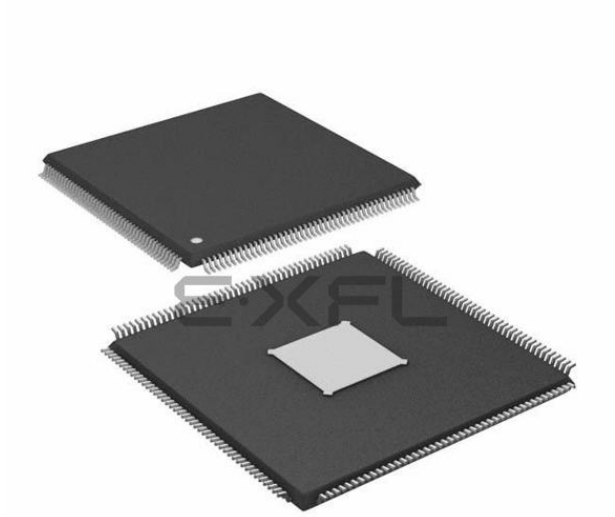
Microchip Technology - PIC32MZ2025DAH176T-I/2J Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2025dah176t-i-2j

TABLE 6: PIN NAMES FOR 176-PIN DEVICES

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAA176
PIC32MZ1025DAB176
PIC32MZ1064DAA176
PIC32MZ1064DAB176
PIC32MZ2025DAA176
PIC32MZ2025DAB176
PIC32MZ2064DAA176
PIC32MZ2064DAB176
PIC32MZ1025DAG176
PIC32MZ1025DAH176
PIC32MZ1064DAG176
PIC32MZ1064DAH176
PIC32MZ2025DAG176
PIC32MZ2025DAH176
PIC32MZ2064DAG176
PIC32MZ2064DAH176

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1

Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	VREF-/CVREF-/AN27/RA9	37	VSS
2	VREF+/CVREF+/AN28/RA10	38	VDDIO
3	AVDD	39	VDDCORE
4	AVDD	40	EBID0/PMD0/RE0
5	AVSS	41	RPF2/SDA3/RF2
6	AVSS	42	INT0/RH14
7	AN3/C2INA/RPB15/OCFB/RB15	43	EBID4/AN18/PMD4/RE4
8	AN8/RPB3/RB3	44	No Connect
9	AN48/CTPLS/RB13	45	VBUS
10	EBID10/AN4/RPB8/PMD10/RB8	46	VUSB3V3
11	PGEC1/AN9/RPB1/CTED1/RB1	47	VUSB3V3
12	AN49/RB11	48	VSS
13	PGEC2/RPB6/RB6	49	VSS
14	EBID12/AN10/RPC2/PMD12/RC2	50	D-
15	EBIWE/AN34/RPC3/PMWR/RC3	51	D+
16	EBIOE/AN19/RPC4/PMRD/RC4	52	USBID
17	EBID5/AN12/RPC1/PMD5/RC1	53	TMS/SDCD/RA0
18	VDDCORE	54	TRCLK/SDCK/SQICLK/RA6
19	VDDIO	55	TRD3/SDDATA3/SQID3/RA7
20	No Connect	56	TRD1/SDDATA1/SQID1/RG12
21	VSS	57	VDDR1V8(5)
22	VSS	58	VDDR1V8(5)
23	EBID6/AN16/PMD6/RE6	59	VDDR1V8(5)
24	EBID7/AN15/PMD7/RE7	60	VDDR1V8(5)
25	AN25/RPE8/RE8	61	VDDR1V8(5)
26	AN26/RPE9/RE9	62	VDDR1V8(5)
27	TDO/AN31/RPF12/RF12	63	VDDR1V8(5)
28	TDI/AN17/SCK5/RF13	64	TRD0/SDDATA0/SQID0/RG13
29	VSS	65	TRD2/SDDATA2/SQID2/RG14
30	AN14/C1IND/SCK2/RG6	66	DDRVREF(6)
31	AN13/C1INC/RPG7/SDA4/RG7	67	VDDR1V8(5)
32	AN30/C2IND/RPG8/SCL4/RG8	68	VDDR1V8(5)
33	EBIA2/AN23/C2INC/RPG9/PMA2/RG9	69	EBIA6/RPE5/PMA6/RE5
34	AN21/RG15	70	SDCMD/SQICS0/RPD4/RD4
35	AN20/RH4	71	SQICS1/RPD5/RD5
36	EBID1/AN39/PMD1/RE1	72	VDDR1V8(5)

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to VSS1V8 and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a No Connect in devices without DDR.
7: These pins are restricted to input functions only.

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TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
External Bus Interface						
EBIA0	H13	142	N17	O	—	External Bus Interface Address Bus
EBIA1	J11	136	R18	O	—	
EBIA2	C5	33	B9	O	—	
EBIA3	H11	135	R17	O	—	
EBIA4	J12	139	N15	O	—	
EBIA5	A11	174	B18	O	—	
EBIA6	F3	69	K3	O	—	
EBIA7	B12	173	E16	O	—	
EBIA8	N2	96	V9	O	—	
EBIA9	M2	95	T8	O	—	
EBIA10	K3	90	U7	O	—	
EBIA11	L1	91	V7	O	—	
EBIA12	J1	80	U5	O	—	
EBIA13	J2	81	N4	O	—	
EBIA14	G2	74	R6	O	—	
EBIA15	G3	75	T6	O	—	
EBIA16	K12	137	P16	O	—	
EBIA17	L13	134	R16	O	—	
EBIA18	H10	133	P15	O	—	
EBIA19	J10	132	R15	O	—	
EBIA20	M13	131	T18	O	—	
EBIA21	M12	130	T17	O	—	
EBIA22	E8	151	K17	O	—	
EBIA23	L2	92	V8	O	—	
EBID0	C4	40	B7	I/O	ST	External Bus Interface Data I/O Bus
EBID1	A4	40	D8	I/O	ST	
EBID2	N3	36	V10	I/O	ST	
EBID3	M3	99	T9	I/O	ST	
EBID4	B3	98	B6	I/O	ST	
EBID5	B7	43	A12	I/O	ST	
EBID6	F6	17	C11	I/O	ST	
EBID7	C7	23	B11	I/O	ST	
EBID8	K2	24	T7	I/O	ST	
EBID9	L3	89	U9	I/O	ST	
EBID10	A9	97	A15	I/O	ST	
EBID11	G10	10	N18	I/O	ST	
EBID12	A8	143	C13	I/O	ST	
EBID13	G12	14	M16	I/O	ST	
EBID14	L11	144	V17	I/O	ST	
EBID15	H1	127	U6	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-16: ETHERNET MII I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Ethernet						
ERXD0	N7	108	U12	I	ST	Ethernet Receive Data 0
ERXD1	M4	100	U10	I	ST	Ethernet Receive Data 1
ERXD2	N4	101	T10	I	ST	Ethernet Receive Data 2
ERXD3	N6	107	V12	I	ST	Ethernet Receive Data 3
ERXERR	M1	93	U8	I	ST	Ethernet Receive Error Input
ERXDV	M5	104	V11	I	ST	Ethernet Receive Data Valid
ERXCLK	N8	111	U13	I	ST	Ethernet Receive Clock
ETXD0	N9	113	V14	O	—	Ethernet Transmit Data 0
ETXD1	M9	112	T13	O	—	Ethernet Transmit Data 1
ETXD2	M8	110	V13	O	—	Ethernet Transmit Data 2
ETXD3	M7	109	T12	O	—	Ethernet Transmit Data 3
ETXERR	L10	118	V15	O	—	Ethernet Transmit Error
ETXEN	K11	121	V16	O	—	Ethernet Transmit Enable
ETXCLK	M10	120	T15	I	ST	Ethernet Transmit Clock
ECOL	M6	106	T11	I	ST	Ethernet Collision Detect
ECRS	N5	105	U11	I	ST	Ethernet Carrier Sense
EMDC	N10	119	U15	O	—	Ethernet Management Data Clock
EMDIO	K10	114	U14	I/O	—	Ethernet Management Data

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-17: ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Ethernet MII Interface						
ERXD0	N7	108	U12	I	ST	Ethernet Receive Data 0
ERXD1	M4	100	U10	I	ST	Ethernet Receive Data 1
ERXERR	M1	93	U8	I	ST	Ethernet Receive Error Input
ETXD0	N9	113	V14	O	—	Ethernet Transmit Data 0
ETXD1	M9	112	T13	O	—	Ethernet Transmit Data 1
ETXEN	K11	121	V16	O	—	Ethernet Transmit Enable
EMDC	N10	119	U15	O	—	Ethernet Management Data Clock
EMDIO	K10	114	U14	I/O	—	Ethernet Management Data
EREFCLK	N8	111	U13	I	ST	Ethernet Reference Clock
ECRSDV	M5	104	V11	I	ST	Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1240	RCON	31:16	—	—	HVD1V8R	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	VBPOR	VBAT	C802
		15:0	—	—	—	—	—	DPSLP	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0003
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	GNMI	HLVD	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Sub-priority bits
- 11 = Interrupt sub-priority is 3
- 10 = Interrupt sub-priority is 2
- 01 = Interrupt sub-priority is 1
- 00 = Interrupt subdirectory is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Sub-priority bits
- 11 = Interrupt sub-priority is 3
- 10 = Interrupt sub-priority is 2
- 01 = Interrupt sub-priority is 1
- 00 = Interrupt sub-priority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

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REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

bit 10-8 **PLLIDIV<2:0>:** System PLL Input Clock Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

The default setting is specified by the FPLLIDIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information. If the PLLICLK is set for FRC, this setting is ignored by the PLL and the divider is set to Divide-by-1.

bit 7 **PLLICLK:** System PLL Input Clock Source bit

1 = FRC is selected as the input to the System PLL
0 = POSC is selected as the input to the System PLL
The POR default is specified by the FPLLICLK Configuration bit in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

bit 6-3 **Unimplemented:** Read as '0'

bit 2-0 **PLLRANGE<2:0>:** System PLL Frequency Range Selection bits

111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

The default setting is specified by the FPLLRNG<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

REGISTER 8-6: PBxDIV: PERIPHERAL BUS 'x' CLOCK DIVISOR CONTROL REGISTER ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	R-1	U-0	U-0	U-0
	ON(1)	—	—	—	PBDIVRDY	—	—	—
7:0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	PBDIV<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Peripheral Bus 'x' Output Clock Enable bit(1)
- 1 = Output clock is enabled
- 0 = Output clock is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **PBDIVRDY:** Peripheral Bus 'x' Clock Divisor Ready bit
- 1 = Clock divisor logic is not switching divisors and the PBxDIV<6:0> bits may be written
- 0 = Clock divisor logic is currently switching values and the PBxDIV<6:0> bits cannot be written

bit 10-7 **Unimplemented:** Read as '0'

bit 6-0 **PBDIV<6:0>:** Peripheral Bus 'x' Clock Divisor Control bits
- 1111111 = PBCLKx is SYSCLK divided by 128
- 1111110 = PBCLKx is SYSCLK divided by 127
- •
- •
- •
- 0000011 = PBCLKx is SYSCLK divided by 4
- 0000010 = PBCLKx is SYSCLK divided by 3
- 0000001 = PBCLKx is SYSCLK divided by 2 (default value for x < 7)
- 0000000 = PBCLKx is SYSCLK divided by 1 (default value for x ≥ 7)

Note 1: The clock for peripheral bus 1 cannot be turned off. Therefore, the ON bit in the PB1DIV register cannot be written as a '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

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11.0 HI-SPEED USB WITH ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MZ DA family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 51. "Hi-Speed USB with On-The-Go (OTG)"** (DS60001326) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 embedded host, device, or OTG implementation with a minimum of external components.

The module supports Hi-Speed, Full-Speed, or Low-Speed in any of the operating modes. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the RAM controller, packet encode/decode, UTM synchronization, endpoint control, a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is illustrated in Figure 11-1.

The USB module includes the following features:

- USB Hi-Speed, Full-Speed, and Low-Speed support for host and device
- USB OTG support with one or more Hi-Speed, Full-Speed, or Low-Speed device
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Integrated 8-channel DMA to access system RAM and Flash
- Seven transmit endpoints and seven receive endpoints, in addition to Endpoint 0
- Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) support
- Suspend and resume signaling support
- Dynamic FIFO sizing
- Integrated RAM for the FIFOs, eliminating the need for system RAM for the FIFOs
- Link power management support

Note 1: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

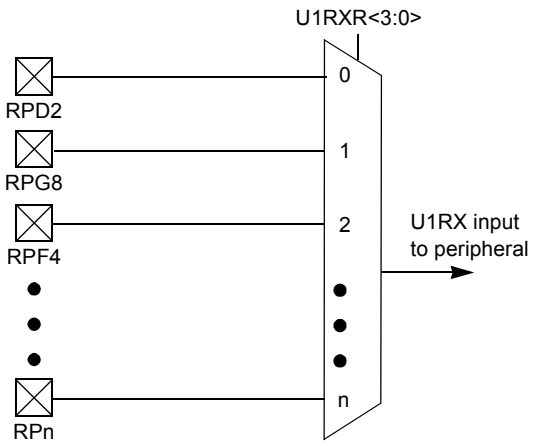
2: If the USB module is used, the Primary Oscillator (POSC) is limited to either 12 MHz or 24 MHz.

12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-1, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-1.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

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REGISTER 23-2: I2CxSTAT: I^2C STATUS REGISTER (CONTINUED)

bit 5 **D_A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^2C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

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FIGURE 27-11: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY3	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY4	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY5	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY6	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY7	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY8	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_AUTHIV1	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV2	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV3	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV4	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV5	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV6	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV7	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV8	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							

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REGISTER 29-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

bit 25-16 **SAMC<9:0>:** Sample Time for the Shared ADC (ADC7) bits

1111111111 = 1025 TAD7
•
•
•
0000000001 = 3 TAD7
0000000000 = 2 TAD7

Where TAD7 = period of the ADC conversion clock for the Shared ADC (ADC7) controlled by the ADCDIV<6:0> bits.

Note: Unlike the high-speed Class 1 ADC modules, the trigger event for the shared Class-3 ADC7 module initiates the SAMC sampling sequence, rather than the convert sequence.

Shared ADC7 Throughput rate:

=((1/((Sample time + Conversion time) (TAD))) / #of ADC inputs used in scan list)

=((1/((SAMC + # bit resolution +1)(TAD))) / #of ADC inputs used in scan list)

For example:

SCAN mode enabled with (2) ANx inputs in scan list (i.e., ADCCSSx<CSSY>), SAMC = 4

TAD, 12-bit mode, TAD = 20ns = 50 MHz

Throughput rate = ((1/ ((4+13)(20ns))) / 2)

= ((1/ (17 * 20ns)) / 2)

= 1,470588 msps

bit 15 **BGVRIEN:** Band Gap/VREF Voltage Ready Interrupt Enable bit

1 = Interrupt will be generated when the BGVRDDY bit is set
0 = No interrupt is generated when the BGVRRDY bit is set

bit 14 **REFFLTIEN:** Band Gap/VREF Voltage Fault Interrupt Enable bit

1 = Interrupt will be generated when the REFFLT bit is set
0 = No interrupt is generated when the REFFLT bit is set

bit 13 **EOSIEN:** End of Scan Interrupt Enable bit

1 = Interrupt will be generated when EOSRDY bit is set
0 = No interrupt is generated when the EOSRDY bit is set

bit 12 **ADCEIOVR:** Early Interrupt Request Override bit

1 = Early interrupt generation is not overridden and interrupt generation is controlled by the ADCEIEN1 and ADCEIEN2 registers
0 = Early interrupt generation is overridden and interrupt generation is controlled by the ADCGIRQEN1 and ADCGIRQEN2 registers

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **ADCEIS<2:0>:** Shared ADC (ADC7) Early Interrupt Select bits

These bits select the number of clocks (TAD7) prior to the arrival of valid data that the associated interrupt is generated.

111 = The data ready interrupt is generated 8 ADC clocks prior to end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to end of conversion
•
•
•
001 = The data ready interrupt is generated 2 ADC module clocks prior to end of conversion
000 = The data ready interrupt is generated 1 ADC module clock prior to end of conversion

Note: All options are available when the selected resolution, set by the SELRES<1:0> bits (ADCCON1<22:21>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.

bit 7 **Unimplemented:** Read as '0'

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REGISTER 29-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3 (CONTINUED)

bit 13 **DIFF38:** AN38 Mode bit
1 = AN38 is using Differential mode
0 = AN38 is using Single-ended mode

bit 12 **SIGN38:** AN38 Signed Data Mode bit
1 = AN38 is using Signed Data mode
0 = AN38 is using Unsigned Data mode

bit 11 **DIFF37:** AN37 Mode bit
1 = AN37 is using Differential mode
0 = AN37 is using Single-ended mode

bit 10 **SIGN37:** AN37 Signed Data Mode bit
1 = AN37 is using Signed Data mode
0 = AN37 is using Unsigned Data mode

bit 9 **DIFF36:** AN36 Mode bit
1 = AN36 is using Differential mode
0 = AN36 is using Single-ended mode

bit 8 **SIGN36:** AN36 Signed Data Mode bit
1 = AN36 is using Signed Data mode
0 = AN36 is using Unsigned Data mode

bit 7 **DIFF35:** AN35 Mode bit
1 = AN35 is using Differential mode
0 = AN35 is using Single-ended mode

bit 6 **SIGN35:** AN35 Signed Data Mode bit
1 = AN35 is using Signed Data mode
0 = AN35 is using Unsigned Data mode

bit 5 **DIFF34:** AN34 Mode bit
1 = AN34 is using Differential mode
0 = AN34 is using Single-ended mode

bit 4 **SIGN34:** AN34 Signed Data Mode bit
1 = AN34 is using Signed Data mode
0 = AN34 is using Unsigned Data mode

bit 3 **DIFF33:** AN33 Mode bit
1 = AN33 is using Differential mode
0 = AN33 is using Single-ended mode

bit 2 **SIGN33:** AN33 Signed Data Mode bit
1 = AN33 is using Signed Data mode
0 = AN33 is using Unsigned Data mode

bit 1 **DIFF32:** AN32 Mode bit
1 = AN32 is using Differential mode
0 = AN32 is using Single-ended mode

bit 0 **SIGN32:** AN32 Signed Data Mode bit
1 = AN32 is using Signed Data mode
0 = AN32 is using Unsigned Data mode

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REGISTER 31-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	MACMAXF<15:8>(1)							
7:0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
	MACMAXF<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MACMAXF<15:0>:** Maximum Frame Length bits(1)

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

Note 1: If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 38-16: DDRDLYCFG3: DDR DELAY CONFIGURATION REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	FAWTDLY<5:0>					
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RAS2RASSBNKDLY<5:0>					
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RAS2PCHRGDLY<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-16 **FAWTDLY<5:0>:** Four Activate Window Time Delay bits
These bits specify the minimum number of clocks within which only four banks may be opened.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RAS2RASSBNKDLY<5:0>:** RAS-to-RAS Same Bank Delay bits
These bits specify the minimum number of clocks required between RAS commands to the same bank.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RAS2PCHRGDLY<4:0>:** RAS-to-Precharge Delay bits
These bits specify the minimum number of clocks required from a RAS command to a Precharge command to the same bank.

39.1 Control Registers

TABLE 39-1: SDHC SFR SUMMARY

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C004	SDHC BLKCON	31:16	BCOUNT<15:0>																0000
		15:0	—	—	—	—	—	—	BSIZE<9:0>										0000
C008	SDHC ARG	31:16	ARG<31:16>																0000
		15:0	ARG<15:0>																0000
C00C	SDHC MODE	31:16	—	—	CIDX<5:0>						CTYPE<1:0>		DPSEL	CIDXCEN	CCRCCEN	—	RESPTYPE<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	BSEL	DTXDSEL	ACEN<1:0>		BCEN	DMAEN	0000
C010	SHDC RESP0	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C014	SHDC RESP1	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C018	SHDC RESP2	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C01C	SHDC RESP3	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C020	SHDC DATA	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
C024	SDHC STAT1	31:16	—	—	—	—	—	—	—	CMDSLVL	DATA3SLVL	DATA2SLVL	DATA1SLVL	DATA0SLVL	WPSLVL	CDSLVL	CARDST	CARDINS	0000
		15:0	—	—	—	—	BREN	BWEN	RDACTIVE	WRACTIVE	—	—	—	—	—	DLACTIVE	CINHDAT	CINHCMD	0000
C028	SDHC CON1	31:16	—	—	—	—	—	WKONREM	WKONINS	WKONINT	—	—	—	—	INTBG	RDWTCON	CONTREQ	SBGREQ	0000
		15:0	—	—	—	—	—	—	—	SDBP	CDSSEL	CDTLVL	—	DMASEL<1:0>		HSEN	DTXWIDTH	—	0000
C02C	SDHC CON2	31:16	—	—	—	—	—	SWRDATA	SWRCMD	SWRALL	—	—	—	—	DTOC<3:0>				0000
		15:0	SDCLKDIV<7:0>								—	—	—	—	—	SDCLKEN	ICLKSTABLE	ICLKEN	0000
C030	SDHC INTSTAT	31:16	—	—	—	—	—	—	ADEIF	ACEIF	CLEIF	DEBEIF	DCRCEIF	DTOEIF	CIDXEIF	CEBEIF	CCRCEIF	CTOEIF	0000
		15:0	EIF	—	—	—	—	—	—	CARDIF	CARDRIF	CARDIIF	BRRDYIF	BWRDYIF	DMAIF	BGIF	TXCIF	CCIF	0000
C034	SDHC INTEN	31:16	—	—	—	—	—	—	ADEIE	AACEIE	CLEIE	DEBEIE	DCRCEIE	DTOEIE	CIDXEIE	CDEBEIE	CCRCEIE	CTOEIE	0000
		15:0	FTZIE	—	—	—	—	—	—	CARDIE	CARDRIE	CARDIIE	BRRDYIE	BWRDYIE	DMAIE	BGIE	TXCIE	CCE	0000
C038	SDHC INTSEN	31:16	—	—	—	—	—	—	ADEISE	ACEISE	CLEISE	DEBEISE	DCRCEISE	DTOEISE	CIDXEISE	CEBEISE	CEBEISE	CCRCEISE	0000
		15:0	FTZEISE	—	—	—	—	—	—	CARDISE	CARDRISE	CARDIISE	BRRDYISE	BWRDYISE	DMAISE	BGISE	TXCISE	CCISE	0000
C03C	SDHC STAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNISSE	—	—	ACIDXE	ACEBE	ACCRCE	ACTOE	ACNEXEC	0000
C040	SDHC CAP	31:16	SLOTTYPE<1:0>		ASYNCINT	—	—	—	—	VOLT3V3	SRESUME	—	HISPEED	—	ADMA2	—	MBLEN<1:0>		0000
		15:0	BASECLK<7:0>								TOCLKU	—	TOCLKFREQ<5:0>						0000
C048	SDHC MAXCAP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	MC3V3<7:0>								0000
C050	SDHCFE	31:16	—	—	—	—	—	—	FEAE	FEACE	FECLE	FEDEBE	FEDCRCE	FEDTOE	FEIDXE	FECEBE	FECCRCE	FECTOE	0000
		15:0	—	—	—	—	—	—	—	—	FECNIACE	—	—	FEACIDXE	FEACEBE	FEACCRCE	FEACTOE	FEACNEE	0000

Legend: '—' = unimplemented; read as '0'.

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41.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129), which are available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MZ DA devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)
- Internal temperature sensor

41.1 Configuration Bits

PIC32MZ DA devices contain two Boot Flash memories (Boot Flash 1 and Boot Flash 2), each with an associated configuration space. These configuration spaces can be programmed to contain various device configurations. Configuration space that is aliased by the Lower Boot Alias memory region is used to provide values for the following Configuration registers. See **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

- DEVSIGN0/ADEVSIGN0: Device Signature Word 0 Register
- DEVCP0/ADEVCP0: Device Code-Protect 0 Register
- DEVCFG0/ADEVCFG0: Device/Alternate Device Configuration Word 0
- DEVCFG1/ADEVCFG1: Device Configuration Word 1
- DEVCFG2/ADEVCFG2: Device Configuration Word 2
- DEVCFG3/ADEVCFG3: Device Configuration Word 3
- DEVCFG4/ADEVCFG4: Device Configuration Word 4
- DEVADCx: Device ADC Calibration Word 'x' ('x' = 0-4, 7)

The following run-time programmable Configuration registers provide additional configuration control:

- CFGCON: Configuration Control Register
- CFGEBIA: External Bus Interface Address Pin Configuration Register
- CFGEBIC: External Bus Interface Control Pin Configuration Register
- CFGPG: Permission Group Configuration Register
- CFGCON2: Configuration Control Register 2
- CFGMPLL: Memory PLL Configuration Register

In addition, the DEVID register (see Register 41-15) provides device and revision information and the DEVSN0 and DEVSN3 registers contain a unique serial number of the device (see Register 41-16).

Note: Do not use word program operation (NVMOP<3:0> = `0001`) when programming the device words that are described in this chapter.

REGISTER 41-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 14-8 **FPLLMULT<6:0>:** System PLL Feedback Divider bits

1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

bit 7 **FPLLICLK:** System PLL Input Clock Select bit

1 = FRC is selected as input to the System PLL
0 = POSC is selected as input to the System PLL

bit 6-4 **FPLLRNG<2:0>:** System PLL Divided Input Clock Frequency Range bits

111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

bit 3 **Reserved:** Write as '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

TABLE 44-26: MPLL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MP10	MF_{IN}	MPLL Input Frequency	8	—	64	MHz	—
MP11	MFV_{CO}	MPLL Vco Frequency Range	400	—	1600	MHz	—
MP12	MF_{MPLL}	MPLL Output Frequency	8	—	400	MHz	—
MP13	M_{LOCK}	MPLL Start-up Time (Lock Time)	—	—	1500 x 1/MF_{IN}	µs	—
MP14	M_{PJ}	MPLL Period Jitter	—		0.015	%	—
MP15	M_{CJ}	MPLL Cycle Jitter	—	—	0.02	%	—
MP16	M_{LTJ}	MPLL Long-term Jitter	—	—	0.5	%	—

Note 1: These parameters are characterized, but not test in manufacturing.

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