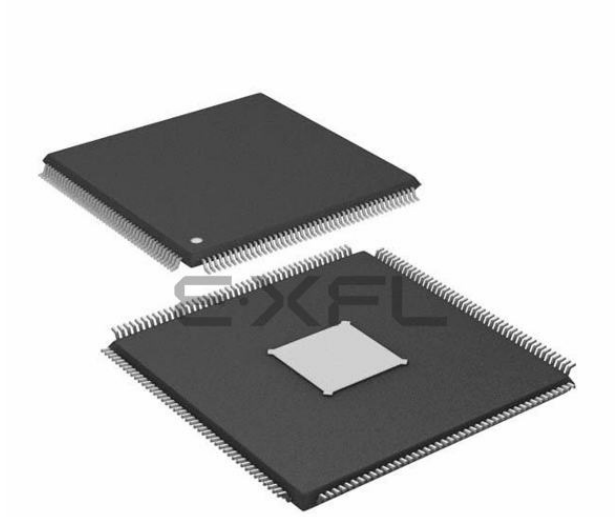
Microchip Technology - PIC32MZ2064DAA176-I/2J Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2064daa176-i-2j

TABLE 6: PIN NAMES FOR 176-PIN DEVICES (CONTINUED)

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAA176
PIC32MZ1025DAB176
PIC32MZ1064DAA176
PIC32MZ1064DAB176
PIC32MZ2025DAA176
PIC32MZ2025DAB176
PIC32MZ2064DAA176
PIC32MZ2064DAB176
PIC32MZ1025DAG176
PIC32MZ1025DAH176
PIC32MZ1064DAG176
PIC32MZ1064DAH176
PIC32MZ2025DAG176
PIC32MZ2025DAH176
PIC32MZ2064DAG176 176
PIC32MZ2064DAH176 1

Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	SCK1/RD1	109	ETXD3/RH1
74	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2	110	ETXD2/RH0
75	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3	111	ERXCLK/EREFCLK/RJ11
76	GD2/EBID15/RPD9/PMD15/RD9	112	ETXD1/RJ9
77	SCK4/RD10	113	ETXD0/RJ8
78	V_{DDR1V8}(5)	114	EMDIO/RJ1
79	RTCC/RPD0/RD0	115	V_{SS}
80	GD7/EBIA12/RPD12/PMA12/RD12	116	V_{DDCORE}
81	GD22/EBIA13/PMA13/RD13	117	V_{DDIO}
82	RPF8/SCL3/RF8	118	ETXERR/RJ0
83	V_{SS}	119	EMDC/RPD11/RD11
84	V_{DDCORE}	120	ETXCLK/RPD7/RD7
85	$\overline{MCLR}$	121	ETXEN/RPD6/RD6
86	V_{DDIO}	122	V_{SS}
87	V_{SS}	123	V_{SS}
88	No Connect	124	V_{DDIO}
89	GD16/EBID8/RPF5/SCL5/PMD8/RF5	125	RPA15/SDA1/RA15
90	GD5/EBIA10/RPF1/PMA10/RF1	126	RPA14/SCL1/RA14
91	GD6/EBIA11/RPF0/PMA11/RF0	127	GD1/EBID14/PMD14/RA4
92	GD21/EBIA23/RH15	128	EBIRDY1/SDA2/RA3
93	ERXERR/RPF3/RF3	129	SCL2/RA2
94	V_{SS}	130	GD19/EBIA21/RK7
95	GD4/EBIA9/RPG1/PMA9/RG1	131	GD15/EBIA20/RK6
96	GD3/EBIA8/RPG0/PMA8/RG0	132	GD14/EBIA19/RK5
97	GD17/EBID9/RPF4/SDA5/PMD9/RF4	133	GD13/EBIA18/RK4
98	EBID3/RPE3/PMD3/RE3	134	GD12/EBIA17/RK3
99	EBID2/PMD2/RE2	135	EBIA3/AN11/PMA3/RK2
100	ERXD1/RH5	136	EBIA1/AN38/PMA1/RK1
101	ERXD2/RH6	137	GD23/EBIA16/RK0
102	V_{DDIO}	138	EBIRDY2/AN37/RH11
103	V_{SS}	139	EBIA4/AN36/PMA4/RH7
104	ERXDV/ECRSDV/RH13	140	AN35/RH3
105	ECRS/RH12	141	$\overline{SDWP}$/EBIRP/RH2
106	ECOL/RH10	142	EBIA0/PMA0/RJ15
107	ERXD3/RH9	143	GD8/EBID11/PMD11/RJ14
108	ERXD0/RH8	144	GD0/EBID13/PMD13/RJ13

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to V_{SS1V8} and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a No Connect in devices without DDR.
7: These pins are restricted to input functions only.

TABLE 1-10: I2C1 THROUGH I2C5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Inter-Integrated Circuit 1						
SCL1	M11	126	T16	I/O	ST	I2C1 Synchronous Serial Clock Input/Output
SDA1	N11	125	U16	I/O	ST	I2C1 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 2						
SCL2	L12	129	U18	I/O	ST	I2C2 Synchronous Serial Clock Input/Output
SDA2	N12	128	U17	I/O	ST	I2C2 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 3						
SCL3	J3	82	P4	I/O	ST	I2C3 Synchronous Serial Clock Input/Output
SDA3	A3	41	A7	I/O	ST	I2C3 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 4						
SCL4	B5	32	C9	I/O	ST	I2C4 Synchronous Serial Clock Input/Output
SDA4	D5	31	D9	I/O	ST	I2C4 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 5						
SCL5	K2	89	T7	I/O	ST	I2C5 Synchronous Serial Clock Input/Output
SDA5	L3	97	U9	I/O	ST	I2C5 Synchronous Serial Data Input/Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-11: COMPARATOR 1, COMPARATOR 2 AND CVREF PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Comparator Voltage Reference						
CVREF+	C10	2	C15	I	Analog	Comparator Voltage Reference (High) Input
CVREF-	B11	1	A17	I	Analog	Comparator Voltage Reference (Low) Input
CVREFOUT	C11	168	E18	O	Analog	Comparator Voltage Reference Output
Comparator 1						
C1INA	D12	170	D17	I	Analog	Comparator 1 Positive Input
C1INB	A12	176	B17	I	Analog	Comparator 1 Selectable Negative Input
C1INC	D5	31	D9	I	Analog	
C1IND	E5	30	A9	I	Analog	
C1OUT	PPS	PPS	PPS	O	—	Comparator 1 Output
Comparator 2						
C2INA	B10	7	B16	I	Analog	Comparator 2 Positive Input
C2INB	A13	172	C17	I	Analog	Comparator 2 Selectable Negative Input
C2INC	C5	33	B9	I	Analog	
C2IND	B5	32	C9	I	Analog	
C2OUT	PPS	PPS	PPS	O	—	Comparator 2 Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

2.10.1.3 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/Boost regulators as the local power source for PIC32MZ DA devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-9. In addition to a more stable power source, using T-Filters can greatly reduce susceptibility to EMI sources and events.

Note:	The EMI/EMC/EFT Suppression Circuit represents only a few supply/ground pairs. However, the number of pairs on a given package may vary. The number of T-Filters in the system depends on the ferrite chip current limitation and the number of supply/ground pairs. For example, with 600 mA current limitation per T-Filter for the 288-LFBGA package, the system should use three T-Filters.

FIGURE 2-9: EMI/EMC/EFT SUPPRESSION CIRCUIT

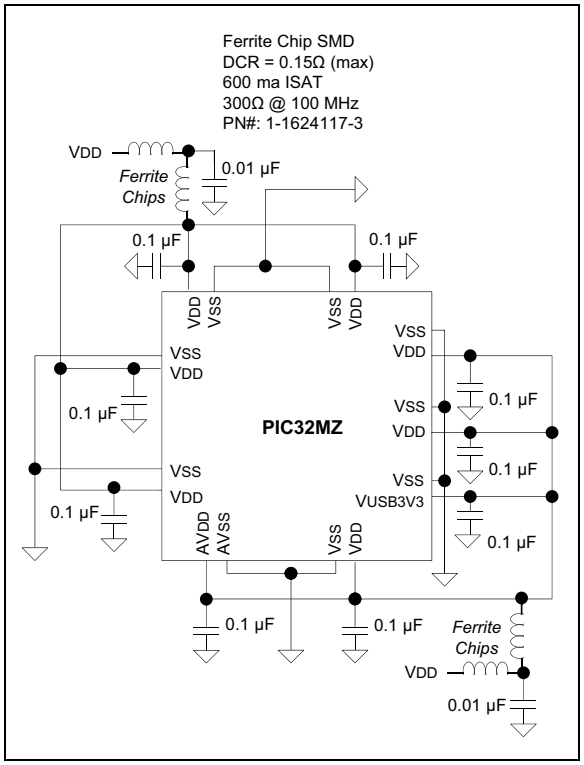

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TABLE 4-8: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Protection Number	Target Description (see Note 5)	SBTxREGy Register (see Note 7)							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
0	System Bus	SBT0REG0	R	0x1F8F0000	R	64 KB	—	0	SBT0RD0	0,1,1,1	SBT0WR0	0,1,1,1
		SBT0REG1	R	0x1F8F8000	R	32 KB	—	3	SBT0RD1	0,0,0,1	SBT0WR1	0,0,0,1
1	Flash Memory(6): Program Flash Boot Flash Prefetch	SBT1REG0	R	0x1D000000	R(4)	R(4)	—	0	SBT1RD0	0,0,0,0	SBT1WR0	0,0,0,0
		SBT1REG2	R	0x1F8E0000	R	4 KB	1	2	SBT1RD2	R/W(1)	SBT1WR2	R/W(1)
		SBT1REG3	R/W	R/W	R/W	R/W	1	2	SBT1RD3	0,0,0,0	SBT1WR3	0,0,0,0
		SBT1REG4	R/W	R/W	R/W	R/W	1	2	SBT1RD4	0,0,0,0	SBT1WR4	0,0,0,0
		SBT1REG5	R/W	R/W	R/W	R/W	1	2	SBT1RD5	0,0,0,0	SBT1WR5	0,0,0,0
		SBT1REG6	R/W	R/W	R/W	R/W	1	2	SBT1RD6	0,0,0,0	SBT1WR6	0,0,0,0
		SBT1REG7	R/W	R/W	R/W	R/W	0	1	SBT1RD7	0,0,0,0	SBT1WR7	0,0,0,0
		SBT1REG8	R/W	R/W	R/W	R/W	0	1	SBT1RD8	0,0,0,0	SBT1WR8	0,0,0,0
2	RAM Bank 1 Memory	SBT2REG0	R	0	R(4)	R(4)	—	0	SBT2RD0	R/W(1)	SBT2WR0	R/W(1)
		SBT2REG1	R/W	R/W	R/W	R/W	—	3	SBT2RD1	R/W(1)	SBT2WR1	R/W(1)
		SBT2REG2	R/W	R/W	R/W	R/W	0	1	SBT2RD2	R/W(1)	SBT2WR2	R/W(1)
3	RAM Bank 2 Memory	SBT3REG0	R(4)	R(4)	R(4)	R(4)	—	0	SBT3RD0	R/W(1)	SBT3WR0	R/W(1)
		SBT3REG1	R/W	R/W	R/W	R/W	—	3	SBT3RD1	R/W(1)	SBT3WR1	R/W(1)
		SBT3REG2	R/W	R/W	R/W	R/W	0	1	SBT3RD2	R/W(1)	SBT3WR2	R/W(1)
4	External Memory via DDR2 and DDR2 Target 0	SBT4REG0	R	0x08000000	R	R(4)	—	0	SBT4RD0	R/W(1)	SBT4WR0	R/W(1)
		SBT4REG1	R/W	R/W	R/W	R/W	—	3	SBT4RD1	R/W(1)	SBT4WR1	R/W(1)
		SBT4REG2	R/W	R/W	R/W	R/W	1	2	SBT4RD2	R/W(1)	SBT4WR2	R/W(1)
		SBT4REG3	R/W	R/W	R/W	R/W	1	2	SBT4RD3	R/W(1)	SBT4WR3	R/W(1)
		SBT4REG4	R/W	R/W	R/W	R/W	1	2	SBT4RD4	R/W(1)	SBT4WR4	R/W(1)
5	External Memory via DDR2 and DDR2 Targets 1 and 2	SBT5REG0	R	0x08000000	R	R(4)	—	0	SBT5RD0	R/W(1)	SBT5WR0	R/W(1)
		SBT5REG1	R/W	R/W	R/W	R/W	—	3	SBT5RD1	R/W(1)	SBT5WR1	R/W(1)
		SBT5REG2	R/W	R/W	R/W	R/W	1	2	SBT5RD2	R/W(1)	SBT5WR2	R/W(1)
		SBT5REG3	R/W	R/W	R/W	R/W	1	2	SBT5RD3	R/W(1)	SBT5WR3	R/W(1)
		SBT5REG4	R/W	R/W	R/W	R/W	1	2	SBT5RD4	R/W(1)	SBT5WR4	R/W(1)

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Map (Figure 4-1) for specific device memory sizes and start addresses.

5: See Table 4-2 for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

7: The 'x' in the SBTxREGy, SBTxRDy, and SBTxWRy registers represents the target protection number and not the actual target number (e.g., for SQI 'x' = 13 and not 11, whereas 11 is the actual target number).

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TABLE 4-13: SYSTEM BUS TARGET PROTECTION GROUP 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

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TABLE 4-18: SYSTEM BUS TARGET PROTECTION GROUP 8 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8820	SBT8ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8824	SBT8ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8828	SBT8ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT8ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT8ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT8REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8850	SBT8RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8858	SBT8WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8860	SBT8REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8870	SBT8RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8878	SBT8WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

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NOTES:

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REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Analog Circuit Ready	_ADC_ARDY_VECTOR	197	OFF197<17:1>	IFS6<5>	IEC6<5>	IPC49<12:10>	IPC49<9:8>	Yes
ADC Update Ready	_ADC_URDY_VECTOR	198	OFF198<17:1>	IFS6<6>	IE6<6>	IPC49<20:18>	IPC49<17:16>	Yes
ADC0 Early Interrupt	_ADC0_EARLY_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
ADC1 Early Interrupt	_ADC1_EARLY_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
ADC2 Early Interrupt	_ADC2_EARLY_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes
ADC3 Early Interrupt	_ADC3_EARLY_VECTOR	202	OFF202<17:1>	IFS6<10>	IEC6<10>	IPC50<20:18>	IPC50<17:16>	Yes
ADC4 Early Interrupt	_ADC4_EARLY_VECTOR	203	OFF203<17:1>	IFS6<11>	IEC6<11>	IPC50<28:26>	IPC50<25:24>	Yes
Reserved	—	—	—	—	—	—	—	—
ADC Group Early Interrupt Request	_ADC_EARLY_VECTOR	205	OFF205<17:1>	IFS6<13>	IEC6<13>	IPC51<12:10>	IPC51<9:8>	Yes
ADC7 Early Interrupt	_ADC7_EARLY_VECTOR	206	OFF206<17:1>	IFS6<14>	IEC6<14>	IPC51<20:18>	IPC51<17:16>	Yes
ADC0 Warm Interrupt	_ADC0_WARM_VECTOR	207	OFF207<17:1>	IFS6<15>	IEC6<15>	IPC51<28:26>	IPC51<25:24>	Yes
ADC1 Warm Interrupt	_ADC1_WARM_VECTOR	208	OFF208<17:1>	IFS6<16>	IEC6<16>	IPC52<4:2>	IPC52<1:0>	Yes
ADC2 Warm Interrupt	_ADC2_WARM_VECTOR	209	OFF209<17:1>	IFS6<17>	IEC6<17>	IPC52<12:10>	IPC52<9:8>	Yes
ADC3 Warm Interrupt	_ADC3_WARM_VECTOR	210	OFF210<17:1>	IFS6<18>	IEC6<18>	IPC52<20:18>	IPC52<17:16>	Yes
ADC4 Warm Interrupt	_ADC4_WARM_VECTOR	211	OFF211<17:1>	IFS6<19>	IEC6<19>	IPC52<28:26>	IPC52<25:24>	Yes
Reserved	—	—	—	—	—	—	—	—
Reserved	—	—	—	—	—	—	—	—
ADC7 Warm Interrupt	_ADC7_WARM_VECTOR	214	OFF214<17:1>	IFS6<22>	IEC6<22>	IPC53<20:18>	IPC53<17:16>	Yes
MPLL Fault Interrupt	_MPLL_FAULT_VECTOR	215	OFF215<17:1>	IFS6<23>	IEC6<23>	IPC53<28:26>	IPC53<25:24>	Yes
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

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REGISTER 11-6: USBIE0CSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	NAKLIM<4:0>				
23:16	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SPEED<1:0>		—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	RXCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **NAKLIM<4:0>:** Endpoint 0 NAK Limit bits

The number of frames/microframes (Hi-Speed transfers) after which Endpoint 0 should time-out on receiving a stream of NAK responses.

bit 23-22 **SPEED<1:0>:** Operating Speed Control bits
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-7 **Unimplemented:** Read as '0'

bit 6-0 **RXCNT<6:0>:** Receive Count bits

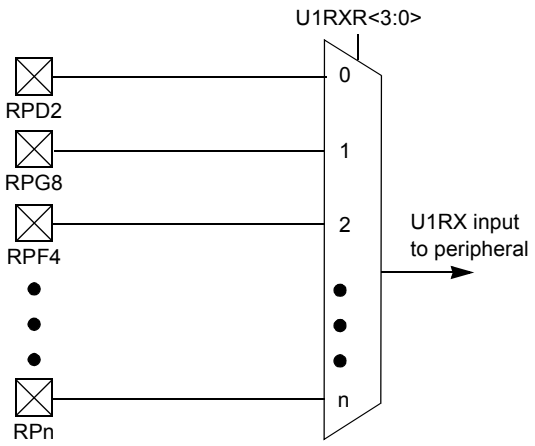
The number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while the RXPKTRDY bit is set.

12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-1, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-1.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

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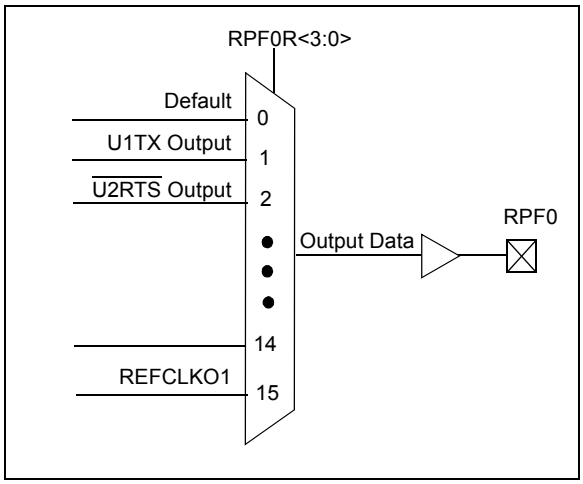
12.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 12-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-2 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0



12.4.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MZ DA devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

12.4.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting the IOLOCK bit prevents writes to the control registers and clearing the IOLOCK bit allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

12.4.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

26.1 EBI Control Registers

TABLE 26-1: EBI REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1014	EBICS0	31:16	CSADDR<15:0>																2000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1018	EBICS1	31:16	CSADDR<15:0>																1000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
101C	EBICS2	31:16	CSADDR<15:0>																2040
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1020	EBICS3	31:16	CSADDR<15:0>																1040
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1054	EBIMSK0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
1058	EBIMSK1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
105C	EBIMSK2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1060	EBIMSK3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1094	EBISMT0	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
1098	EBISMT1	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
109C	EBISMT2	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
10A0	EBIFTRPD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRPD<11:0>												00C8
10A4	EBISMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SMDWIDTH2<2:0>			SMDWIDTH1<2:0>			SMDWIDTH0<2:0>			—	—	—	—	—	—	SMRP	0201

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 29-10: ADCCSS1: ADC COMMON SCAN SELECT REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CSS31:CSS0:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

Note 1: In addition to setting the appropriate bits in this register, Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSS*x* bits. Refer to the bit descriptions in the ADCTRGx registers for selecting the STRIG option.

2: If a Class 1 or Class 2 input is included in the scan by setting the CSSx bit to '1' and by setting the TRGSRCx<4:0> bits to STRIG mode ('0b11), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

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REGISTER 29-14: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CMPE31:CMPE0:** ADC Digital Comparator '*x*' Enable bits

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: CMPE*x* = AN*x*, where '*x*' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

2: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

REGISTER 29-24: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Unimplemented:** Read as '0'

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

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REGISTER 36-1: GLCDMODE: GRAPHICS LCD CONTROLLER MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	LCDEN	CURSOR EN	—	VSYNC POL	HSYNC POL	DEPOL	—	DITHER
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	VSYNC CYC	PCLKPOL	—	PGRAMP EN	FORCE BLANK	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	YUV OUTPUT	FORMAT CLK
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	RGBSEQ<2:0>			—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **LCDEN:** LCD Controller Module Enable bit
1 = LCD Controller module is enabled
0 = LCD Controller module is not enabled

bit 30 **CURSOREN:** Programmable Cursor Enable bit
1 = Programmable cursor is enabled
0 = Programmable cursor is enabled

bit 29 **Unimplemented:** Read as '0'

bit 28 **VSYNCPOL:** Vertical Sync Polarity bit
1 = VSYNC polarity is negative
0 = VSYNC polarity is positive

bit 27 **HSYNCPOL:** Horizontal Sync Polarity bit
1 = HSYNC polarity is negative
0 = HSYNC polarity is positive

bit 26 **DEPOL:** DE Polarity bit
1 = DE polarity is negative
0 = DE polarity is positive

bit 25 **Unimplemented:** Read as '0'

bit 24 **DITHER:** Dithering Enable bit
1 = Dithering is enabled
0 = Dithering is not enabled

bit 23 **VSYNCCYC:** Vertical Sync for Single Cycle Per Line Enable bit
1 = VSYNC for a single cycle per line is enabled
0 = VSYNC for a single cycle per line is not enabled

bit 22 **PCLKPOL:** Pixel Clock Out Polarity bit
1 = Pixel clock out polarity is negative
0 = Pixel clock out polarity is positive

bit 21 **Unimplemented:** Read as '0'

bit 20 **PGRAMPEN:** Palette Gamma Ramp Enable bit
1 = Palette gamma ramp is enabled
0 = Palette gamma ramp is not enabled

REGISTER 38-16: DDRDLYCFG3: DDR DELAY CONFIGURATION REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	FAWTDLY<5:0>					
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RAS2RASSBNKDLY<5:0>					
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RAS2PCHRGDLY<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-16 **FAWTDLY<5:0>:** Four Activate Window Time Delay bits
These bits specify the minimum number of clocks within which only four banks may be opened.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RAS2RASSBNKDLY<5:0>:** RAS-to-RAS Same Bank Delay bits
These bits specify the minimum number of clocks required between RAS commands to the same bank.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RAS2PCHRGDLY<4:0>:** RAS-to-Precharge Delay bits
These bits specify the minimum number of clocks required from a RAS command to a Precharge command to the same bank.

REGISTER 39-13: SDHCCAP: SDHC CAPABILITIES REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1, HS
	—	—	—	—	—	—	—	VOLT3V3
23:16	R-x, HS	U-0	R-x, HS	U-0	R-x, HS	U-0	R-0, HS	R-0, HS
	SRESUME	—	HISPEED	—	ADMA2	—	MBLEN<1:0>	
15:8	U-0	U-0	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS
	—	—	BASECLK<5:0>					
7:0	R-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	TOCLKU	—	TOCLKFREQ<5:0>					

Legend:		HS = Hardware settable	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **VOLT3V3:** 3.3V Voltage Support bit
1 = Voltage of 3.3V is supported

bit 23 **SRESUME:** Suspend/Resume Support bit
1 = Suspend/resume is supported
0 = Suspend/resume is not supported

bit 22 **Unimplemented:** Read as '0'

bit 21 **HISPEED:** High-speed Support bit
1 = High speed is supported
0 = High speed is not supported

bit 20 **Unimplemented:** Read as '0'

bit 19 **ADMA2:** ADMA2 Support bit
1 = ADMA2 is supported
0 = ADMA2 is not supported

bit 18 **Unimplemented:** Read as '0'

bit 17-16 **MBLEN<1:0>:** Maximum Block Length bits
11 = Reserved
10 = 2048
01 = 1024
00 = 512

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **BASECLK<5:0>:** Base Clock Frequency for SDCLK bits
111111 = 63 MHz
111110 = 62 MHz
111101 = 61 MHz
.
.
.
000010 = 2 MHz
000001 = 1 MHz
000000 = Reserved

bit 7 **TOCLKU:** Time-out Clock Unit bit
1 = Time-out clock unit is in kHz
0 = Time-out clock unit is in MHz

bit 6 **Unimplemented:** Read as '0'

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REGISTER 40-1: DSCON: DEEP SLEEP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	HC, R/W-y	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	DSEN(1)	—	DSGPREN	RTCDIS	—	—	—	RTCCWDIS
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DSBOR(2)	RELEASE

Legend:	HC = Hardware Cleared	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **DSEN:** Deep Sleep Enable bit(1)
- 1 = Deep Sleep mode is entered on a WAIT instruction
- 0 = Sleep mode is entered on a WAIT instruction

bit 14 **Unimplemented:** Read as '0'

bit 13 **DSGPREN:** General Purpose Registers Enable bit
- 1 = General purpose register retention is enabled in Deep Sleep mode
- 0 = No general purpose register retention in Deep Sleep mode

bit 12 **RTCDIS:** RTCC Module Disable bit
- 1 = RTCC module is not enabled
- 0 = RTCC module is enabled

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RTCCWDIS:** RTCC Wake-up Disable bit
- 1 = Wake-up from RTCC is disabled
- 0 = Wake-up from RTCC is enabled

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit(2)
- 1 = DSBOREN was enabled and V_{DDCORE} dropped below the DSBOR threshold during Deep Sleep(2)
- 0 = DSBOREN was disabled, or V_{DDCORE} did not drop below the DSBOR threshold during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit
- 1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states
- 0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

Note 1: To enter Deep Sleep mode, Sleep mode must be executed after setting the DSEN bit.

2: Unlike all other events, a Deep Sleep Brown-out Reset (BOR) event will not cause a wake-up from Deep Sleep mode; this bit is present only as a status bit.