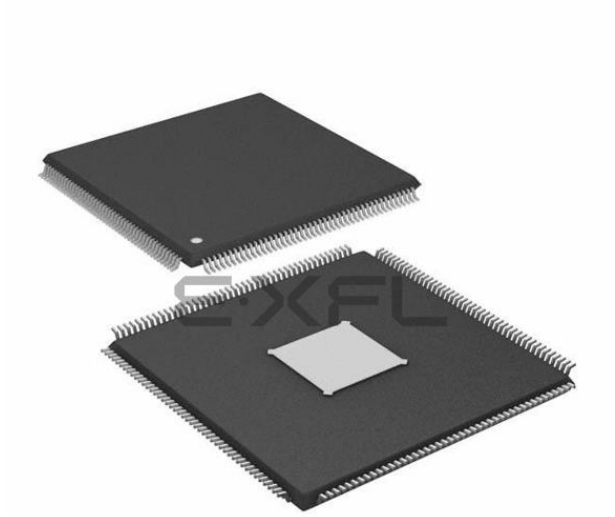

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 640K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 45x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP Exposed Pad |
| Supplier Device Package | 176-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2064daa176t-i-2j |

**TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | 169-pin LFBGA | 176-pin LQFP | 288-pin LFBGA | | | |
| **PORTG** | | | | | | |
| RG0 | N2 | 96 | V9 | I/O | ST | PORTG is a bidirectional I/O port |
| RG1 | M2 | 95 | T8 | I/O | ST | |
| RG6 | E5 | 30 | A9 | I/O | ST | |
| RG7 | D5 | 31 | D9 | I/O | ST | |
| RG8 | B5 | 32 | C9 | I/O | ST | |
| RG9 | C5 | 33 | B9 | I/O | ST | |
| RG12 | E3 | 56 | G4 | I/O | ST | |
| RG13 | E2 | 64 | H4 | I/O | ST | |
| RG14 | E1 | 65 | J4 | I/O | ST | |
| RG15 | A5 | 34 | A8 | I/O | ST | |
| **PORTH** | | | | | | |
| RH0 | M8 | 110 | V13 | I/O | ST | PORTH is a bidirectional I/O port |
| RH1 | M7 | 109 | T12 | I/O | ST | |
| RH2 | H12 | 141 | N16 | I/O | ST | |
| RH3 | J13 | 140 | P18 | I/O | ST | |
| RH4 | D4 | 35 | B8 | I/O | ST | |
| RH5 | M4 | 100 | U10 | I/O | ST | |
| RH6 | N4 | 101 | T10 | I/O | ST | |
| RH7 | J12 | 139 | N15 | I/O | ST | |
| RH8 | N7 | 108 | U12 | I/O | ST | |
| RH9 | N6 | 107 | V12 | I/O | ST | |
| RH10 | M6 | 106 | T11 | I/O | ST | |
| RH11 | K13 | 138 | P17 | I/O | ST | |
| RH12 | N5 | 105 | U11 | I/O | ST | |
| RH13 | M5 | 104 | V11 | I/O | ST | |
| RH14 | C3 | 42 | A6 | I/O | ST | |
| RH15 | L2 | 92 | V8 | I/O | ST | |
| **PORTJ** | | | | | | |
| RJ0 | L10 | 118 | V15 | I/O | ST | PORTJ is a bidirectional I/O port |
| RJ1 | K10 | 114 | U14 | I/O | ST | |
| RJ2 | F10 | 152 | K16 | I/O | ST | |
| RJ3 | E8 | 151 | K17 | I/O | ST | |
| RJ4 | F13 | 150 | K18 | I/O | ST | |
| RJ5 | F12 | 149 | L18 | I/O | ST | |
| RJ6 | G11 | 148 | L17 | I/O | ST | |
| RJ7 | G13 | 147 | L16 | I/O | ST | |
| RJ8 | N9 | 113 | V14 | I/O | ST | |
| RJ9 | M9 | 112 | T13 | I/O | ST | |
| RJ10 | F8 | 146 | M18 | I/O | ST | |
| RJ11 | N8 | 111 | U13 | I/O | ST | |
| RJ12 | F9 | 145 | M17 | I/O | ST | |
| RJ13 | G12 | 144 | M16 | I/O | ST | |
| RJ14 | G10 | 143 | N18 | I/O | ST | |
| RJ15 | H13 | 142 | N17 | I/O | ST | |

**Legend:** CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

**TABLE 1-23: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | 169-pin LFBGA | 176-pin LQFP | 288-pin LFBGA | | | |
| VSS1V8 | G4, H4, J4, K4, L4, L5 | See **Note 1** | D3, F6, F7, F8, G6, G7, G8, G9, H9, J9, K9, L9, M6, M7, M8, M9, N6, N7, N8, N9, R4 | P | — | Ground reference for DDR2 SDRAM memory. |
| **Voltage Reference** | | | | | | |
| DDRVREF | F4 (**Note 3**) | 66 (**Note 3**) | J11 | P | — | 1.8V Voltage Reference to DDR2 SDRAM memory. |
| VREF+ | C10 | 2 | C15 | I | Analog | Analog Voltage Reference (High) Input |
| VREF- | B11 | 1 | A17 | I | Analog | Analog Voltage Reference (Low) Input |

**Legend:** CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

**Note 1:** The metal plane at the bottom of the device is internally tied to VSS1V8 and must be connected to 1.8V ground externally.
**2:** This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
**3:** This pin is a No Connect in devices without DDR.

**TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

| Interrupt Source(1) | XC32 Vector Name | IRQ # | Vector # | Interrupt Bit Location | | | | Persistent Interrupt |
|---|---|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority | Sub-priority | |
| ADC Digital Filter 1 | _ADC_DF1_VECTOR | 52 | OFF052<17:1> | IFS1<20> | IEC1<20> | IPC13<4:2> | IPC13<1:0> | Yes |
| ADC Digital Filter 2 | _ADC_DF2_VECTOR | 53 | OFF053<17:1> | IFS1<21> | IEC1<21> | IPC13<12:10> | IPC13<9:8> | Yes |
| ADC Digital Filter 3 | _ADC_DF3_VECTOR | 54 | OFF054<17:1> | IFS1<22> | IEC1<22> | IPC13<20:18> | IPC13<17:16> | Yes |
| ADC Digital Filter 4 | _ADC_DF4_VECTOR | 55 | OFF055<17:1> | IFS1<23> | IEC1<23> | IPC13<28:26> | IPC13<25:24> | Yes |
| ADC Digital Filter 5 | _ADC_DF5_VECTOR | 56 | OFF056<17:1> | IFS1<24> | IEC1<24> | IPC14<4:2> | IPC14<1:0> | Yes |
| ADC Digital Filter 6 | _ADC_DF6_VECTOR | 57 | OFF057<17:1> | IFS1<25> | IEC1<25> | IPC14<12:10> | IPC14<9:8> | Yes |
| ADC Fault | _ADC_FAULT_VECTOR | 58 | OFF058<17:1> | IFS1<26> | IEC1<26> | IPC14<20:18> | IPC14<17:16> | Yes |
| ADC Data 0 | _ADC_DATA0_VECTOR | 59 | OFF059<17:1> | IFS1<27> | IEC1<27> | IPC14<28:26> | IPC14<25:24> | Yes |
| ADC Data 1 | _ADC_DATA1_VECTOR | 60 | OFF060<17:1> | IFS1<28> | IEC1<28> | IPC15<4:2> | IPC15<1:0> | Yes |
| ADC Data 2 | _ADC_DATA2_VECTOR | 61 | OFF061<17:1> | IFS1<29> | IEC1<29> | IPC15<12:10> | IPC15<9:8> | Yes |
| ADC Data 3 | _ADC_DATA3_VECTOR | 62 | OFF062<17:1> | IFS1<30> | IEC1<30> | IPC15<20:18> | IPC15<17:16> | Yes |
| ADC Data 4 | _ADC_DATA4_VECTOR | 63 | OFF063<17:1> | IFS1<31> | IEC1<31> | IPC15<28:26> | IPC15<25:24> | Yes |
| ADC Data 5 | _ADC_DATA5_VECTOR | 64 | OFF064<17:1> | IFS2<0> | IEC2<0> | IPC16<4:2> | IPC16<1:0> | Yes |
| ADC Data 6 | _ADC_DATA6_VECTOR | 65 | OFF065<17:1> | IFS2<1> | IEC2<1> | IPC16<12:10> | IPC16<9:8> | Yes |
| ADC Data 7 | _ADC_DATA7_VECTOR | 66 | OFF066<17:1> | IFS2<2> | IEC2<2> | IPC16<20:18> | IPC16<17:16> | Yes |
| ADC Data 8 | _ADC_DATA8_VECTOR | 67 | OFF067<17:1> | IFS2<3> | IEC2<3> | IPC16<28:26> | IPC16<25:24> | Yes |
| ADC Data 9 | _ADC_DATA9_VECTOR | 68 | OFF068<17:1> | IFS2<4> | IEC2<4> | IPC17<4:2> | IPC17<1:0> | Yes |
| ADC Data 10 | _ADC_DATA10_VECTOR | 69 | OFF069<17:1> | IFS2<5> | IEC2<5> | IPC17<12:10> | IPC17<9:8> | Yes |
| ADC Data 11 | _ADC_DATA11_VECTOR | 70 | OFF070<17:1> | IFS2<6> | IEC2<6> | IPC17<20:18> | IPC17<17:16> | Yes |
| ADC Data 12 | _ADC_DATA12_VECTOR | 71 | OFF071<17:1> | IFS2<7> | IEC2<7> | IPC17<28:26> | IPC17<25:24> | Yes |
| ADC Data 13 | _ADC_DATA13_VECTOR | 72 | OFF072<17:1> | IFS2<8> | IEC2<8> | IPC18<4:2> | IPC18<1:0> | Yes |
| ADC Data 14 | _ADC_DATA14_VECTOR | 73 | OFF073<17:1> | IFS2<9> | IEC2<9> | IPC18<12:10> | IPC18<9:8> | Yes |
| ADC Data 15 | _ADC_DATA15_VECTOR | 74 | OFF074<17:1> | IFS2<10> | IEC2<10> | IPC18<20:18> | IPC18<17:16> | Yes |
| ADC Data 16 | _ADC_DATA16_VECTOR | 75 | OFF075<17:1> | IFS2<11> | IEC2<11> | IPC18<28:26> | IPC18<25:24> | Yes |
| ADC Data 17 | _ADC_DATA17_VECTOR | 76 | OFF076<17:1> | IFS2<12> | IEC2<12> | IPC19<4:2> | IPC19<1:0> | Yes |
| ADC Data 18 | _ADC_DATA18_VECTOR | 77 | OFF077<17:1> | IFS2<13> | IEC2<13> | IPC19<12:10> | IPC19<9:8> | Yes |
| ADC Data 19 | _ADC_DATA19_VECTOR | 78 | OFF078<17:1> | IFS2<14> | IEC2<14> | IPC19<20:18> | IPC19<17:16> | Yes |
| ADC Data 20 | _ADC_DATA20_VECTOR | 79 | OFF079<17:1> | IFS2<15> | IEC2<15> | IPC19<28:26> | IPC19<25:24> | Yes |
| ADC Data 21 | _ADC_DATA21_VECTOR | 80 | OFF080<17:1> | IFS2<16> | IEC2<16> | IPC20<4:2> | IPC20<1:0> | Yes |

**Note 1:** Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

**2:** Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

**REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)**

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 3 uses Shadow Set 0)
0111 = Interrupt with a priority level of 3 uses Shadow Set 7
0110 = Interrupt with a priority level of 3 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 2 uses Shadow Set 0)
0111 = Interrupt with a priority level of 2 uses Shadow Set 7
0110 = Interrupt with a priority level of 2 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 1 uses Shadow Set 0)
0111 = Interrupt with a priority level of 1 uses Shadow Set 7
0110 = Interrupt with a priority level of 1 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

**Note 1:** These bits are ignored if the MVEC bit (INTCON<12>) = 0.

## 10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

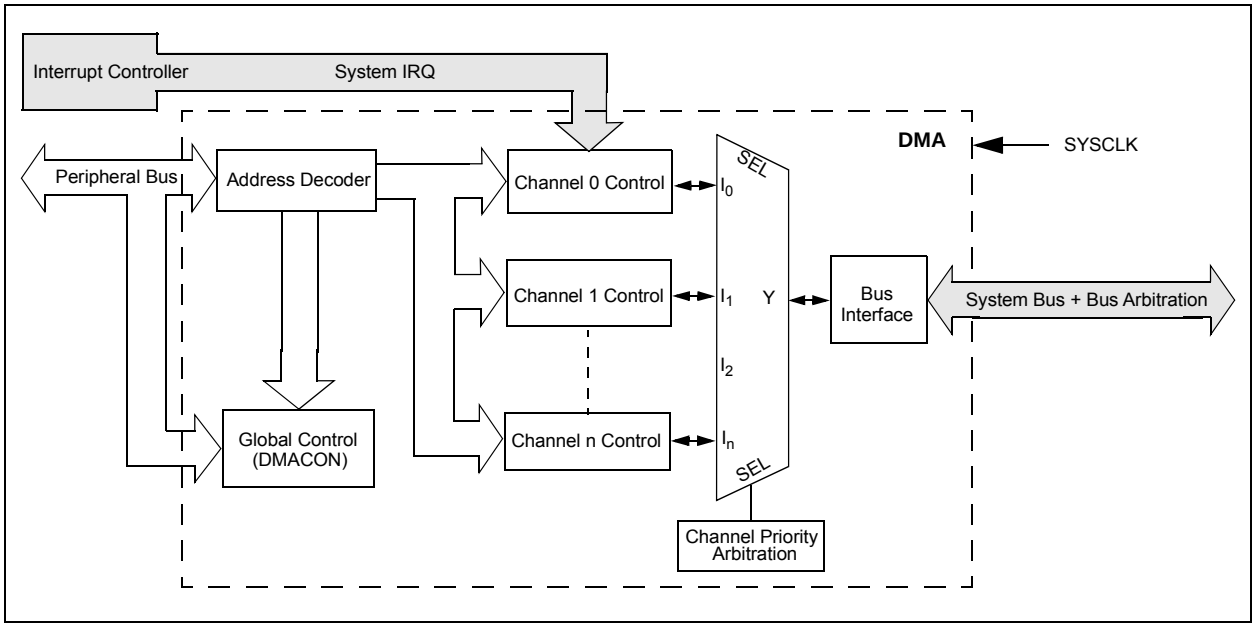
**Note:** This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the device such as SPI, UART, PMP, etc., or memory itself.

Following are some of the key features of the DMA Controller module:

- Eight identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Up to 2-byte Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent error address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

**FIGURE 10-1: DMA BLOCK DIAGRAM**



**REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)**

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

**ERROR:** No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

**REGISTER 11-17: USBEOFRST: USB END-OF-FRAME/SOFT RESET CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | NRSTX | NRST |
| 23:16 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R.W-0 | R/W-1 | R/W-0 |
| | LSEOF<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R.W-1 | R/W-1 | R/W-1 |
| | FSEOF<7:0> | | | | | | | |
| 7:0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R.W-0 | R/W-0 | R/W-0 |
| | HSEOF<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **NRSTX:** Reset of XCLK Domain bit
1 = Reset the XCLK domain, which is clock recovered from the received data by the PHY
0 = Normal operation

bit 24 **NRST:** Reset of CLK Domain bit
1 = Reset the CLK domain, which is clock recovered from the peripheral bus
0 = Normal operation

bit 23-16 **LSEOF<7:0>:** Low-Speed EOF bits
These bits set the Low-Speed transaction in units of 1.067 µs (default setting is 121.6 µs) prior to the EOF to stop new transactions from beginning.

bit 15-8 **FSEOF<7:0>:** Full-Speed EOF bits
These bits set the Full-Speed transaction in units of 533.3 µs (default setting is 63.46 µs) prior to the EOF to stop new transactions from beginning.

bit 7-0 **HSEOF<7:0>:** Hi-Speed EOF bits
These bits set the Hi-Speed transaction in units of 133.3 µs (default setting is 17.07µs) prior to the EOF to stop new transactions from beginning.

**TABLE 12-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1538 | RPA14R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA14R<3:0> | | | | 0000 |
| 153C | RPA15R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA15R<3:0> | | | | 0000 |
| 1540 | RPB0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB0R<3:0> | | | | 0000 |
| 1544 | RPB1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB1R<3:0> | | | | 0000 |
| 1548 | RPB2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB2R<3:0> | | | | 0000 |
| 154C | RPB3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB3R<3:0> | | | | 0000 |
| 1554 | RPB5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB5R<3:0> | | | | 0000 |
| 1558 | RPB6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB6R<3:0> | | | | 0000 |
| 155C | RPB7R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB7R<3:0> | | | | 0000 |
| 1560 | RPB8R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB8R<3:0> | | | | 0000 |
| 1564 | RPB9R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB9R<3:0> | | | | 0000 |
| 1568 | RPB10R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB10R<3:0> | | | | 0000 |
| 157C | RPB15R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB15R<3:0> | | | | 0000 |
| 1584 | RPC1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC1R<3:0> | | | | 0000 |
| 1588 | RPC2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC2R<3:0> | | | | 0000 |
| 158C | RPC3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC3R<3:0> | | | | 0000 |
| 15B4 | RPC13R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC13R<3:0> | | | | 0000 |
| 15B8 | RPC14R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC14R<3:0> | | | | 0000 |
| 15C0 | RPD0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD0R<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 16.1 Output Compare Control Registers

**TABLE 16-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP**

| Virtual Address (BF84_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 4000 | OC1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 4010 | OC1R | 31:16 | OC1R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4020 | OC1RS | 31:16 | OC1RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4200 | OC2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 4210 | OC2R | 31:16 | OC2R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4220 | OC2RS | 31:16 | OC2RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4400 | OC3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 4410 | OC3R | 31:16 | OC3R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4420 | OC3RS | 31:16 | OC3RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4600 | OC4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 4610 | OC4R | 31:16 | OC4R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4620 | OC4RS | 31:16 | OC4RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4800 | OC5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 4810 | OC5R | 31:16 | OC5R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4820 | OC5RS | 31:16 | OC5RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

## 27.0 CRYPTO ENGINE

**Note:** This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Crypto Engine is intended to accelerate applications that need cryptographic functions. By executing these functions in the hardware module, software overhead is reduced, and actions such as encryption, decryption, and authentication can execute much more quickly.

The Crypto Engine uses an internal descriptor-based DMA for efficient programming of the security association data and packet pointers (allowing scatter/gather data fetching). An intelligent state machine schedules the crypto engines based on the protocol selection and packet boundaries. The hardware engines can perform the encryption and authentication in sequence or in parallel.

Key features of the Crypto Engine are:

- Bulk ciphers and hash engines
- Integrated DMA to off-load processing:
  - Buffer descriptor-based
  - Secure association per buffer descriptor
- Some functions can execute in parallel

Bulk ciphers that are handled by the Crypto Engine include:

- AES:
  - 128-bit, 192-bit, and 256-bit key sizes
  - CBC, ECB, CTR, CFB, and OFB modes
- DES/TDES:
  - CBC, ECB, CFB, and OFB modes

Authentication engines that are available through the Crypto Engine include:

- SHA-1
- SHA-256
- MD-5
- AES-GCM
- HMAC operation (for all authentication engines)

The rate of data that can be processed by the Crypto Engine depends on a number of factors, including:

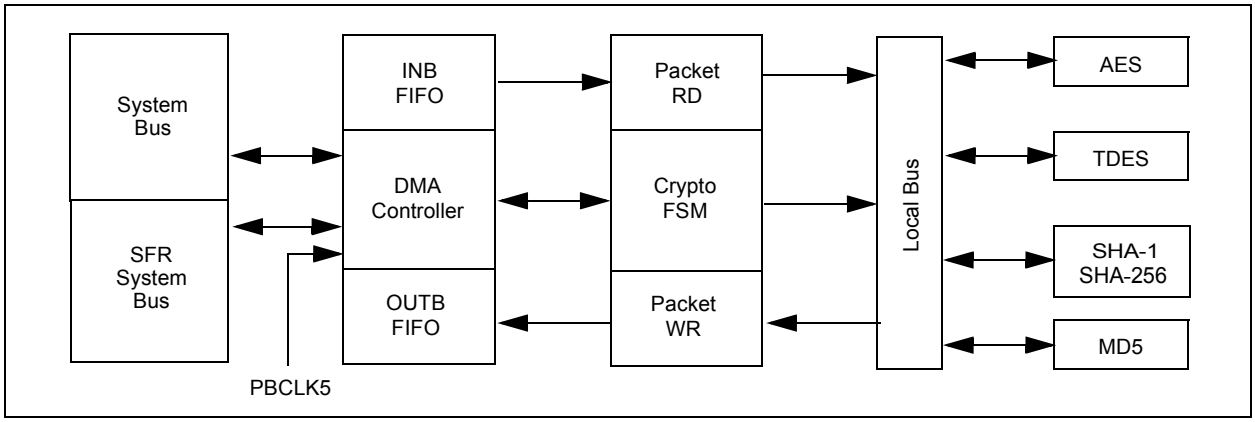
- Which engine is in use
- Whether the engines are used in parallel or in series
- The demands on source and destination memories by other parts of the system (i.e., CPU, DMA, etc.)
- The speed of PBCLK5, which drives the Crypto Engine

Table 27-1 provides typical performance for various engines. Figure 27-1 illustrates the Crypto Engine block diagram.

**TABLE 27-1: CRYPTO ENGINE PERFORMANCE**

| Engine/ Algorithm | Performance Factor (Mbps/MHz) | Maximum Mbps (PBCLK5 = 100 MHz) |
|---|---|---|
| DES | 14.4 | 1440 |
| TDES | 6.6 | 660 |
| AES-128 | 9.0 | 900 |
| AES-192 | 7.9 | 790 |
| AES-256 | 7.2 | 720 |
| MD5 | 15.6 | 1560 |
| SHA-1 | 13.2 | 1320 |
| SHA-256 | 9.3 | 930 |

**FIGURE 27-1: CRYPTO ENGINE BLOCK DIAGRAM**



**REGISTER 29-25: ADCDATAx: ADC OUTPUT DATA REGISTER 'x' ('x' = 0 THROUGH 43)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<31:24> | | | | | | | |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<23:16> | | | | | | | |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

**Note 1:** When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

**2:** Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

**REGISTER 30-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6 (CONTINUED)**

bit 15 **FLTEN25:** Filter 25 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL25<1:0>:** Filter 25 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL25<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN24:** Filter 24 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL24<1:0>:** Filter 24 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL24<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 31-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-1 |
| | — | — | CWINDOW<5:0> | | | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | — | — | — | — | RETX<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RETX<3:0>:** Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is '0xF'.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**TABLE 38-1: DDR SDRAM CONTROLLER REGISTER SUMMARY (CONTINUED)**

| Virtual Address (BF8E_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 80A8 | DDR CMD110 | 31:16 | MDALCMD<7:0> | | | | | | | | WEN CMD2 | CASCMD2 | RASCMD2 | CSCMD2<7:3> | | | | | 0000 |
| | | 15:0 | CSCMD2<2:0> | | | CLKEN CMD2 | WEN CMD1 | CASCMD1 | RASCMD1 | CSCMD1<7:0> | | | | | | | | CLKEN CMD1 | 0000 |
| 80AC | DDR CMD111 | 31:16 | MDALCMD<7:0> | | | | | | | | WEN CMD2 | CASCMD2 | RASCMD2 | CSCMD2<7:3> | | | | | 0000 |
| | | 15:0 | CSCMD2<2:0> | | | CLKEN CMD2 | WEN CMD1 | CASCMD1 | RASCMD1 | CSCMD1<7:0> | | | | | | | | CLKEN CMD1 | 0000 |
| 80B0 | DDR CMD112 | 31:16 | MDALCMD<7:0> | | | | | | | | WEN CMD2 | CASCMD2 | RASCMD2 | CSCMD2<7:3> | | | | | 0000 |
| | | 15:0 | CSCMD2<2:0> | | | CLKEN CMD2 | WEN CMD1 | CASCMD1 | RASCMD1 | CSCMD1<7:0> | | | | | | | | CLKEN CMD1 | 0000 |
| 80B4 | DDR CMD113 | 31:16 | MDALCMD<7:0> | | | | | | | | WEN CMD2 | CASCMD2 | RASCMD2 | CSCMD2<7:3> | | | | | 0000 |
| | | 15:0 | CSCMD2<2:0> | | | CLKEN CMD2 | WEN CMD1 | CASCMD1 | RASCMD1 | CSCMD1<7:0> | | | | | | | | CLKEN CMD1 | 0000 |
| 80B8 | DDR CMD114 | 31:16 | MDALCMD<7:0> | | | | | | | | WEN CMD2 | CASCMD2 | RASCMD2 | CSCMD<27:3> | | | | | 0000 |
| | | 15:0 | CSCMD2<2:0> | | | CLKEN CMD2 | WEN CMD1 | CASCMD1 | RASCMD1 | CSCMD1<7:0> | | | | | | | | CLKEN CMD1 | 0000 |
| 80BC | DDR CMD115 | 31:16 | MDALCMD<7:0> | | | | | | | | WEN CMD2 | CASCMD2 | RASCMD2 | CSCMD2<7:3> | | | | | 0000 |
| | | 15:0 | CSCMD2<2:0> | | | CLKEN CMD2 | WEN CMD1 | CASCMD1 | RASCMD1 | CSCMD1<7:0> | | | | | | | | CLKEN CMD1 | 0000 |
| 80C0 | DDR CMD20 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80C4 | DDR CMD21 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80C8 | DDR CMD22 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80CC | DDR CMD23 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80D0 | DDR CMD24 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80D4 | DDR CMD25 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80D8 | DDR CMD26 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80DC | DDR CMD27 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80E0 | DDR CMD28 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |
| 80E4 | DDR CMD29 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | WAIT<8:5> | | | | 0000 |
| | | 15:0 | WAIT<4:0> | | | | | BNKADDRCMD<2:0> | | | MDADDRHCMD<7:0> | | | | | | | | 0000 |

**REGISTER 38-5: DDRMEMCON: DDR MEMORY CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | INITDN | STINIT |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **Unimplemented:** Read as '0'

bit 1 **INITDN:** Memory Initialize Done bit

Set by software after memory initialization is completed to enable controller for regular operation.

1 = All commands have been issued; the controller is enabled for regular operation
0 = Controller not enabled for regular operation

bit 0 **STINIT:** Memory Initialize Start bit

Set by software after the memory initialization commands are loaded into the DDRCMD registers to start memory initialization.

1 = Start memory initialization
0 = Do not start memory initialization

**REGISTER 39-1: SDHCBLKCON: SDHC BLOCK CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BCOUNT<15:8>(1) | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BCOUNT<7:0>(1) | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | BSIZE<9:8>(2) | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BSIZE<7:0>(2) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **BCOUNT<31:0>:** Blocks Count for Current Transfer bits(1)

These bits represent the number of blocks. The software sets this value between 1 and 65,535 blocks and the SDHC decrements the count after each block transfer and stops when the count reaches zero.
0xFFFF = 65,535 blocks
0x0002 = 2 blocks
0x0001 = 1 block
0x0000 = Stop count Blocks Count for Current Transfer bits

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **BSIZE<9:0>:** Transfer Block Size bits(2)

These bits specify the block size of the data transfer for CMD17, CMD18, CMD24, CMD25, and CMD53.
0x200 = 512 bytes
0x1FF = 511 bytes
•
•
•
0x002 = 2 bytes
0x001 = 1 byte
0x000 = No data transfer

**Note 1:** These bits are only used when the BCEN bit (SDHCMODE<1>) is set to '1' and is valid only for multiple block transfers. The BCOUNT<15:0> bits need not be set if the BSIZE bit (SDHCMODE<5>) is set to '0'.

**2:** These bits can only be accessed when no transactions are in progress. Read operations during transfers will return an invalid value and write operations to these bits will be ignored.

**REGISTER 41-3: DEVCFG0/ADEVCFG0: DEVICE/ALTERNATE DEVICE CONFIGURATION WORD 0 (CONTINUED)**

bit 10 **FSLEEP:** Flash Sleep Mode bit
1 = Flash is powered down when the device is in Sleep mode
0 = Flash power down is controlled by the VREGS bit (PWRCON<0>)

bit 9-8 **FECCCON<1:0>:** Dynamic Flash ECC Configuration bits
11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

**Note:** Upon a device POR, the value of these bits are copied by hardware into CFGCON<5:4> bits, (i.e. ECCCON<1:0>.

bit 7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit
1 = Boot code and Exception code is MIPS32
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit
1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit
1 = JTAG is enabled
0 = JTAG is disabled

**Note 1:** On Reset, this Configuration bit is copied into JTAGEN (CFGCON<3>). If JTAGEN (DEVCFG0<2>) = 0, the JTAGEN bit cannot be set to '1' by the user application at run-time, as JTAG is always disabled. However, if JTAGEN (DEVCFG0<2>) = 1, the user application may enable/disable JTAG at run-time by simply writing JTAGEN (CFGCON<3> as required.

**2:** This bit sets the value of the JTAGEN bit in the CFGCON register.

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
11 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Disabled
10 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Enabled
01 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Disabled
00 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Enabled

**Note:** When the FJTAGEN or JTAGEN bits are equal to '0', this prevents 4-wire JTAG debugging, but not PGECx/PGEDx debugging.

**TABLE 44-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: $V_{DDIO}$ = 2.2V to 3.6V, $V_{DDCORE}$ = 1.7V to 1.9V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDDIO | I/O Supply Voltage **(Note 1)** | 2.2 | — | 3.6 | V | — |
| DC11 | VDDCORE | Core Supply Voltage **(Note 1)** | 1.7 | 1.8 | 1.9 | V | — |
| DC12 | SVDDIO/ SVDDCORE | **VDDIO/VDDCORE Rise Rate** to Ensure Internal Power-on Reset Signal **(Note 2)** | 0.000011 | — | 1.1 | V/µs | 300 ms to 3 µs @ 3.3v |
| DC13 | VBAT | Battery Supply Voltage | 2.2 | — | 3.6 | V | — |
| DC14 | VDDR1V8 | DDR Memory Supply Voltage | 1.7 | 1.8 | 1.9 | V | — |
| DC15 | DDRVREF | DDR Reference Voltage | 0.49 x VDDR1V8 | 0.50 x VDDR1V8 | 0.51 x VDDR1V8 | V | — |

**Note 1:** Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

**2:** Voltage on VDDIO must always be greater than or equal to VDDCORE during power-up.

**TABLE 44-5: ELECTRICAL CHARACTERISTICS: RESETS**

| DC CHARACTERISTICS (Note 1) | | | Standard Operating Conditions: $V_{DDIO}$ = 2.2V to 3.6V, $V_{DDCORE}$ = 1.7V to 1.9V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| RST10 | VPORIO | VDDIO POR Voltage **(Note 2)** | VSS + 0.3 | — | 1.75 | V | — |
| RST11 | VPORCORE /VBATSW | VDDCORE POR Voltage **(Note 2)**<br>VDDCORE to VBAT Switch Voltage **(Note 3)** | VSS + 0.3 | — | 1.7 | V | — |
| RST12 | VBORIO | BOR Event on VDDIO transition high-to-low **(Note 4)** | 1.92 | — | 2.2 | V | — |
| RST13 | VPORBAT | POR Event on VBAT **(Note 4)** | 1.35 | — | 2.2 | V | — |
| RST14 | VHVD1V8 | High Voltage Detect on VDDR1V8 pins | 2.16 | — | 2.24 | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**2:** This is the limit to which VDDIO/VDDCORE must be lowered to ensure Power-on Reset.

**3:** Device enters VBAT mode upon VDDCORE Power-on Reset.

**4:** Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages.

**FIGURE 44-21: PARALLEL SLAVE PORT TIMING**

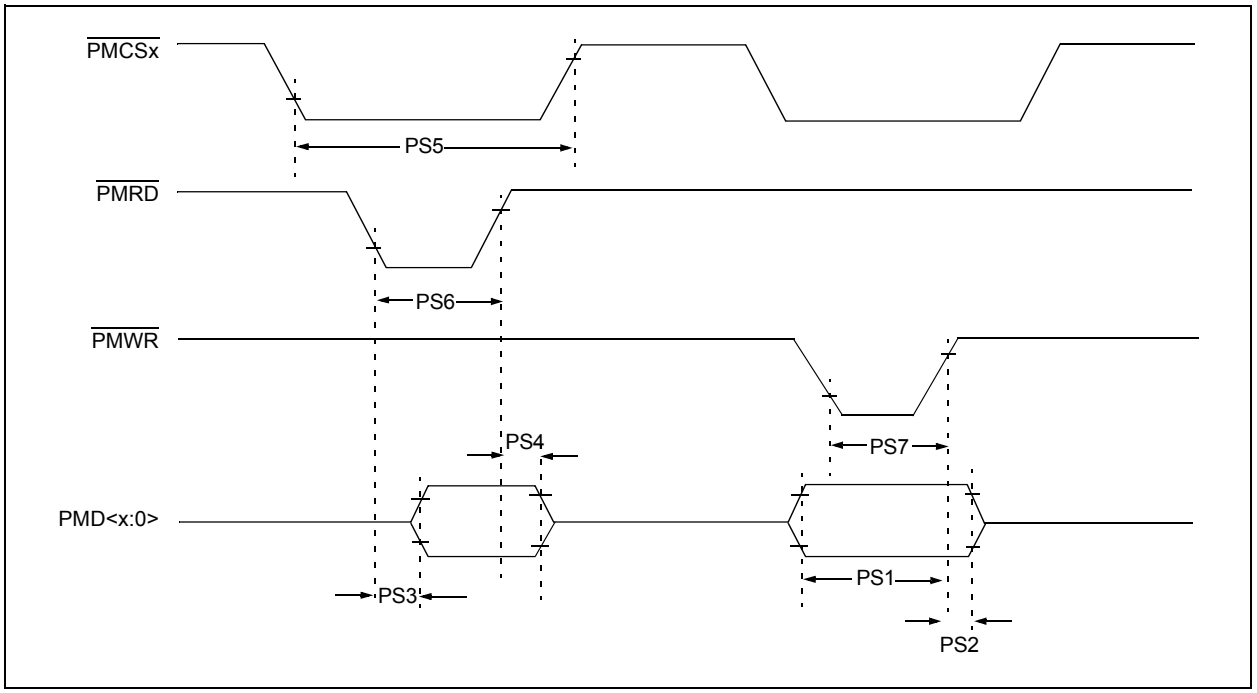



**TABLE 44-49: PARALLEL SLAVE PORT REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: $V_{DDIO}$ = 2.2V to 3.6V, $V_{DDCORE}$ = 1.7V to 1.9V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param.No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PS1 | TdtV2wrH | Data In Valid before $\overline{PMWR}$ or $\overline{PMCSx}$ Inactive (setup time) | 20 | — | — | ns | — |
| PS2 | TwrH2dtI | $\overline{PMWR}$ or $\overline{PMCSx}$ Inactive to Data-in Invalid (hold time) | 40 | — | — | ns | — |
| PS3 | TrdL2dtV | $\overline{PMRD}$ and $\overline{PMCSx}$ Active to Data-out Valid | — | — | 60 | ns | — |
| PS4 | TrdH2dtI | $\overline{PMRD}$ Active or $\overline{PMCSx}$ Inactive to Data-out Invalid | 0 | — | 10 | ns | — |
| PS5 | Tcs | $\overline{PMCSx}$ Active Time | TPBCLK2 + 40 | — | — | ns | — |
| PS6 | TWR | $\overline{PMWR}$ Active Time | TPBCLK2 + 25 | — | — | ns | — |
| PS7 | TRD | $\overline{PMRD}$ Active Time | TPBCLK2 + 25 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**NOTES:**