

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, PMP, SPI, SQT, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	288-LFBGA
Supplier Device Package	288-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2064daa288-i-4j

PIC32MZ Graphics (DA) Family

TABLE 1-18: SQ11 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Serial Quad Interface						
SQ1CLK	E4	54	E4	O	—	Serial Quad Interface Clock
SQ1CS0	F1	70	K4	O	—	Serial Quad Interface Chip Select 0
SQ1CS1	F2	71	L4	O	—	Serial Quad Interface Chip Select 1
SQ1D0	E2	64	H4	I/O	ST	Serial Quad Interface Data 0
SQ1D1	E3	56	G4	I/O	ST	Serial Quad Interface Data 1
SQ1D2	E1	65	J4	I/O	ST	Serial Quad Interface Data 2
SQ1D3	D1	55	F4	I/O	ST	Serial Quad Interface Data 3

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 1-19: SDHC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
SDHC						
SDCK	E4	54	E4	O	—	SD Serial Clock
SDCMD	F1	70	K4	O	—	SD Command/Response
SDDATA0	E2	64	H4	I/O	ST	SD Serial Data 0
SDDATA1	E3	56	G4	I/O	ST	SD Serial Data 1
SDDATA2	E1	65	J4	I/O	ST	SD Serial Data 2
SDDATA3	D1	55	F4	I/O	ST	SD Serial Data 3/Card Detect
SDCD	D2	53	D4	I	ST	SD Mechanical Card Detect
SDWP	H12	141	N16	I	ST	SD Write Protect

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 1-20: CTMU PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Charge Time Measurement Unit						
CTED1	B9	11	A14	I	ST	CTMU External Edge Input 1
CTED2	C12	169	D18	I	ST	CTMU External Edge Input 2
CTPLS	F7	9	B15	O	—	CTMU Output Pulse

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

PIC32MZ Graphics (DA) Family

REGISTER 4-6: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13) (CONTINUED)

- bit 15-8 **INITID<7:0>**: Initiator ID of Requester bits
11111111 = Reserved
.
.
00001111 = Reserved
00001110 = SDHC
00001101 = GPU
00001100 = GLCD
00001011 = Crypto Engine
00001010 = Flash Controller
00001001 = SQ11
00001000 = CAN2
00000111 = CAN1
00000110 = Ethernet Write
00000101 = Ethernet Read
00000100 = USB
00000011 = DMA Write
00000010 = DMA Read
00000001 = CPU
00000000 = Reserved
- bit 7-4 **REGION<3:0>**: Requested Region Number bits
1111 - 0000 = Target's region that reported a permission group violation
- bit 3 **Unimplemented**: Read as '0'
- bit 2-0 **CMD<2:0>**: Transaction Command of the Requester bits
111 = Reserved
110 = Reserved
101 = Write (a non-posted write)
100 = Reserved
011 = Read (a locked read caused by a Read-Modify-Write transaction)
010 = Read
001 = Write
000 = Idle

Note: Refer to Table 4-8 for the list of available targets and their descriptions.

PIC32MZ Graphics (DA) Family

REGISTER 8-7: SLEWCON: OSCILLATOR SLEW CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	SYSDIV<3:0> ⁽¹⁾		
7:0	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0
						SLWDIV<2:0>		
						R/W-1	R/W-0	R-0, HS, HC
						UPEN	DNEN	BUSY

Legend:	HC = Hardware Cleared	HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-16 **SYSDIV<3:0>:** System Clock Divide Control bits⁽¹⁾

1111 = SYSCLK is divided by 16

1110 = SYSCLK is divided by 15

.

.

.

0010 = SYSCLK is divided by 3

0001 = SYSCLK is divided by 2

0000 = SYSCLK is not divided

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **SLWDIV<2:0>:** Slew Divisor Steps Control bits

These bits control the maximum division steps used when slewing during a frequency change.

111 = Steps are divide by 128, 64, 32, 16, 8, 4, 2, and then no divisor

110 = Steps are divide by 64, 32, 16, 8, 4, 2, and then no divisor

101 = Steps are divide by 32, 16, 8, 4, 2, and then no divisor

100 = Steps are divide by 16, 8, 4, 2, and then no divisor

011 = Steps are divide by 8, 4, 2, and then no divisor

010 = Steps are divide by 4, 2, and then no divisor

001 = Steps are divide by 2, and then no divisor

000 = No divisor is used during slewing

The steps apply in reverse order (i.e., 2, 4, 8, etc.) during a downward frequency change.

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **UPEN:** Upward Slew Enable bit

1 = Slewing enabled for switching to a higher frequency

0 = Slewing disabled for switching to a higher frequency

bit 1 **DNEN:** Downward Slew Enable bit

1 = Slewing enabled for switching to a lower frequency

0 = Slewing disabled for switching to a lower frequency

bit 0 **BUSY:** Clock Switching Slewing Active Status bit

1 = Clock frequency is being actively slewed to the new frequency

0 = Clock switch has reached its final value

Note 1: The SYSDIV<3:0> bit settings are ignored if both UPEN and DNEN = 0, and SYSCLK will be divided by 1.

9.2 Prefetch Control Registers

TABLE 9-1: PREFETCH REGISTER MAP

Virtual Address (BF8E_#)	Register Name(s)	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
0000	PRECON	31:16	—	—	—	—	—	PFMSECEN	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	PREFEN<1:0>	—	—	PFMWS<2:0>	—	0007
0010	PRESTAT	31:16	—	—	—	—	PFMDDED	PFMSEC	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PFMSECCNT<7:0>	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 “CLR, SET, and INV Registers” for more information.

PIC32MZ Graphics (DA) Family

REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RDWR	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	DMACH<2:0>		

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31 **RDWR**: Read/Write Status bit

1 = Last DMA bus access when an error was detected was a read
0 = Last DMA bus access when an error was detected was a write

bit 30-3 **Unimplemented**: Read as '0'

bit 2-0 **DMACH<2:0>**: DMA Channel bits

These bits contain the value of the most recent active DMA channel when an error was detected.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-0 **DMAADDR<31:0>**: DMA Module Address bits

These bits contain the address of the most recent DMA access when an error was detected.

PIC32MZ Graphics (DA) Family

REGISTER 11-6: USBIE0CSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	NAKLIM<4:0>				
23:16	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SPEED<1:0>		—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	RXCNT<6:0>						

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **NAKLIM<4:0>:** Endpoint 0 NAK Limit bits

The number of frames/microframes (Hi-Speed transfers) after which Endpoint 0 should time-out on receiving a stream of NAK responses.

bit 23-22 **SPEED<1:0>:** Operating Speed Control bits

11 = Low-Speed

10 = Full-Speed

01 = Hi-Speed

00 = Reserved

bit 21-7 **Unimplemented:** Read as '0'

bit 6-0 **RXCNT<6:0>:** Receive Count bits

The number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while the RXPTRDY bit is set.

TABLE 12-4: PORTB REGISTER MAP

Virtual Address (BF86_#)	Register Name (')	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB15	ANSB14	ANSB13	ANSB12	ANSB11	ANSB10	ANSB9	ANSB8	ANSB7	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	FFBF
0110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
0120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
0130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
0140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
0150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
0160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
0170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
0190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000
01A0	CNNEB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEB15	CNNEB14	CNNEB13	CNNEB12	CNNEB11	CNNEB10	CNNEB9	CNNEB8	CNNEB7	CNNEB6	CNNEB5	CNNEB4	CNNEB3	CNNEB2	CNNEB1	CNNEB0	0000
01B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB15	CNFB14	CNFB13	CNFB12	CNFB11	CNFB10	CNFB9	CNFB8	CNFB7	CNFB6	CNFB5	CNFB4	CNFB3	CNFB2	CNFB1	CNFB0	0000
01C0	SRCON0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1B15	SR1B14	SR1B13	SR1B12	SR1B11	SR1B10	SR1B9	SR1B8	SR1B7	SR1B6	SR1B5	SR1B4	SR1B3	SR1B2	SR1B1	SR1B0	0000
01D0	SRCON1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SROB15	SROB14	SROB13	SROB12	SROB11	SROB10	SROB9	SROB8	SROB7	SROB6	SROB5	SROB4	SROB3	SROB2	SROB1	SROB0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

PIC32MZ Graphics (DA) Family

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 5-4 **TCKPS<1:0>**: Timer Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value
- bit 3 **Unimplemented**: Read as '0'
- bit 2 **TSYNC**: Timer External Clock Input Synchronization Selection bit
When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized
When TCS = 0:
This bit is ignored.
- bit 1 **TCS**: Timer Clock Source Select bit
1 = External clock is defined by the TECS<1:0> bits
0 = Internal peripheral clock
- bit 0 **Unimplemented**: Read as '0'

PIC32MZ Graphics (DA) Family

REGISTER 25-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HS = Hardware Set	SC = Software Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit

- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit

- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits

- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit

- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit

- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits

- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

PIC32MZ Graphics (DA) Family

REGISTER 29-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

- bit 10 **FSSCLKEN**: Fast Synchronous System Clock to ADC Control Clock bit
1 = Fast synchronous system clock to ADC control clock is enabled
0 = Fast synchronous system clock to ADC control clock is disabled
- bit 9 **FSPBCLKEN**: Fast Synchronous Peripheral Clock to ADC Control Clock bit
1 = Fast synchronous peripheral clock to ADC control clock is enabled
0 = Fast synchronous peripheral clock to ADC control clock is disabled
- bit 8-7 **Unimplemented**: Read as '0'
- bit 6-4 **IRQVS<2:0>**: Interrupt Vector Shift bits
To determine interrupt vector address, this bit specifies the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with the ADCBASE register.
Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).
111 = Shift x left 7 bit position
110 = Shift x left 6 bit position
101 = Shift x left 5 bit position
100 = Shift x left 4 bit position
011 = Shift x left 3 bit position
010 = Shift x left 2 bit position
001 = Shift x left 1 bit position
000 = Shift x left 0 bit position
- bit 3 **STRGLVL**: Scan Trigger High Level/Positive Edge Sensitivity bit
1 = Scan trigger is high level sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), the scan trigger will continue for all selected analog inputs, until the STRIG option is removed.
0 = Scan trigger is positive edge sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), only a single scan trigger will be generated, which will complete the scan of all selected analog inputs.
- bit 2-0 **Unimplemented**: Read as '0'

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 "Output Compare"** and Figure 32-1 in **32.0 "Comparator"** for more information.

PIC32MZ Graphics (DA) Family

REGISTER 29-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

bit 6-0 **ADCDIV<6:0>**: Shared ADC (ADC7) Clock Divider bits

11111111 = 254 * T_Q = T_{AD7}

.

.

.

00000111 = 6 * T_Q = T_{AD7}

00000101 = 4 * T_Q = T_{AD7}

00000011 = 2 * T_Q = T_{AD7}

00000000 = Reserved

The ADCDIV<6:0> bits divide the ADC control clock (T_Q) to generate the clock for the Shared ADC, ADC7 (T_{AD7}).

PIC32MZ Graphics (DA) Family

REGISTER 29-8: ADCGIRQEN1: ADC GLOBAL INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN31	AGIEN30	AGIEN29	AGIEN28	AGIEN27	AGIEN26	AGIEN25	AGIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN23	AGIEN22	AGIEN21	AGIEN20	AGIEN19	AGIEN18	AGIEN17	AGIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **AGIEN31:AGIEN0**: ADC Global Interrupt Enable bits

- 1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the ARDYx bit ('x' = 31-0) of the ADCDSTAT1 register)
- 0 = Interrupts are disabled

REGISTER 29-9: ADCGIRQEN2: ADC GLOBAL INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AGIEN43	AGIEN42	AGIEN41	AGIEN40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN39	AGIEN38	AGIEN37	AGIEN36	AGIEN35	AGIEN34	AGIEN33	AGIEN32

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-12 **Unimplemented**: Read as '0'

bit 11-0 **AGIEN43:AGIEN32**: ADC Global Interrupt Enable bits

- 1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the ARDYx bit ('x' = 43-32) of the ADCDSTAT2 register)
- 0 = Interrupts are disabled

PIC32MZ Graphics (DA) Family

REGISTER 29-34: ADCSYSCFG1: ADC SYSTEM CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
AN<31:23>								
23:16	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
AN<23:16>								
15:8	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
AN<15:8>								
7:0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
AN<7:0>								

Legend:	HS = Hardware Set	HC = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-0 **AN<31:0>**: ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

REGISTER 29-35: ADCSYSCFG2: ADC SYSTEM CONFIGURATION REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—								
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—								
15:8	U-0	U-0	U-0	U-0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
—					AN<43:40>			
7:0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
AN<39:32>								

Legend:	HS = Hardware Set	HC = Cleared by Software
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **AN<43:32>**: ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

PIC32MZ Graphics (DA) Family

REGISTER 31-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER (CONTINUED)

- bit 7 **CRCERREN:** CRC Error Collection Enable bit
1 = The received packet CRC must be invalid for the packet to be accepted
0 = Disable CRC Error Collection filtering
This bit allows the user to collect all packets that have an invalid CRC.
- bit 6 **CRCOKEN:** CRC OK Enable bit
1 = The received packet CRC must be valid for the packet to be accepted
0 = Disable CRC filtering
This bit allows the user to reject all packets that have an invalid CRC.
- bit 5 **RUNTERREN:** Runt Error Collection Enable bit
1 = The received packet must be a runt packet for the packet to be accepted
0 = Disable Runt Error Collection filtering
This bit allows the user to collect all packets that are runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes (when CRCOKEN = 0) or any packet with a size of less than 64 bytes that has a valid CRC (when CRCOKEN = 1).
- bit 4 **RUNTEN:** Runt Enable bit
1 = The received packet must not be a runt packet for the packet to be accepted
0 = Disable Runt filtering
This bit allows the user to reject all runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes.
- bit 3 **UCEN:** Unicast Enable bit
1 = Enable Unicast Filtering
0 = Disable Unicast Filtering
This bit allows the user to accept all unicast packets whose Destination Address matches the Station Address.
- bit 2 **NOTMEEN:** Not Me Unicast Enable bit
1 = Enable Not Me Unicast Filtering
0 = Disable Not Me Unicast Filtering
This bit allows the user to accept all unicast packets whose Destination Address does not match the Station Address.
- bit 1 **MCEN:** Multicast Enable bit
1 = Enable Multicast Filtering
0 = Disable Multicast Filtering
This bit allows the user to accept all Multicast Address packets.
- bit 0 **BCEN:** Broadcast Enable bit
1 = Enable Broadcast Filtering
0 = Disable Broadcast Filtering
This bit allows the user to accept all Broadcast Address packets.

- Note 1:** XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

- | |
|--|
| <p>Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.</p> |
|--|

PIC32MZ Graphics (DA) Family

REGISTER 36-18: GLCDCURDATAx: GRAPHICS LCD CONTROLLER CURSOR DATA 'n' REGISTER ('n' = 0-127)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0> ⁽¹⁾				PIXELxy<3:0> ⁽¹⁾			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0> ⁽¹⁾				PIXELxy<3:0> ⁽¹⁾			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0> ⁽¹⁾				PIXELxy<3:0> ⁽¹⁾			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0> ⁽¹⁾				PIXELxy<3:0> ⁽¹⁾			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

bit 27-24 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

bit 23-20 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

bit 19-16 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

bit 15-12 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

bit 11-8 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

bit 7-4 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

bit 3-0 **PIXELxy<3:0>**: Pixel 'xy' Color Lookup bits⁽¹⁾

Note 1: For the PIXELxy bits, x = 0-31 and y = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

PIC32MZ Graphics (DA) Family

REGISTER 38-10: DDRMEMCFG4: DDR MEMORY CONFIGURATION REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	CSADDRMSK<2>
7:0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CSADDRMSK<1:0>		—	—	—	BNKADDRMSK<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8-6 **CSADDRMSK<2:0>:** Chip Select Address Mask bits

These bits, which are used in conjunction with the CSADDR<4:0> bits (DDRMEMCFG0<20:16>), determine which bits of user address space are used to derive the Chip Select address for the DDR memory.

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BNKADDRMSK<2:0>:** Bank Address Mask bits

These bits, which are used in conjunction with the BNKADDR<4:0> bits (DDRMEMCFG0<12:8>), determine which bits of user address space are used to derive the bank address for the DDR memory.

PIC32MZ Graphics (DA) Family

REGISTER 41-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	R/P UPLLFSEL	r-1 —	R/P FDSEN	R/P DSWDTEN	R/P DSWDTOSC	R/P DSWDTPS<4:3>	R/P
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	DSWDTPS<2:0>			DSBORNEN	VBATBORNEN	FPLLODIV<2:0>		
15:8	r-1 —	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FPLLMULT<6:0>							
7:0	R/P FPLLICK	R/P	R/P	R/P	R/P	r-1 —	R/P	R/P FPLLIDIV<2:0>

Legend:

R = Readable bit

-n = Value at POR

r = Reserved bit

W = Writable bit

'1' = Bit is set

P = Programmable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31 **Reserved:** Write as '1'

bit 30 **UPLLFSEL:** USB PLL Input Frequency Select bit

1 = UPLL input clock is 24 MHz

0 = UPLL input clock is 12 MHz

bit 29 **Reserved:** Write as '1'

bit 28 **FDSEN:** Deep Sleep Enable bit

1 = Deep Sleep mode is entered on a WAIT instruction

0 = Sleep mode is entered on a WAIT instruction

bit 27 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit

1 = Enable the Deep Sleep Watchdog Timer (DSWDT) during Deep Sleep mode

0 = Disable the DSWDT during Deep Sleep mode

bit 26 **DSWDTOSC:** Deep Sleep Watchdog Timer Reference Clock Select bit

1 = Select the LPRC Oscillator as the DSWDT reference clock

0 = Select the Secondary Oscillator as the DSWDT reference clock

42.0 INSTRUCTION SET

The PIC32MZ Graphics (DA) Family family instruction set complies with the MIPS32[®] Release 2 instruction set architecture. The PIC32MZ DA device family *does not* support the following features:

- Core extend instructions
- Coprocessor 2 instructions

Note: Refer to “MIPS32[®] Architecture for Programmers Volume II: The MIPS32[®] Instruction Set” at www.imgtec.com for more information.

PIC32MZ Graphics (DA) Family

FIGURE 44-2: EXTERNAL CLOCK TIMING

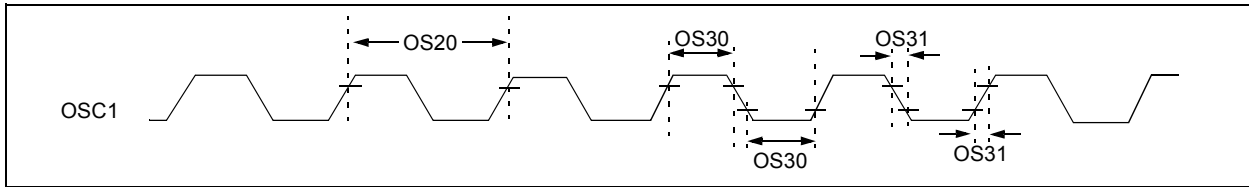


TABLE 44-23: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: $V_{DDIO} = 2.2V$ to $3.6V$, $V_{DDCORE} = 1.7V$ to $1.9V$ (unless otherwise stated) Operating temperature $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	64	MHz	EC (Note 2)
OS13		Oscillator Crystal Frequency	4	—	32	MHz	HS (Note 2)
OS15			32	32.768	100	kHz	Sosc (Note 2)
OS20	Tosc	$Tosc = 1/Fosc$	—	—	—	—	See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	$0.375 \times Tosc$	—	—	ns	EC (Note 2)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	7.5	ns	EC (Note 2)
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, and Sosc Clock Oscillator modes)	—	1024	—	TOSC	(Note 2)
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 2)
OS42	GM	External Oscillator Transconductance	—	400	—	$\mu A/V$	$V_{DDIO} = 3.3V$, $T_A = +25^{\circ}C$ (Note 2)

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

2: This parameter is characterized, but not tested in manufacturing.

PIC32MZ Graphics (DA) Family

TABLE 44-57: SD HOST CONTROLLER DEFAULT MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: $V_{DDIO} = 2.2V$ to $3.6V$, $V_{DDCORE} = 1.7V$ to $1.9V$ (unless otherwise stated) Operating temperature $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ for Industrial				
Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
SD20	tSDCK	Clock Frequency	—	—	25	MHz	—
SD21	tDUTY	Duty Cycle	—	50	—	%	—
SD22	tHIGH	Clock High Time	10	—	—	ns	—
SD23	tLOW	Clock Low Time	10	—	—	ns	—
SD24	tRISE	Clock Rise Time	—	10	—	ns	—
SD25	tFALL	Clock Fall Time	—	10	—	ns	—
SD26	tSETUP	Input Setup Time	5	—	—	ns	—
SD27	tHOLD	Input Hold Time	5	—	—	ns	—

TABLE 44-58: SD HOST CONTROLLER HIGH-SPEED MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: $V_{DDIO} = 2.2V$ to $3.6V$, $V_{DDCORE} = 1.7V$ to $1.9V$ (unless otherwise stated) Operating temperature $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ for Industrial				
Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
SD30	tSDCK	Clock Frequency	—	—	50	MHz	—
SD31	tDUTY	Duty Cycle	—	50	—	%	—
SD32	tHIGH	Clock High Time	7	—	—	ns	—
SD33	tLOW	Clock Low Time	7	—	—	ns	—
SD34	tRISE	Clock Rise Time	—	3	—	ns	—
SD35	tFALL	Clock Fall Time	—	3	—	ns	—
SD36	tSETUP	Input Setup Time	6	—	—	ns	—
SD37	tHOLD	Input Hold Time	2	—	—	ns	—