Microchip Technology - PIC32MZ2064DAB169T-I/HF Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2064dab169t-i-hf

TABLE 1: PIC32MZ DA FEATURES COMMON TO ALL DEVICES

Boot Flash Memory (KB)	Remappable Peripherals						12-bit ADC Channels	Analog Comparators	CTMU	USB 2.0 HS OTG	I^2C	GLCD	GPU	EBI	PMP	SQI	SDHC	RTCC	Ethernet	I/O Pins	JTAG	Trace
	Remappable Pins	Timers(1)/Capture/ Compare	UART	SPI/I^2S	CAN 2.0B	External Interrupts(2)																
160	47	9/9/9	6	6	2	5	45	2	Y	Y	5	Y	Y	Y	Y	Y	Y	Y	Y	120	Y	Y

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.

TABLE 2: 169-PIN LFBGA PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/ Dedicated)
PIC32MZ1025DAA169	1024	256	No	—	N	8/24
PIC32MZ1025DAB169					Y	8/26
PIC32MZ1064DAA169		640			N	8/24
PIC32MZ1064DAB169					Y	8/26
PIC32MZ2025DAA169	2048	256			N	8/24
PIC32MZ2025DAB169					Y	8/26
PIC32MZ2064DAA169		640			N	8/24
PIC32MZ2064DAB169					Y	8/26
PIC32MZ1025DAG169	1024	256	Yes (INT)	32	N	8/24
PIC32MZ1025DAH169					Y	8/26
PIC32MZ1064DAG169		640			N	8/24
PIC32MZ1064DAH169					Y	8/26
PIC32MZ2025DAG169	2048	256			N	8/24
PIC32MZ2025DAH169					Y	8/26
PIC32MZ2064DAG169		640			N	8/24
PIC32MZ2064DAH169					Y	8/26

TABLE 3: 176-PIN LQFP PIC32MZ DA FEATURES

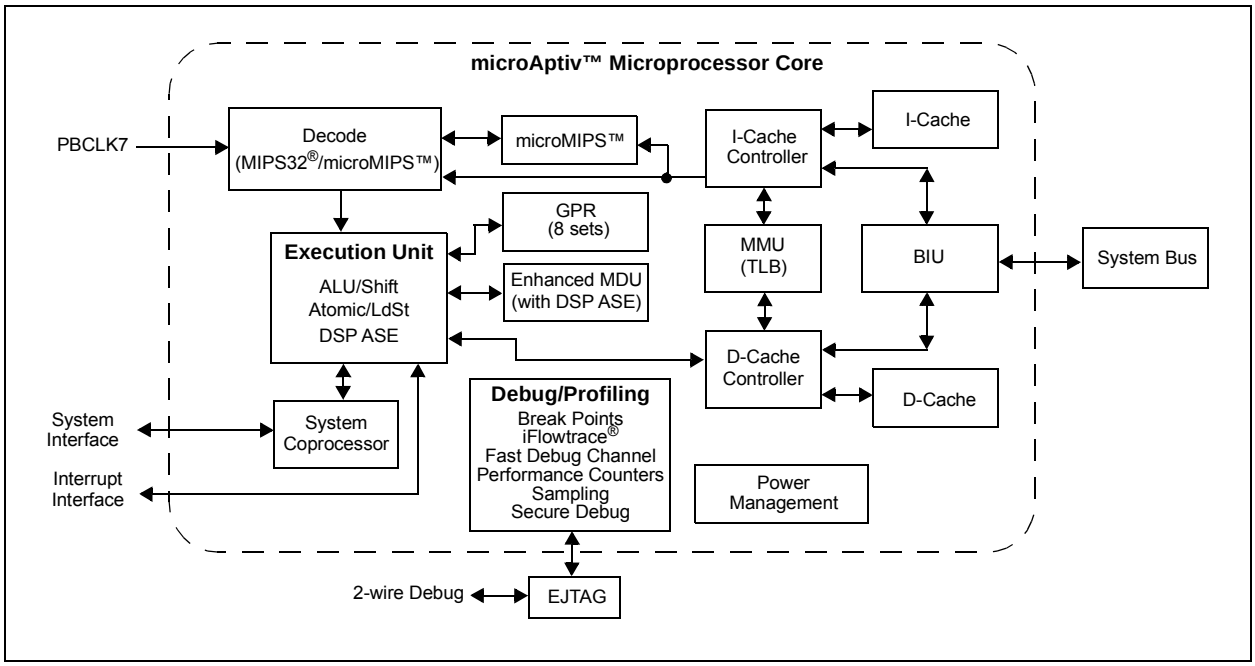
Devices	Program Memory (KB	Data Memory (KB	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/ Dedicated)
PIC32MZ1025DAA176	1024	256	No	—	N	8/24
PIC32MZ1025DAB176					Y	8/26
PIC32MZ1064DAA176		640			N	8/24
PIC32MZ1064DAB176					Y	8/26
PIC32MZ2025DAA176	2048	256			N	8/24
PIC32MZ2025DAB176					Y	8/26
PIC32MZ2064DAA176		640			N	8/24
PIC32MZ2064DAB176					Y	8/26
PIC32MZ1025DAG176	1024	256	Yes (INT)	32	N	8/24
PIC32MZ1025DAH176					Y	8/26
PIC32MZ1064DAG176		640			N	8/24
PIC32MZ1064DAH176					Y	8/26
PIC32MZ2025DAG176	2048	256			N	8/24
PIC32MZ2025DAH176					Y	8/26
PIC32MZ2064DAG176		640			N	8/24
PIC32MZ2064DAH176					Y	8/26

TABLE 4: 288-PIN LFBGA PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	Crypto/RNG	DMA Channels (Programmable/Dedicated)
PIC32MZ1025DAA288	1024	256	Yes (EXT)	N	8/24
PIC32MZ1025DAB288				Y	8/26
PIC32MZ1064DAA288		640		N	8/24
PIC32MZ1064DAB288				Y	8/26
PIC32MZ2025DAA288	2048	256		N	8/24
PIC32MZ2025DAB288				Y	8/26
PIC32MZ2064DAA288		640		N	8/24
PIC32MZ2064DAB288				Y	8/26

A block diagram of the PIC32MZ DA family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ DA FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



REGISTER 5-4: NVMDATAx: FLASH DATA REGISTER (x = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATA<31:0>:** Flash Data bits
Word Program: Writes NVMDATA0 to the target Flash address defined in NVMADDR
Quad Word Program: Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the Least Significant Instruction Word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits
The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 22	_ADC_DATA22_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
ADC Data 23	_ADC_DATA23_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
ADC Data 24	_ADC_DATA24_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes
ADC Data 25	_ADC_DATA25_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
ADC Data 26	_ADC_DATA26_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
ADC Data 27	_ADC_DATA27_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
ADC Data 28	_ADC_DATA28_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
ADC Data 29	_ADC_DATA29_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
ADC Data 30	_ADC_DATA30_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
ADC Data 31	_ADC_DATA31_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
ADC Data 32	_ADC_DATA32_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Data 33	_ADC_DATA33_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
ADC Data 34	_ADC_DATA34_VECTOR	93	OFF093<17:1>	IFS2<29>	IEC2<29>	IPC23<12:10>	IPC23<9:8>	Yes
ADC Data 35	_ADC_DATA35_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Data 36	_ADC_DATA36_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Data 37	_ADC_DATA37_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Data 38	_ADC_DATA38_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Data 39	_ADC_DATA39_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Data 40	_ADC_DATA40_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Data 41	_ADC_DATA41_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC Data 42	_ADC_DATA42_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Data 43	_ADC_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
USB Suspend/Resume Event	_USB1_SR_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	No
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes
System Bus Protection Violation	_SYSTEM_BUS_PROTECTION_VECTOR	106	OFF106<17:1>	IFS3<10>	IEC3<10>	IPC26<20:18>	IPC26<17:16>	Yes
Crypto Engine Event	_CRYPTO_VECTOR	107	OFF107<17:1>	IFS3<11>	IEC3<11>	IPC26<28:26>	IPC26<25:24>	Yes
Reserved	—	108	—	—	—	—	—	—
SPI1 Fault	_SPI1_FAULT_VECTOR	109	OFF109<17:1>	IFS3<13>	IEC3<13>	IPC27<12:10>	IPC27<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 19-16 **TXFIFOSZ<3:0>:** TX Endpoint FIFO packet size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **TXEDMA:** TX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 8 **RXEDMA:** RX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 7 **BDEV:** USB Device Type bit
1 = USB is operating as a 'B' device
0 = USB is operating as an 'A' device

bit 6 **FSDEV:** Full-Speed/Hi-Speed device detection bit (*Host mode*)
1 = A Full-Speed or Hi-Speed device has been detected being connected to the port
0 = No Full-Speed or Hi-Speed device detected

bit 5 **LSDEV:** Low-Speed Device Detection bit (*Host mode*)
1 = A Low-Speed device has been detected being connected to the port
0 = No Low-Speed device detected

bit 4-3 **VBUS<1:0>:** VBUS Level Detection bits
11 = Above VBUS Valid
10 = Above AValid, below VBUS Valid
11 = Above Session End, below AValid
00 = Below Session End

bit 2 **HOSTMODE:** Host Mode bit
1 = USB module is acting as a Host
0 = USB module is not acting as a Host

bit 1 **HOSTREQ:** Host Request Control bit
'B' device only:
1 = USB module initiates the Host Negotiation when Suspend mode is entered. This bit is cleared when Host Negotiation is completed.
0 = Host Negotiation is not taking place

NOTES:

17.1 Deadman Timer Control Registers

TABLE 17-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0A10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0A20	DMTCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0A30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0A40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0A60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	0000
0A70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 22-4: SQI1CON: SQI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	r-0	R/W-0
	—	—	—	—	—	—	—	SCHECK(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DDRMODE	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<7:0>							

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **Reserved:** Must be programmed as '0'

bit 24 **SCHECK:** Flash Status Check bit(1)
- 1 = Check the status of the Flash
- 0 = Do not check the status of the Flash

bit 23 **DDRMODE:** Double Data Rate Mode bit
- 1 = Set the SQI transfers to DDR mode
- 0 = Set the SQI transfers to SDR mode

bit 22 **DASSERT:** Chip Select Assert bit
- 1 = Chip Select is deasserted after transmission or reception of the specified number of bytes
- 0 = Chip Select is not deasserted after transmission or reception of the specified number of bytes

bit 21-20 **DEVSEL<1:0>:** SQI Device Select bits
- 11 = Reserved
- 10 = Reserved
- 01 = Select Device 1
- 00 = Select Device 0

bit 19-18 **LANEMODE<1:0>:** SQI Lane Mode Select bits
- 11 = Reserved
- 10 = Quad Lane mode
- 01 = Dual Lane mode
- 00 = Single Lane mode

bit 17-16 **CMDINIT<1:0>:** Command Initiation Mode Select bits

If it is Transmit, commands are initiated based on a write to the transmit register or the contents of TX buffer. If CMDINIT is Receive, commands are initiated based on reads to the read register or RX buffer availability.
- 11 = Reserved
- 10 = Receive
- 01 = Transmit
- 00 = Idle

bit 15-0 **TXRXCOUNT<15:0>:** Transmit/Receive Count bits

These bits specify the total number of bytes to transmit or received (based on CMDINIT).

Note 1: When this bit is set to '1', the SQI module uses the SQI1MEMSTAT register to control the status check command process.

REGISTER 22-9: SQI1INTSTAT: SQI INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
	—	—	—	—	DMA EIF	PKT COMPIF	BD DONEIF	CON THRIF
7:0	R/W-1, HS	R/W-0, HS	R/W-1, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS	R/W-0, HS	R/W-1, HS
	CON EMPTYIF	CON FULLIF	RXTHRIF(1)	RXFULLIF	RX EMPTYIF	TXTHRIF	TXFULLIF	TX EMPTYIF

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **DMAEIF:** DMA Bus Error Interrupt Flag bit
1 = DMA bus error has occurred
0 = DMA bus error has not occurred

bit 10 **PKTCOMPIF:** DMA Buffer Descriptor Processor Packet Completion Interrupt Flag bit
1 = DMA BD packet is complete
0 = DMA BD packet is in progress

bit 9 **BDDONEIF:** DMA Buffer Descriptor Done Interrupt Flag bit
1 = DMA BD process is done
0 = DMA BD process is in progress

bit 8 **CONTHRIF:** Control Buffer Threshold Interrupt Flag bit
1 = The control buffer has more than THRES words of space available
0 = The control buffer has less than THRES words of space available

bit 7 **CONEMPTYIF:** Control Buffer Empty Interrupt Flag bit
1 = Control buffer is empty
0 = Control buffer is not empty

bit 6 **CONFULLIF:** Control Buffer Full Interrupt Flag bit
1 = Control buffer is full
0 = Control buffer is not full

bit 5 **RXTHRIF:** Receive Buffer Threshold Interrupt Flag bit(1)
1 = Receive buffer has more than RXINTTHR words of space available
0 = Receive buffer has less than RXINTTHR words of space available

bit 4 **RXFULLIF:** Receive Buffer Full Interrupt Flag bit
1 = Receive buffer is full
0 = Receive buffer is not full

bit 3 **RXEMPTYIF:** Receive Buffer Empty Interrupt Flag bit
1 = Receive buffer is empty
0 = Receive buffer is not empty

Note 1: In the case of Boot/XIP mode, the POR value of the receive buffer threshold is zero. Therefore, this bit will be set to a '1', immediately after a POR until a read request on the System Bus bus is received.

Note: The bits in the register are cleared by writing a '1' to the corresponding bit position.

REGISTER 24-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R-0, HS, HC	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>(1)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:	HS = Hardware set	HC = Hardware cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **SLPEN:** Run During Sleep Enable bit
- 1 = UARTx BRG clock runs during Sleep mode
- 0 = UARTx BRG clock is turned off during Sleep mode

Note: SLPEN = 1 only applies if CLKSEL = FRC. All clocks, as well as the UART, are disabled in Deep Sleep mode.

bit 22 **ACTIVE:** UARTx Module Running Status bit
- 1 = UARTx module is active (UxMODE register should not be updated)
- 0 = UARTx module is not active (UxMODE register can be updated)

bit 21-19 **Unimplemented:** Read as '0'

bit 18-17 **CLKSEL<1:0>:** UARTx Module Clock Selection bits
- 11 = BRG clock is PBCLK2
- 10 = BRG clock is FRC
- 01 = BRG clock is SYSCLK (turned off in Sleep mode)
- 00 = BRG clock is PBCLK2 (turned off in Sleep mode)

bit 16 **RUNOVF:** Run During Overflow Condition Mode bit
- 1 = When an Overflow Error (OERR) condition is detected, the shift register continues to run to remain synchronized
- 0 = When an Overflow Error (OERR) condition is detected, the shift register stops accepting new data (Legacy mode)

bit 15 **ON:** UARTx Enable bit
- 1 = UARTx module is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
- 0 = UARTx module is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx, and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 25-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	RDSTART	—	—	—	—	—	DUALBUF	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP(2)	CS2P(2)	CS1P(2)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start Read on PMP Bus bit
This bit is cleared by hardware at the end of the read cycle.
1 = Start a read cycle on the PMP bus
0 = No effect

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Parallel Master Port Dual Read/Write Buffer Enable bit
This bit is only valid in Master mode.
1 = PMP uses separate registers for reads and writes
Reads: PMRADDR and PMRDIN
Writes: PMRWADDR and PMDOUT
0 = PMP uses legacy registers for reads and writes
Reads/Writes: PMADDR and PMRDIN

bit 16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit(1)
1 = PMP enabled
0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = All 16 bits of address are multiplexed on PMD<15:0>
10 = All 16 bits of address are multiplexed on PMD<7:0>
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 8 bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 27-1: CEVER: CRYPTO ENGINE REVISION, VERSION, AND ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **REVISION<7:0>:** Crypto Engine Revision bits

bit 23-16 **VERSION<7:0>:** Crypto Engine Version bits

bit 15-0 **ID<15:0>:** Crypto Engine Identification bits

TABLE 30-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
0100	C1FLTCON4	31:16	FLTEN19	MSEL19<1:0>		FSEL19<4:0>					FLTEN18	MSEL18<1:0>		FSEL18<4:0>					0000
		15:0	FLTEN17	MSEL17<1:0>		FSEL17<4:0>					FLTEN16	MSEL16<1:0>		FSEL16<4:0>					0000
0110	C1FLTCON5	31:16	FLTEN23	MSEL23<1:0>		FSEL23<4:0>					FLTEN22	MSEL22<1:0>		FSEL22<4:0>					0000
		15:0	FLTEN21	MSEL21<1:0>		FSEL21<4:0>					FLTEN20	MSEL20<1:0>		FSEL20<4:0>					0000
0120	C1FLTCON6	31:16	FLTEN27	MSEL27<1:0>		FSEL27<4:0>					FLTEN26	MSEL26<1:0>		FSEL26<4:0>					0000
		15:0	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					FLTEN24	MSEL24<1:0>		FSEL24<4:0>					0000
0130	C1FLTCON7	31:16	FLTEN31	MSEL31<1:0>		FSEL31<4:0>					FLTEN30	MSEL30<1:0>		FSEL30<4:0>					0000
		15:0	FLTEN29	MSEL29<1:0>		FSEL29<4:0>					FLTEN28	MSEL28<1:0>		FSEL28<4:0>					0000
0140-0330	C1RXFn (n = 0-31)	31:16	SID<10:0>											--	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
0340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0																	0000
0350	C1FIFOCONn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
0360	C1FIFOINTn (n = 0)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
0370	C1FIFOUAn (n = 0)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
0380	C1FIFOCIn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000
0390-0B40	C1FIFOCONn C1FIFOINTn C1FIFOUAn C1FIFOCIn (n = 1-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
		31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
		31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 39-7: SDHCCON1: SDHC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WKONREM	WKONINS	WKONINT
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	HC, R/W-0	R/W-0
	—	—	—	—	INTBG	RDWTCON	CONTREQ	SBGREQ
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	SDBP
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	CDSSEL	CDTLVL	—	DMASEL<1:0>		HSEN	DTXWIDTH	—

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **WKONREM:** Wake-up Event Enable on SD Card Removal bit
1 = Wake-up event is enabled
0 = Wake-up event is disabled

bit 25 **WKONINS:** Wake-up Event Enable on SD Card Insertion bit
1 = Wake-up event is enabled
0 = Wake-up event is disabled

bit 24 **WKONINT:** Wake-up Event Enable on SD Card Interrupt bit
1 = Wake-up event is enabled
0 = Wake-up event is disabled

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **INTBG:** Interrupt at Block Gap bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **RDWTCON:** Read Wait Control bit
1 = Read wait control is enabled
0 = Read wait control is disabled

bit 17 **CONTREQ:** Continue Request bit
A write to this bit is ignored if STOPREQ is set to '1'.
1 = Restart
0 = No effect

bit 16 **SBGREQ:** Stop at Block Gap Request bit
1 = Stop
0 = Transfer

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **SDBP:** SD Bus Power bit
1 = Bus power is on
0 = Bus power is off

bit 7 **CDSSEL:** Card Detect Signal Selection bit
1 = The card detect test level is select (for test purposes)
0 = SDCDx is selected (for normal use)

bit 6 **CDTLVL:** Card Detect Test Level bit
1 = Card is inserted
0 = Card is not inserted

REGISTER 41-10: CFGEBIA: EXTERNAL BUS INTERFACE ADDRESS PIN CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-0 **EBIA23EN:EBIA0EN:** EBI Address Pin Enable bits
1 = EBIAx pin is enabled for use by EBI
0 = EBIAx pin has is available for general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

TABLE 44-19: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	—	—	10	µs	See **Note 1**
D313	DACREFH	CVREF Input Voltage Reference Range	AVSS	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24		CVRCON<CVRR> = 1
			—	—	DACREFH/32		CVRCON<CVRR> = 0
D316	DACACC	Absolute Accuracy(2)	—	—	1/4	LSB	DACREFH/24, CVRCON<CVRR> = 1
			—	—	1/2	LSB	DACREFH/32, CVRCON<CVRR> = 0

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 44-24: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OS51	FSYS	System Frequency	DC	—	200	MHz	USB module disabled
			30	—	200	MHz	USB module enabled
OS55a	FPB	Peripheral Bus Frequency	DC	—	100	MHz	For PBCLKx, 'x' < 7
OS55b			DC	—	200	MHz	For PBCLK7
OS56	FREF	Reference Clock Frequency	—	—	50	MHz	For REFCLK1, REFCLK3, REFCLK4, REFCLKO1, REFCLK3, and REFCLK4 pins

TABLE 44-25: SPLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OS50	FIN	PLL Input Frequency Range	5	—	64	MHz	ECPLL, HSPLL, FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	100	µs	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period
OS54	FVCO	PLL VCO Frequency Range	350	—	700	MHz	—
OS54a	FPLL	PLL Output Frequency Range	10	—	200	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter \quad \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter \quad \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} \quad \frac{D_{CLK}}{1.41}$$

TABLE 44-48: TEMPERATURE SENSOR SPECIFICATIONS

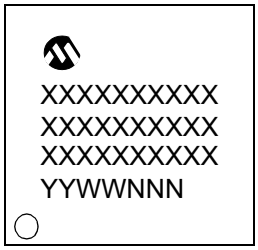
AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TS10	VTS	Rate of Change	—	5	—	mV/ºC	—
TS11	TR	Resolution	-2	—	+2	ºC	—
TS12	IVTEMP	Voltage Range	0.5	—	1.5	V	—
TS13	TMIN	Minimum Temperature	—	-40	—	ºC	IVTEMP = 0.5V
TS14	TMAX	Maximum Temperature	—	160	—	ºC	IVTEMP = 1.5V

Note 1: The temperature sensor is functional at VBORIOMIN < VDDIO < VDDIOMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

46.0 PACKAGING INFORMATION

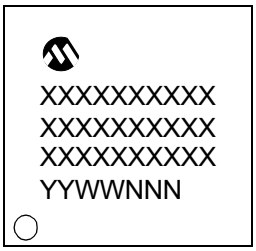
46.1 Package Marking Information

169-Lead LFBGA (11x11x1.56 mm)

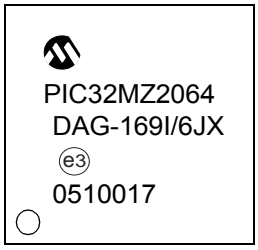


Example

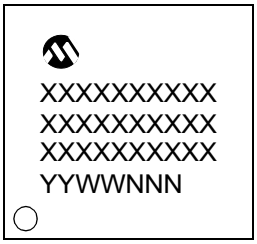
169-Lead LFBGA (11x11 mm)



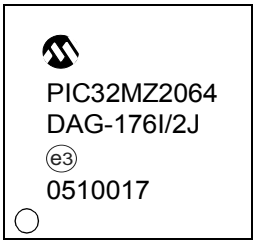
Example



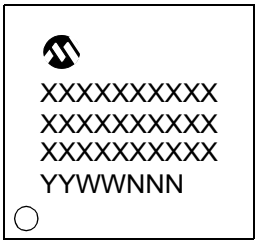
176-Lead LQFP (20x20x1.45 mm)



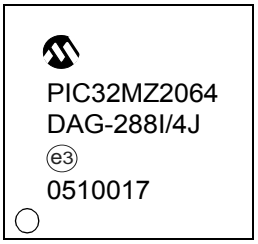
Example



288-Lead LFBGA (15x15x1.4 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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